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Review

Metal-Insulator-Metal Single Electron Transistors with Tunnel Barriers Prepared by Atomic Layer Deposition

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Abstract: Single electron transistors are nanoscale electron devices that require thin, high-quality tunnel barriers to operate and have potential applications in sensing, metrology and beyond-CMOS computing schemes. Given that atomic layer deposition is used to form CMOS gate stacks with low trap densities and excellent thickness control, it is well-suited as a technique to form a variety of tunnel barriers. This work is a review of our recent research on atomic layer deposition and post-fabrication treatments to fabricate metallic single electron transistors with a variety of metals and dielectrics.

Keywords: single electron transistor; atomic layer deposition; tunnel barrier

1. Introduction

Single electron tunneling transistors (SETs) utilize the Coulomb blockade effect experienced by electrons travelling through a nanoscale "island" between the source and drain. The transport mechanism responsible for transfer of charge is quantum mechanical tunneling through thin layers of dielectrics connecting the island to the external electrodes, thus forming metal-insulator-metal (MIM) junctions. (In actuality, the devices discussed in this paper have M-I-M-I-M structure. We will refer to them as "MIM" SETs for the devices made using the same metal for the electrodes and island; if two different metals are used for the island and source/drain electrodes, the full sequence of materials will be presented; we will use the generic term "metal-based SET" for any SET device which uses metals (as opposed to semiconductors) for the island and electrodes.) Since the first experimental demonstration almost 30 years ago [1], the dominant technique for making the ultrathin tunnel barriers required for SET operation has remained the controlled oxidation of the metals forming the devices. The performance of SETs is critically dependent on the quality of the dielectrics forming the tunnel barriers. While oxidation of metals (Al, Nb, Cr, Ni, and Ti) to form tunnel junctions is possible, the quality of the resulting dielectric suffers from several detrimental effects. A very limited number of metals can form stable defect-free oxide dielectrics suitable for quantum tunneling. Devices fabricated using chromium [2,3] and titanium [4] oxides exhibit instabilities of junction resistance and excess noise caused by charge traps in the barriers. In addition, metal oxides such as TiO_x and NiO have the

disadvantage of low tunnel barrier heights (~100 meV for TiO_x [4] and ~200 meV for NiO [5]), which makes it difficult to operate devices at high temperatures. The most widely used metal for nanoscale MIM junctions is aluminum. It has the advantage of easily forming a stable oxide with a large band gap and band offset suitable for forming MIM junctions. Consequently, Al-based SETs have by far the most mature fabrication process, with the lowest noise [6] and the largest charging energy [7] among all MIM SET devices. Nonetheless, Al-based SETs still suffer from several detrimental effects. Zimmerman et al. [8] demonstrated that alumina (Al_2O_3) formed by controlled oxidation exhibits unquenchable long term drift in device characteristics. Rippard et al. [9] showed that there is a broad energy distribution of electron states inside Al_2O_3 and these states can provide low-energy single-electron channels through the oxide. Therefore, the search for suitable high quality dielectrics needs to be continued.

One promising fabrication method for the controllable formation of tunnel barriers is Atomic Layer Deposition (ALD), a self-limiting process that ideally allows the deposition of films, including non-native oxides, with single monolayer accuracy. In this paper we summarize experimental results of MIM SETs fabricated with electrodes of either noble metals (Pt and Pd) or a metal that allows chemical reduction of its native oxide (Ni). The formation of the tunnel barriers, which are not a native oxide of the metals used, is by ex-situ atomic layer deposition of ALD using Al_2O_3, SiO_2, their combination, as well as SiN_x. Two ALD tools were used in fabrication: a Savannah ALD system from Ultratech/Cambridge NanoTech with an integrated ozone generator and a FlexAl ALD system from Oxford Instruments with a remote plasma reactor which enables plasma-enhanced ALD (PEALD).

2. Materials and Methods

To investigate the applicability of ALD to tunnel barrier formation, we fabricate "cross-tie" SETs, as illustrated in Figure 1. The process involves fabrication of two metal layers defined by electron-beam lithography (EBL, Vistec, Jena, Germany) with ALD dielectric in between. The general approach for fabrication of SETs in the cross-tie geometry is outlined below, while more fabrication details are given within the results subsections.

In the first step, the bottom metal layer defining the source and drain electrodes (20–40 nm thick, 50 nm wide) is deposited by electron beam evaporation through the EBL-defined mask on 500 nm of thermally grown SiO_2, as shown in Figure 1a. After liftoff and cleaning, the dielectric barrier is deposited using ALD (Figure 1b). Finally, the top metal layer forming a cross-tie island (20–50 nm thick) is defined by evaporating the metal through the EBL-defined mask and liftoff (Figure 1c). In cross-tie SETs, inert metals such as platinum (Pt) and palladium (Pd) were studied as electrode materials to avoid the influence of native metal oxides in the MIM junctions.

The resulting structures feature two nominally identical junctions, the capacitance of which can be estimated from a parallel-plate approximation $C_d = C_s = \varepsilon\varepsilon_0 A/d$ where ε_0 and ε are the vacuum permittivity and the dielectric constant of a chosen ALD dielectric, A is the junction area defined by the overlap between the island and each lead, and d is the thickness of the barrier. For a 1 nm thick SiO_2 (Al_2O_3) tunnel barrier with a junction area of ~4000 nm^2 (Figure 1d), the parallel plate model gives a capacitance value of ~180(350) aF (using bulk values of $\varepsilon = 3.9$ for SiO_2 and $\varepsilon = 9$ for Al_2O_3). The charge population of the island is controlled by an electrostatic gate situated 0.5 to 5 um away from the island (shown in Figure 1d) resulting in an experimentally determined capacitance of 0.1 to 30 aF. Assuming a gate capacitance much smaller than the junction capacitance, the total island capacitance for device is, therefore, ~350–400 aF for an SiO_2 barrier and ~700–900 aF for an Al_2O_3 barrier.

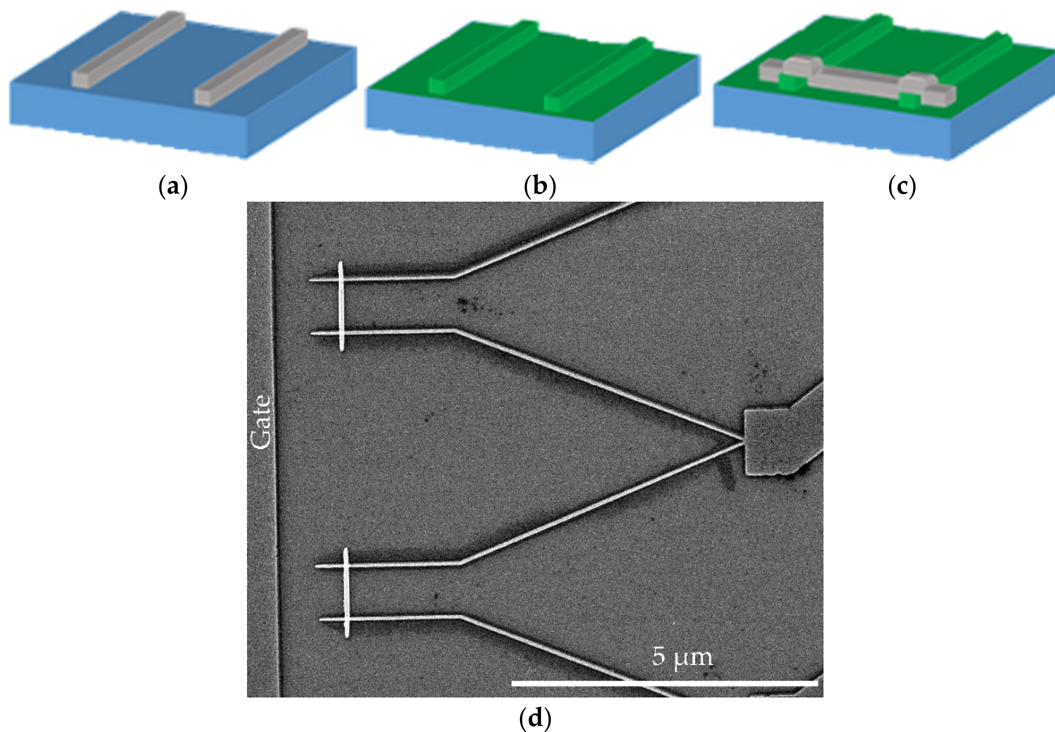

Figure 1. "Cross-tie" fabrication of single electron transistors (SETs): (**a**) the metal source and drain (shown in grey) are deposited on thermal SiO_2 (shown in blue) using electron beam lithography (EBL) and liftoff; (**b**) the sample is blanket coated by a dielectric (shown in green) using atomic layer deposition (ALD) to form the tunnel barrier (usually about 1 nm thick); (**c**) EBL and liftoff are used to form the metal island of the single electron transistor (SET) (shown in grey); and (**d**) micrograph of two cross-tie SETs. The wide line on the far left is the gate electrode and the narrow vertical lines are the metal islands.

This sum of the capacitances C_Σ defines the figure of merit for an SET, the charging energy $E_C = e^2/2C_\Sigma$ [10], where e is electron charge, the calculated value of which is ~0.2 meV for an SiO_2 barrier or 0.1 meV for Al_2O_3. Thus, the chosen design enables observation of well-developed Coulomb blockade at an experimentally attainable temperature T = 0.3 K << E_C/k_B where k_B is the Boltzmann constant.

A modification of this process, known as "half damascene" fabrication, is used to decrease the overlap of the source and drain with the island by fabricating an island inlaid in the substrate dielectric (Figure 2) [11]. This lowers the capacitance of the junctions by narrowing the width of the island and avoiding the side overlap always present in cross-tie design and thus raises the maximum operating temperature of the device. To fabricate the inlaid island devices, the pattern of the island is etched into the oxide in an inductively coupled plasma (ICP, Oxford, Abingdon, UK) etcher [12] (Figure 2b). Metal is deposited by e-beam evaporation to fill the trench in the SiO_2 (Figure 2c) and chemical mechanical polishing (CMP, Logitech, Glasgow, UK) is then used to remove any residual metal on the oxide field, while leaving the island trench filled with metal (Figure 2d). CMP enables a very significant decrease in the junction area and can be used to fabricate a full-damascene metallic SET [13]. Next, ALD is used to form the tunnel barrier over the island (Figure 2e). Finally, the source and drain are defined using the same process as for the cross-tie devices (Figure 2f). The overlap area of the junctions prepared by these techniques was in the range 500–1000 nm^2 (Figure 2g, gate not shown). Source and drain junctions of 1000 nm^2, together with a gate capacitance of 0.1 aF, result in an island capacitance of 70 aF. With this capacitance, the charging energy is expected to exceed 1 meV, allowing well-developed Coulomb blockade to be observed at temperatures up to ~3 K.

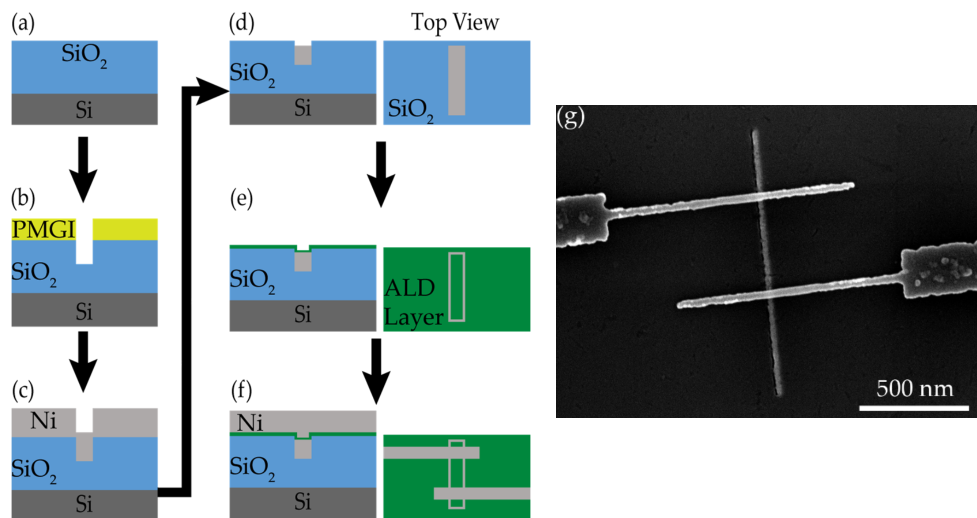

Figure 2. Process steps in fabricating the "half-damascene" cross-tie SET: (**a**) Si substrate (dark grey) is oxidized (SiO_2 in blue); (**b**) a trench for the island is etched through an EBL defined polymethylglutarimide (PMGI) mask (yellow); (**c**) metal (light grey, e.g. Ni) is deposited; (**d**) the chemical mechanical polishing (CMP) step is performed and metal island is formed; (**e**) ALD dielectric (green) is deposited; (**f**) metal source and drain electrodes (light grey) are deposited; and (**g**) micrograph of half-damascene SET (gate not shown). The nearly vertical line is the inlaid island and the slightly wider, nearly horizontal lines are the source and drain.

The metal used in half-damascene and full-damascene SET structures was Ni due to its good adhesion to SiO_2, relative oxidation resistance, and well-established CMP process.

The thickness of the barrier is estimated using the known deposition rate for the ALD process and has been validated by transmission electron microscopy (TEM, FEI, Hillsboro, OR, USA) [11,14]. In order for the electron wave function to be localized to the island the junction resistance R_J must satisfy the following condition: $R_J > R_Q$ [10] (where $R_Q = h/e^2$ is the quantum resistance, h is Planck's constant, and e is the elementary charge). Our experiments show that to fulfill this condition at least 9 Al_2O_3 ALD cycles or 12 SiO_2 ALD cycles (~1 nm in both cases) are required to form the tunnel barrier dielectric; otherwise, the number of devices with short circuited junctions exceeds 50%.

Following fabrication, devices are wire bonded to a ceramic chip carrier and placed in a closed-cycle refrigerator (CCR) for electrical characterization. Two CCRs were used in this study: a ^{4}He CCR with a base temperature ~3.5 K (Advanced Research Systems, Macungie, PA, USA), and a ^{3}He CCR with a base temperature of ~0.3 K (Janis Research Company, Woburn, MA, USA); the temperature of the sample is monitored by a thermometer attached to the chip carrier. Low temperature characterization was performed on a total of more than 100 devices (Pt-ALD dielectric-Pt and Ni-ALD dielectric-Ni structures) resulting from more than 10 fabrication runs.

Electrical measurements of differential conductance of the devices, $G = dI/dV_{ds}$, are performed using standard lock-in techniques with a 10–1000 µV excitation voltage at low frequencies (8–38 Hz). For spectral analysis of noise, a spectrum analyzer (based on a UHF lock-in amplifier from Zurich Instruments, Zurich, Switzerland) connected to the output of the current amplifier was used.

3. Results

3.1. Devices Featuring Pt-ALD Dielectric-Pt Junctions

3.1.1. Initial Experiments: SETs with H_2O-Based ALD of the Tunnel Barrier

The first experimental demonstration of a metal-based SET fabricated using ALD dielectric was reported in [15]. In those experiments, the source/drain leads of the SET were first defined by

evaporating 10/20 nm of Ti/Pt through an EBL-defined pattern on a double layer methyl methacrylate (MMA)/polymethyl methacrylate (PMMA) resist, followed by a lift-off in acetone. Before the dielectric deposition, the sample was cleaned in an oxygen plasma barrel etcher for 2–3 min to remove any e-beam resist residue from the previous step. Next, a layer of Al_2O_3 with a target thickness of ~1 nm was deposited in a Savannah S100 ALD system by Cambridge Nanotech at 200 °C using nine cycles of trimethylaluminum $Al(CH_3)_3$ (TMA) and H_2O as precursors. Finally, the SET island was defined by a second EBL and deposition of 10/30 nm of Ti/Pt at 1×10^{-6} Torr base pressure. The resulting devices (with Pt-Al_2O_3-Ti-Pt tunnel junctions) showed characteristic Coulomb blockade oscillations (CBOs) of conductance with applied gate voltage [15], but it was also observed that the electrical characteristics of these devices strongly deviated from that expected for metal-based SETs.

According to the orthodox model of Coulomb blockade [16], when a metal-based SET is cooled to a temperature $T \approx E_C/k_B$ the differential conductance at V_{ds} = 0 mV (where V_{ds} is the drain to source voltage) decreases towards $G_0/2$, where $G_0 = G(|V_{ds}| >> 2E_C/e)$ due to a reduction in the island occupation probability imposed by Coulomb blockade [17]. For $\phi_B/e >> |V_{ds}| > 2E_C/e$ (where ϕ_B is the tunnel barrier height), the Coulomb blockade is lifted and the SET should exhibit an almost constant differential conductance that approaches G_0. However, the zero-bias conductance of Pt-Al_2O_3-Ti-Pt SETs in [15] at low temperatures was significantly lower than $G_0/2$, and the temperature dependence of this conductance indicated the presence of an in-series thermally activated component. Moreover, the device was retested 5 weeks after the initial fabrication, and it was found that its conductance at room temperature decreased significantly (by a factor of >100) while at low temperature G_0 was too low to be measured, indicating a freeze out of carriers, and no evidence of CBOs was observed. It appears reasonable that over time the Ti layer at the bottom of Ti/Pt island reacted with the ALD layer and altered the tunnel barriers, most likely leading to a formation of an insulating ternary Ti_xAl_yO compound. This observation is consistent with reports on ternary Ti_xAl_yO compounds [18,19], where a 1000-fold increase of resistance as compared to TiO_2 and a dielectric constant of 62 was reported. Such a large dielectric constant results in a charging energy smaller than k_BT and attenuates gate modulation so that CBOs disappear.

To avoid this problem, in subsequent experiments the Ti adhesion layer was excluded from the top metal layer, and pure Pt was used as the SET island material. A Coulomb diamond plot or "charge stability diagram" [10] of a typical Pt-Al_2O_3-Pt device fabricated with nine cycles of ALD Al_2O_3 (~1 nm) is shown in Figure 3a. One immediately noticeable difference between this device (with Pt-Al_2O_3-Pt junctions) and the one reported in [15] (with Pt-Al_2O_3-Ti-Pt junctions) is that the value of the zero-bias differential conductance measured in a peak of the CBOs is much closer to the expected value $G(V_{ds} = 0\text{ mV}) \approx G_0/2$ (Figure 3b). Further analysis of the plot by fitting it to the orthodox model [16,20] enables estimation of the junction parameters (C_S = 240 aF; G_S = 35 µS; C_d = 160 aF; G_d = 45 µS; C_g = 32 aF (the value of gate capacitance can be extracted from the period of CBOs, $C_g = e/dV_g$, where dV_g is a voltage difference between adjacent CBO peaks) and charging energy E_C = 0.185 meV. The total capacitance (C_Σ = 432 aF) is lower than expected from the parallel plate model estimate (~700–900 aF) potentially due to the low dielectric constant of very thin Al_2O_3 films compared to the bulk value [21]. Unexpectedly, the differential conductance of the devices steadily increased over the course of several months, approaching values expected for shorted metal structures with no dielectric barriers (~1 mS). This clearly indicates the instability of the Al_2O_3 tunnel barrier on a Pt substrate using TMA and H_2O precursors. We will discuss a probable cause for this below.

Another metal studied in combination with H_2O-based ALD Al_2O_3 was Pd. However, devices fabricated with Pd as a metal onto which ALD Al_2O_3 was deposited exhibited a much broader spread of junction resistances compared to Pt-based devices, possibly due to greater surface roughness of the Pd film compared to the Pt film, as shown by atomic force microscopy measurements [22].

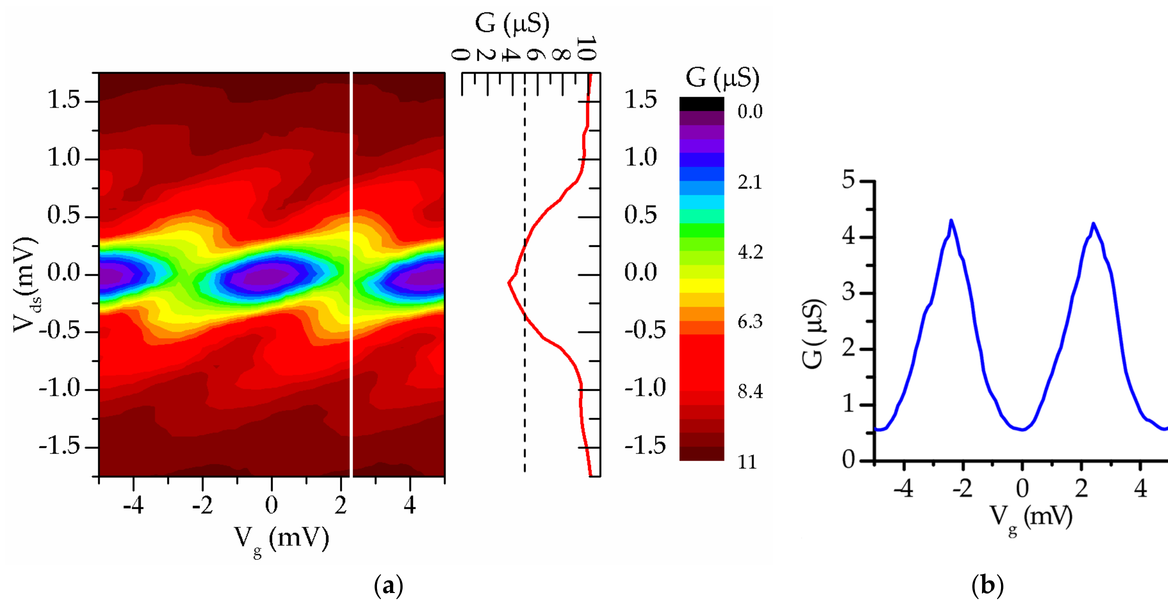

Figure 3. Electrical characterization of Pt-Al_2O_3-Pt SET prepared using nine ALD cycles of Al_2O_3 (~1 nm) with no post fabrication treatments: (**a**) Coulomb diamond plot and $G(V_{ds})$ dependence for V_g = 2.3 mV (a peak of Coulomb blockade oscillation). Note that zero bias conductance $G(V_{ds}$ = 0 mV) is just slightly below the $G_0/2$ value (indicated by the dashed line) expected from orthodox theory; (**b**) Coulomb Blockade Oscillations (CBOs) for V_{ds} = 0 mV. T = 0.3 K, measurements were performed immediately after fabrication.

3.1.2. O_3-Based vs. H_2O-Based ALD of Al_2O_3 in SETs

Initial experiments described above indicated that H_2O-based ALD of tunnel barriers resulted in functional devices, but these suffered from intrinsic barrier instabilities resulting in irreversible detrimental changes in the device performance. An alternative method for forming Al_2O_3 in the Cambridge Savannah ALD reactor is to use a different oxidizer by replacing H_2O with O_3 from a dedicated ozone generator. To investigate the difference between H_2O-based ALD and O_3-based ALD, two batches of Pt-Al_2O_3-Pt SET devices were fabricated with an equal number of ALD cycles using ozone and water [14]. It was discovered that SETs that used H_2O-based ALD showed much lower resistance than SETs fabricated with O_3-based ALD for a given number of ALD cycles. For both batches, nine cycles of ALD (~1 nm in thickness) were used as this was found to be an optimal balance between complete coverage of the barrier over the electrodes and measureable tunneling currents. Structures fabricated using H_2O showed an average resistance of around 1 MΩ with a very significant spread of resistances ranging from tens of kΩ to several MΩ. Again, after a few weeks at ambient conditions, the resistance of these devices dropped to about 10 kΩ. In contrast, the as-prepared, O_3-based devices showed an average resistance of almost 1 GΩ. Low temperature (~5 K) testing of both O_3- and H_2O-based devices revealed, in addition to a "dip" near V_{ds} = 0 mV related to Coulomb blockade, a temperature dependent monotonic increase of conductance with increasing bias outside of the Coulomb gap ($|V_{ds}| > 2E_c/e$) contrary to orthodox Coulomb blockade theory [16]. This indicates the presence of a parasitic non-metallic component in series with the tunnel barrier in the junctions.

One technique frequently used to improve the quality of thin films is annealing, which can passivate fabrication defects [23]. However, the results of annealing the SETs after fabrication (375 °C for 3 min in an Ar environment) differed drastically depending on the oxidant used in the ALD process for devices fabricated with the same number of deposition cycles. Namely, most of the H_2O-based devices developed electrical shorts after annealing. In contrast, the resistance of devices fabricated with O_3-based ALD dropped by approximately two orders of magnitude after annealing under the same conditions, yet they did not develop any shorts. Instead, the resistance became quite

uniformly reduced to a few MΩs and remained stable over time (for at least six months, the longest observation time available). When tested again at ~5 K with $|V_{ds}| > 2E_C/e$ applied, the annealed O_3-based devices displayed almost constant differential conductance, as expected from orthodox Coulomb blockade theory. (The value of the charging energy in these experiments—as estimated above from the parallel plate model—is on the order of 5 K, precluding observation of developed Coulomb blockade at the temperature of experiment (~5 K).) Interestingly, the shape of the Coulomb blockade "dip", which is a function of the charging energy of the island, did not change noticeably with annealing, indicating that the junction capacitance was not noticeably changed [14].

Analysis by TEM and energy dispersive x-ray spectroscopy (EDX) showed a disproportionate amount of oxygen (compared to aluminum) at the bottom Pt/Al_2O_3 interface, suggesting that the bottom platinum layer was slightly oxidized during the ALD process [14]. Since platinum oxide is thermodynamically unstable, its presence would explain the change in conductance after annealing for both ozone- and water-based devices and the long-term instability of water-based devices [24,25]. According to calculations of the change in Gibbs free energy, PtO_2 should be readily reduced by hydrogen even at room temperature. However, exposing ozone-based devices to forming gas (5% H_2 in Ar) at near room temperature (32 °C) for 1 h caused an increase in the device conductance by about a factor of 30 (0.5 to 15 nS) which is a smaller change compared to that observed after high-temperature annealing in Ar. This suggests not all of the platinum oxide is reduced at low temperatures [14], probably due to slower diffusion of molecular hydrogen and slower reaction rates. Upon raising the temperature, further increases in conductance were observed as can be seen in Figure 4.

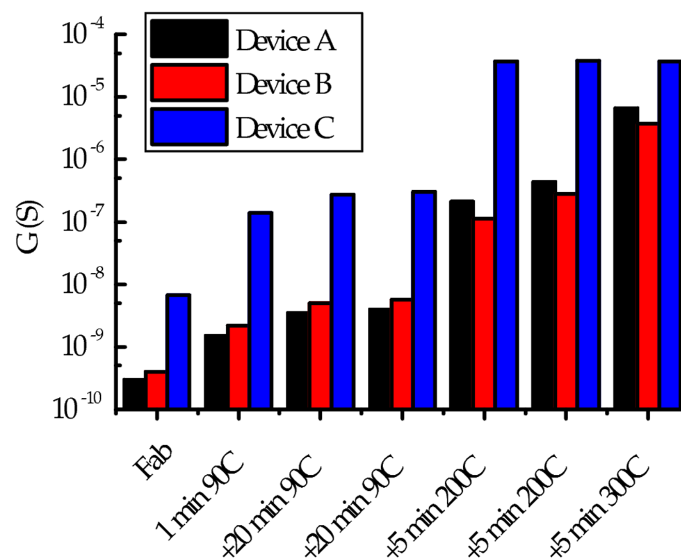

Figure 4. Measurement of three $Pt\text{-}Al_2O_3\text{-}Pt$ devices from the same die displaying how successive treatments using longer exposures to forming gas and higher temperatures caused further increases in conductance.

Another observation that supports the idea of platinum oxide formation was the time-dependent decrease in conductance following the forming gas treatments. Figure 5 shows the change of the room temperature conductance of a device over a 23-h period immediately after treatment in forming gas at 90 °C for 20 min; as can be seen, the conductance drops by almost an order of magnitude. This can be explained by re-oxidation of the Pt electrodes from the edge of the tunnel barriers in the device. As mentioned above, treatment in forming gas at lower temperatures does not appear to completely reduce the parasitic oxide as further increases in conductance were observed when subsequently higher temperatures were used (Figure 4). The time-dependent drop in conductance suggests that

when the devices are taken out of the anneal chamber into the oxygen-containing ambient, a thin ring of platinum around the edge of the tunnel barrier begins to re-oxidize and "pinch-off" the current tunneling through the barrier as shown in Figure 6. At higher temperatures, when most of the platinum oxide is decomposed, this effect is negligible because the majority of the tunneling area is free of the parasitic oxide.

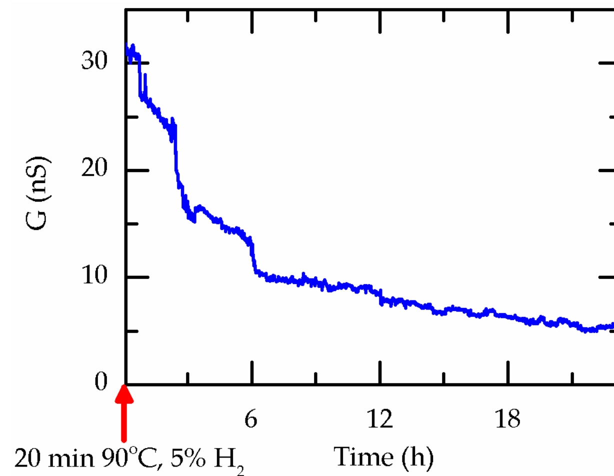

Figure 5. Single electron transistor (Pt-Al_2O_3-Pt) conductance at room temperature for an O_3-based device as a function of time immediately after an anneal in forming gas. The decrease in conductance is most likely caused by reoxidation near the edge of the tunnel barrier (Figure 6).

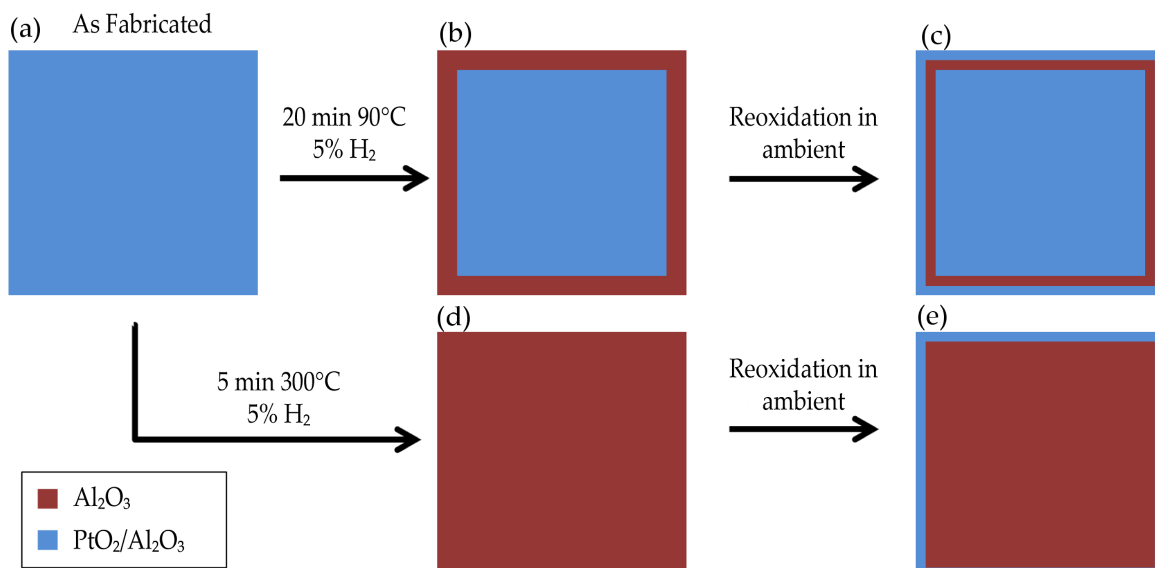

Figure 6. Illustration showing a top view of the reduction and reoxidation of Pt-Al_2O_3-Pt tunnel barriers. In as fabricated devices (**a**), electrons must travel through both the Al_2O_3 and the PtO_x (blue region). This thicker barrier causes low conductance. Treatment with forming gas at 90 °C only partially reduces the PtO_x (**b**) but this provides a region where the electrons can tunnel through just the Al_2O_3 layer (brown area). When brought back out into the oxygen-containing ambient, this more conductive region shrinks as the edge of the tunneling region is re-oxidized (**c**). The same process happens when the devices are treated at 300 °C but, since all the parasitic oxide is reduced in this case (**d**), the effect of re-oxidation is negligible (**e**).

Figure 7 shows the Coulomb diamond plot measured at 0.35 K for O_3-based devices treated with forming gas at 90 °C in a single post-fabrication step. The performance of these devices, however, was hampered by unusually high levels of excess noise far exceeding Johnson and shot noise levels typical for MIM SETs [26]. This noise is identified as random telegraph signal (RTS) noise [27], a topic that will be discussed below. Figure 7b shows a series of $G(V_{ds})$ characteristics measured in the peak of CBO at several temperatures for an O_3-based device treated in forming gas. It is clear that the conductance in the peaks of CBOs, instead of saturating at a level of $G_0/2$ (~55 nS in Figure 7b) as expected for MIM SETs, continues to drop with the lowering of temperature. An estimation of activation energy in the peak of blockade gives a value of less than 0.05 meV, typical for granular metals [28,29]. This observation suggests that a thin layer of platinum oxide survived the forming gas treatment and its presence in series with the Al_2O_3 tunnel barrier results in the weak activation behavior in the peaks of CBO at V_{ds} = 0 mV [29].

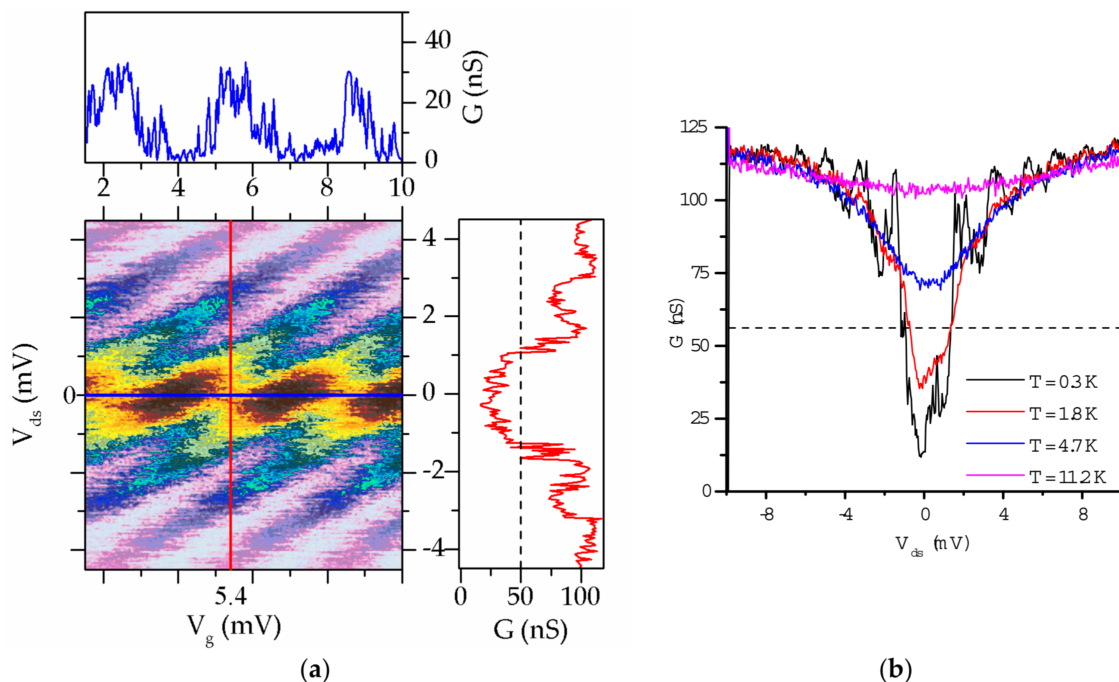

Figure 7. Electrical characteristics for O_3-based Pt-Al_2O_3-Pt SET after anneal in forming gas at 90 °C for 1 h: (**a**) diamond plot at 0.3 K with V_g (V_{ds} = 0 mV, blue) and V_{ds} (V_g = 5.4 mV, red) cross sections; and (**b**) $G(V_{ds})$ dependence of SET conductance measured in the peak of Coulomb blockade at several temperatures. The peaks of CBOs are below $G_0/2$ (black dashed line), contrary to Coulomb blockade theory for metal-insulator-metal SETs.

A comparison of experimental results obtained for two batches of devices featuring Pt-Al_2O_3-Pt junctions (Figures 3 and 7) with the exact same number of ALD cycles (nine) and similar overlap areas for the junctions shows a significant difference in charging energy. Namely, the charging energy for the H_2O-based device of Figure 3 ($E_C \approx$ 0.185 meV) as compared to the O_3-based device of Figure 7 ($E_C \approx$ 0.37 meV) was about two times smaller, while its conductance was about two orders of magnitude larger. This difference in charging energy is evidently caused by a difference in the junction capacitances and for the same area of the junctions a doubling of the dielectric thickness would result in half the capacitance and exponentially larger resistance, in reasonable agreement with the experiments. (This is admittedly just an "order of magnitude" estimate, because in both cases (Figures 3 and 7) the shape of the diamonds also indicates a significant difference in junction capacitances in each device, most likely caused by non-uniformities in the dielectric thickness and uncertainty in the junction area.) This observation suggests that the actual thickness of a dielectric is

different for the two different oxidant precursors with the same number of deposition cycles. Namely, the actual thickness of the dielectric in the water-based devices was about half of what was expected from the number of deposition cycles. The likely cause for this is the different effects of H_2O and O_3 oxidizing pulses on the nucleation delay and metal surface oxidation. This again provides evidence for the more aggressive action of O_3 in forming PtO_x (and potentially more uniform coverage) compared to H_2O. Note that in both cases values of junction capacitances are consistent with a reduced dielectric constant, $\varepsilon < 5$, compared to the bulk value ($\varepsilon \approx 9$) [21,30]. The above experiments also provide evidence that the formation of native oxide and interfacial layers, even on noble metals, can drastically change the properties of the MIM junctions.

PEALD of SiO_2 using O_2 plasma and Bis(diethylamino)silane was also attempted on platinum. Using a stencil mask to pattern 140 μm diameter capacitors, it was found that a continuous layer of SiO_2 was not formed until roughly 100 cycles of SiO_2 (~10 nm) had been deposited. This suggests the formation of a non-uniform SiO_2 film (in the form of islands) on the Pt substrate. It was unknown, however, whether the density of pinholes was high enough to prevent the fabrication of pinhole-free nanoscale SET junctions. To test this, a single experiment was run using 15 cycles of SiO_2 (~1.5 nm) to form Pt-SiO_2-Pt SETs using the cross-tie fabrication process. All of these devices (~40) were shorted, supporting the theory that the film has a high density of pinholes where SiO_2 never nucleated. This, together with the previous experiments, supports the hypothesis that ALD nucleation on inert metal substrates, such as platinum and palladium, is a challenge and limits the choice of materials and methods for deposition.

3.2. Devices Featuring Ni-ALD Dielectric-Ni Junctions

Our experimental results obtained with Pt electrodes indicate that a fundamental issue with the use of ALD tunnel barriers in MIM junctions is that the presence of the oxidizing pulse (H_2O or O_3) will likely lead to partial oxidation of the metals in the SET. While the formation of native oxide promotes the nucleation and growth of the ALD dielectric, it drastically reduces the transparency of tunnel barriers making them unusable for target applications.

In order to solve the problem of ALD nucleation and the presence of parasitic native oxide, two different approaches were considered: (1) to use a metal that is more susceptible to oxidation than noble metals but whose oxide can be chemically reduced after the ALD dielectric step; and (2) to use an ALD process in which the tunnel barrier formation does not require an oxidizing pulse. Nickel was selected for the first approach because of its relative inertness, compared to Al and Ti, and the reducibility of its native oxide at temperatures that will not damage the barrier dielectric or cause deformation of the metal layer. SiN_x ALD was selected for the oxygen-free tunnel barrier formation where the N_2 plasma replaces the O_2, O_3, or H_2O pulse and therefore parasitic formation of the native oxide can be minimized. Below we discuss the results obtained using Ni-dielectric-Ni junctions with tunnel dielectric deposited in the Oxford FlexAL PEALD reactor.

3.2.1. SET Devices with Ni-SiO_2-Ni Tunnel Junctions

As discussed above, two issues must be addressed in order to successfully fabricate MIM SETs using an ALD process: the unavoidable oxidation of metals and determination of the appropriate number of cycles to form a pinhole-free tunnel barrier with desired transparency ($R_Q < R_J < 10^4 R_Q$). For that purpose two types of test structures were fabricated on an oxidized Si wafer: (1) single layer nanowires covered with PEALD SiO_2; and (2) liftoff-based cross-tie devices made of Ni-SiO_2-Ni tunnel junctions (as described earlier). The PEALD of SiO_2 was performed using Bis(diethylamino)silane and oxygen plasma with a nominal growth rate of 0.09 nm/cycle.

For cross-tie devices, reference structures ("metal short circuits") with no PEALD dielectric and without any associated oxygen plasma exposure were first fabricated and exhibited conductance of $G \approx 400$ μS, which is comparable with the conductance of a Ni nanowire with similar dimensions. However, devices with only two cycles of SiO_2 PEALD (≈0.2 nm) displayed a conductance below

$G \approx 5$ nS. This value is about four orders of magnitude smaller than the expected value $G \approx 50$ µS based on the Simmons approximation for 0.2 nm of uniform SiO_2 [31]. Furthermore, at low temperatures, strong suppression of conductance at $V_{ds} = 0$ mV along with a significant decrease of conductance over a broad range of V_{ds} was observed (Figure 8), which contradicts orthodox Coulomb blockade theory for MIM SETs [16]. This behavior is, as it was in the case of Pt-Al_2O_3-Pt devices, consistent with a parasitic NiO layer (or a granular metal NiO-Ni mix; we will refer to it as NiO for short) in series with the tunnel junctions (i.e., [Ni-NiO]-SiO_2-[NiO-Ni] instead of Ni-SiO_2-Ni), as it modifies the overall barrier for electron transport and leads to a thermal activation of conductance at low bias [5]. The oxygen plasma step in PEALD has been previously reported to oxidize the surface of the substrates [32–34]. Measurements of the decrease in conductance in single layer nanowires after being covered with 10 cycles of PEALD SiO_2 (~0.9 nm) indicate that the NiO layer is about 2 nm thick. Fortunately, NiO can be reduced to Ni by annealing in hydrogen at moderately high temperatures ≥300 °C [35–37]. We have found that a forming gas anneal (FGA) at 400 °C for 2 min in 5% H_2–95% Ar causes the conductance of the cross-tie structures with two cycles of PEALD SiO_2 to increase from $G \approx 5$ nS to $G > 600$ µS [11], while a 30 min FGA is required to increase the conductance of the Ni nanowire covered by ~1 nm of SiO_2 back to that of the as-deposited nanowires [11,38].

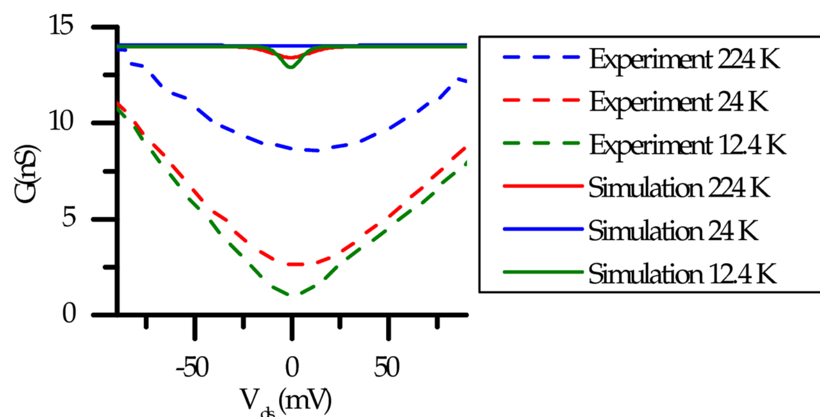

Figure 8. Evidence of parasitic oxide: Experimental and simulated $G(V_{ds})$ dependences for an untreated Ni-SiO_2-Ni SET at different temperatures.

This is consistent with hydrogen-promoted reduction of the parasitic NiO to Ni: H_2 + NiO = H_2O + Ni; the H_2O is removed during annealing [11,38]. Further measurements of cross-tie devices by TEM and EDX revealed that in addition to the oxide formation on the bottom Ni layer, the top Ni electrodes, deposited on the PEALD SiO_2, are likewise oxidized and that a second annealing step is required to reduce the parasitic NiO at the lower interface of the top Ni layer [11].

Based upon our observations, all cross-tie devices with less than 12 cycles of SiO_2 (<1.1 nm) subjected to two FGA steps ((1) for bottom electrode NiO reduction: 30 min, 400 °C and (2) for top electrode NiO reduction: 10 min, 300 °C both in 5% H_2–95% Ar) exhibited fairly high conductance, $G > 50$ µS $> 1/R_Q$. This is most likely due to non-uniformities in the deposited SiO_2, which lead to "pinholes" short-circuiting the top and bottom Ni electrodes [39]. However, for devices with 12 or 13 cycles treated with two anneal steps, the conductance matched the Simmons equation within an order of magnitude, suggesting the ALD growth had filled in the pinholes and both NiO layers had been mostly reduced.

The cause of oxidation in the top Ni electrodes remains to be investigated, but the oxidation of metals when deposited on SiO_2 has been reported for Cu, Mo, and W and has been attributed to oxygen containing contaminants, such as water, on the oxide surface [40,41]. Furthermore, substituting aluminum for nickel as the top electrode (Ni-SiO_2-Al) resulted in devices that were all electrical opens (i.e., no measurable tunneling current). This can be explained as resulting from the aluminum layer

oxidizing at the surface where it makes a contact with the SiO_2 film, just as the nickel layer had, but causing an even greater increase in resistance due to the large band gap of aluminum oxide. Likewise, substituting palladium for nickel on the top layer (Ni-SiO_2-Pd) shows behavior indicative of the top palladium layer oxidizing at the metal-SiO_2 interface but unlike Al_2O_3, this oxide can be reduced. These experiments suggest that the oxidation of the top metal layer is unavoidable (at least for oxide dielectrics such as Al_2O_3 and SiO_2) and that reducing the NiO at the top interface is therefore just as necessary as doing so at the bottom interface [11].

From the experiments described above it was concluded that 12–13 PEALD cycles of SiO_2 (~1.1 nm) are suitable for cross-tie SETs because the resulting conductance is sufficiently below the quantum conductance, $G_Q = 1/R_Q \approx 40$ µS, required to suppress quantum fluctuations [16], but high enough (>10 nS) to avoid signal-to-noise ratio problems.

3.2.2. Limitations of the "Double Anneal" Reduction Technique and Search for Alternative Reduction Methods

As described above, the proposed process for fabricating Ni-SiO_2/Al_2O_3-Ni SETs requires two reduction steps to eliminate the parasitic NiO in series with the tunnel junctions. However, prolonged exposure of the device to elevated temperatures (>375 °C) results in thermally induced deformation of the Ni nanowires, referred to as agglomeration [42] and consequently open circuits. Figure 9 shows a micrograph of agglomeration occurring in an SET device as a result of FGA at 400 °C.

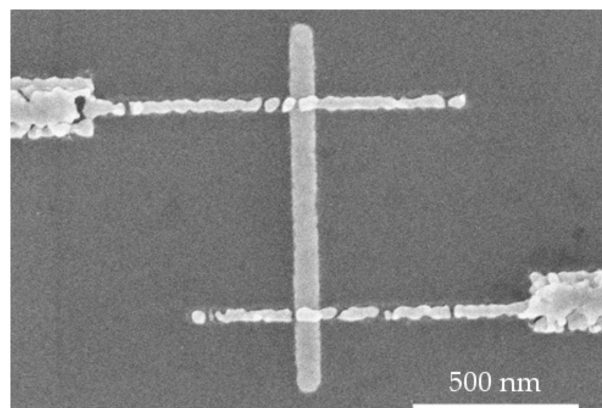

Figure 9. Scanning electron micrograph of a Ni-SiO_2-Ni device where strong agglomeration occurs after a forming gas anneal (FGA) at 400 °C for 30 min leading to the breaks in the source and drain electrodes (nearly horizontal broken lines).

In addition to the thermally-induced deformation of thin metal films during anneal, the experiments also reveal very significant "switching" RTS noise, similar to that observed in Pt-Al_2O_3-Pt devices (Figure 7). Figure 10a shows a measurement of conductance $G(V_{ds})$ with high V_{ds} resolution of an SET device subjected to two FGA treatments. The experimental data highlight the important feature of this noise: for $|V_{ds}| < 2E_c/e$ where Coulomb blockade is present, the conductance jumps between two or more states, but appears remarkably stable once Coulomb blockade is suppressed for $|V_{ds}| >> E_C/e$. By contrast, the sweep of gate bias, V_g, at $V_{ds} = 0$ mV (Figure 10b) reveals very strong intensity of the RTS noise almost uniformly occurring along the V_g axis. This behavior is consistent with random charge trapping/detrapping processes in the vicinity of the island (e.g., in the barrier dielectric) acting as a strong modulation randomly shifting the CBOs along the V_g axis. However, once Coulomb blockade is overcome (by applying $|V_{ds}| >> E_C/e$), these fluctuations are suppressed because the gate can no longer modulate the conductance.

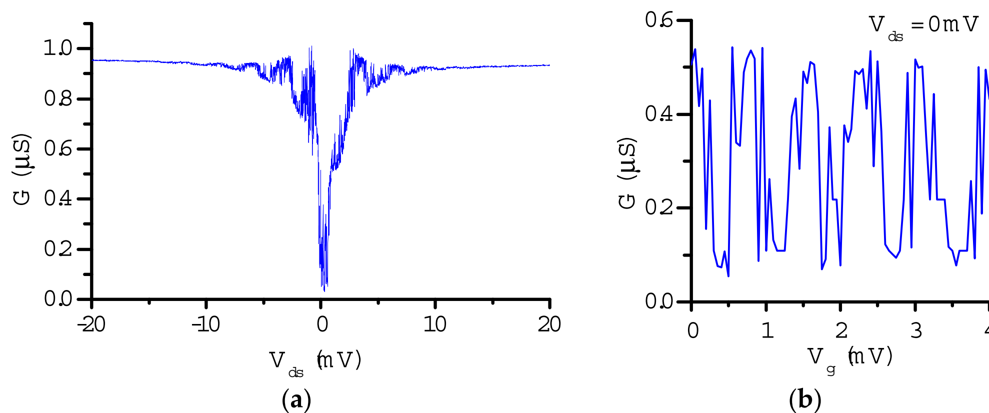

Figure 10. (**a**) Typical $G(V_{ds})$ dependence observed in samples fabricated with two FGA steps; T = 0.4 K. The metal is Ni and the barrier composition is six cycles of ALD SiO_2 (~0.7 nm) and four cycles of ALD Al_2O_3 (~0.4 nm) so the total barrier thickness is ~1.1 nm; (**b**) $G(V_g)$ dependence for the same SET, showing the excess switching noise.

Because of the detrimental effects on device performance associated with FGA, hydrogen plasma treatment has been investigated as an alternative way to reduce NiO [43,44]. This technique has the advantages of using a lower temperature and less time than FGA, and simultaneously passivating the defects residing in the tunnel barrier dielectric [45]. With plasma, various hydrogen species (H^+, H, H_2^-) capable of reacting with NiO are introduced into the process. The remote radio frequency hydrogen plasma (RHP) source in the chamber of the Oxford FlexAl PEALD reactor enables this in-situ treatment of the as-prepared dielectric film. To investigate this technique, following fabrication of the island and 12 cycles of PEALD SiO_2 (~1.1 nm), the sample was subjected to RHP (pressure of 10 mTorr, plasma power of 100 W at 300 °C) for 5 min, followed by definition of the source and drain electrodes using EBL as described above. The resulting average room temperature differential conductance (0.1 μS) was higher than any of the devices prepared with *two* FGA reduction steps and it had a broader distribution of conductance values within a batch. Despite larger conductance values at 300 K, at low temperature (<10 K) devices in which the ALD dielectric was exposed to RHP exhibit a monotonic increase of conductance with applied bias at $|V_{ds}| >> E_C/e$ and a conductance $G(V_{ds}$ = 0 mV) << $G_0/2$ significantly lower than expected at the peaks of CBOs (Figure 11a). Once again, this behavior is indicative of residual NiO at the interface of the oxide and top metal where thermal activation may become a limiting factor in conductance, as mentioned previously. Similar to the previously discussed devices (Figures 7b and 10b), a high level of RTS noise was also observed in CBO characteristics of these devices (Figure 11b).

To achieve a more complete reduction of residual NiO in the tunnel junctions, a second RHP treatment was performed on the completed devices for 5 min under identical conditions. This treatment increased the conductance further, from an average ~0.1 μS to ~3 μS at 300 K, the highest average conductance among all fabricated batches. We attribute this relatively high conductance, observed both before and after the final RHP treatment, to hydrogen-plasma induced thinning of the PEALD dielectric during the time when the uncovered tunnel barrier is subjected to the first RHP step [46]. At low temperature the majority of devices subjected to two consecutive RHP exhibit significantly improved SET characteristics (Figure 12a), most notably, with a very strong suppression of RTS noise at V_{ds} ~0, as compared to the single RHP treated devices in Figure 11, or FGA treated devices (Figures 7 and 10). However, in the peaks of the CBOs, the conductance still remains noticeably lower than expected (G << $G_0/2$) and the $G(V_{ds})$ characteristic still exhibits signs of non-linearity even at $|V_{ds}| >> E_C/e$ evidently due to incomplete reduction of NiO (Figure 12a).

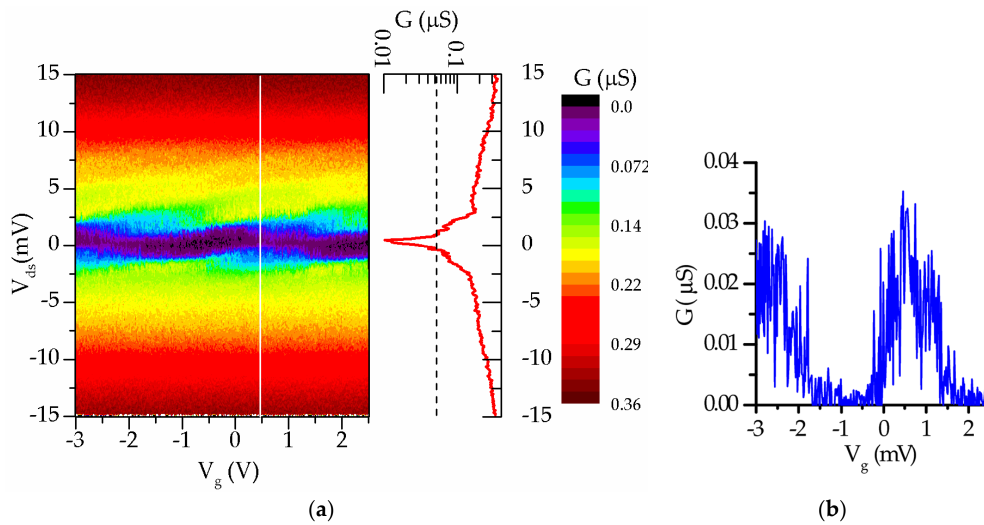

Figure 11. (**a**) Coulomb charging diagram of an Ni-SiO_2-Ni SET in which the ALD dielectric (~1 nm of SiO_2) was exposed to remote hydrogen plasma (RHP) (measured at T = 0.4 K) along with a $G(V_{ds})$ cross section (red curve) at a peak of CBO (V_g = 0.45 mV). Strong asymmetry, non-MIM SET conductance out of blockade region, as well as "switching noise" are visible. (**b**) CBOs of the same device.

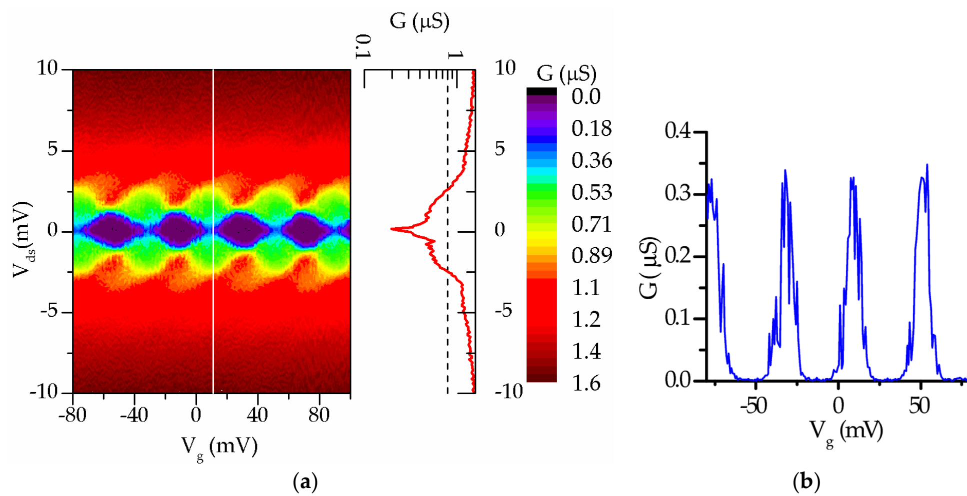

Figure 12. (**a**) Coulomb charging diagram and $G(V_{ds})$ cross section at V_g = 10 mV of a Ni-SiO_2-Ni device fabricated with two RHP steps (measured at T = 0.4 K). Barrier composition is 12 cycles (~1 nm) of SiO_2 by plasma-enhanced ALD (PEALD); (**b**) CBOs of the same device.

Furthermore, above a certain voltage threshold V_{Th} ~$5E_C/e$, a very large noise "floods" the measurement bandwidth to the point that it exceeds the ability of a lock-in amplifier to reject the incoherent signals (Figure 13a). The spectral density of this noise abruptly becomes about two orders of magnitude larger than that at low V_{ds} and it appears to be of Lorenzian shape, typical for RTS trap recombination noise [47]. However, unlike the RTS noise visible in in Figure 10a, this noise is only present outside of the Coulomb blockade region and has a distinctly different frequency cut off (several hundred Hz), suggesting that some other mechanism, other than trap-modulation of Coulomb blockade, is responsible for its appearance. For example, it may be caused by population/depopulation of relatively deep traps located about ~7.5 meV above the Fermi level in the remaining NiO layer.

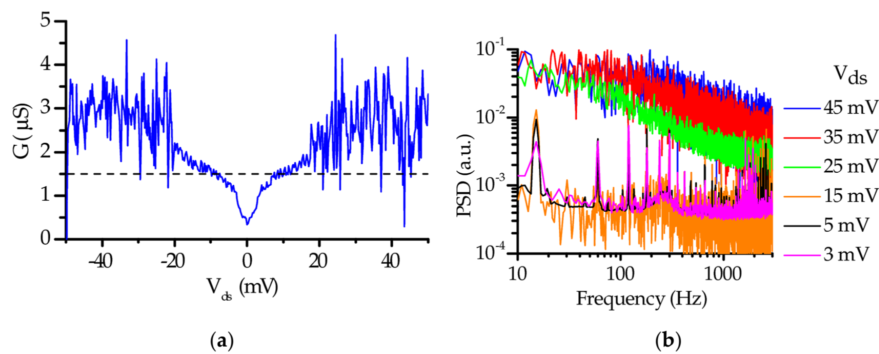

Figure 13. (**a**) $G(V_{ds})$ dependence observed in (Ni-SiO_2-Ni) SET fabricated with two RHP steps at a CBO peak. For V_{ds} above a threshold $V_{Th} \approx 15$ mV, very strong noise is observed, but below this threshold the switching noise is much lower than in double FGA samples. The peaks of CBOs never reach $G_0/2$ indicating that some NiO remains. (**b**) The spectral density of noise as a function of V_{ds} shows two orders of magnitude increase of noise above 15 mV (T = 0.4 K).

To summarize, we have demonstrated that two hydrogen-based treatments are required to achieve restoration of MIM characteristics of the junctions: by using two FGA or two RHP we achieved improvements in the device performance but both techniques have their limitations. The double FGA technique results in the appearance of large switching RTS noise and may lead to agglomeration, resulting in discontinuities, while the double RHP technique, though mitigating the RTS noise, leads to incomplete NiO reduction accompanied with thinning of the ALD dielectric layer.

3.2.3. Optimization of Ni-SiO_2-Ni Junction Fabrication

The optimization of Ni-based MIM SETs with SiO_2 PEALD dielectric was investigated using an approach that exploits the benefits and minimizes the weaknesses of both FGA and RHP treatments. We developed a process flow (referred to as FGA+RHP) where the first hydrogen-based treatment performed after barrier deposition is an FGA at 400 °C, because the main purpose of this step is to achieve complete reduction of the relatively thick parasitic NiO on the first Ni layer without damaging the SiO_2 barrier. At this stage of the fabrication, the byproduct of the process, H_2O, easily diffuses through a thin dielectric layer and is removed. For the second treatment, the primary goal is mainly to anneal defects in the PEALD SiO_2 dielectric with a secondary objective of reducing the NiO layer on the bottom of the upper electrodes.

For this purpose, we performed a study comparing double FGA with FGA+RHP treatments [48]. Using two dice originating from the same oxidized Si wafer, 50 nm-thick inlaid Ni islands are defined in the SiO_2 substrate using EBL, ICP, Ni evaporation, and CMP. Next, 12 layers of SiO_2 as the dielectric tunnel barrier are deposited by PEALD on one sample, and a stack of 10 SiO_2 + 2 Al_2O_3 is deposited on the second sample. Subsequently, the samples are subjected to a 10-s O_2 plasma ashing step to clear any residual carbon on the deposited tunnel barrier. Next, the samples are treated with a 25 min-FGA at 400 °C in 5% H_2–95% Ar. The source and drain leads are then defined in a second EBL, followed by an O_2 plasma de-scum, metal evaporation, and liftoff. After completion of the fabrication process, the devices were tested electrically at 300 K and they all exhibited very low conductance, averaging on the order of 100 pS, indicative of the additional NiO layer on the bottom of the source/drain electrodes [11]. At this stage, the dice are separated into two separate pieces for the final NiO reduction treatment: A1 and B1 with 12 layers of SiO_2, and A2 and B2 with a stack of 10 layers of SiO_2 + two layers of Al_2O_3. Overall, more than 400 devices were fabricated in these four pieces. The A1 and A2 pieces were then used as reference samples and subjected to a second FGA for 10 min at 375 °C. The samples B1 and B2 were subjected to RHP (with the same conditions as described in Section 3.2.2 of this report). The average conductance at 300 K in all samples after the second treatment increased by a factor of ~10^3.

Figure 14 shows the comparison of charging diagrams for devices fabricated using two FGA steps (batches A1 and A2, Figure 14a) vs. devices fabricated using FGA+RHP (batches B1 and B2, Figure 14b). Most importantly, all of the measured devices from batches B1 and B2 clearly show the disappearance of gate-independent excess noise typical of double-FGA devices from batches A1 and A2 (Figure 14a): diamonds are now clearly visible in Figure 14b. A comparison of $G(V_{ds})$ scans also shows the significant decrease in noise as can be seen in the two side-by-side $G(V_{ds})$ cross sections of Figure 14. It is quite clear that in the recipe that combines FGA treatment for the SiO_2-covered island with subsequent RHP treatment of the finished devices, a drastic reduction of switching RTS noise is obtained along with electric characteristics much closer to that expected for MIM junctions [48].

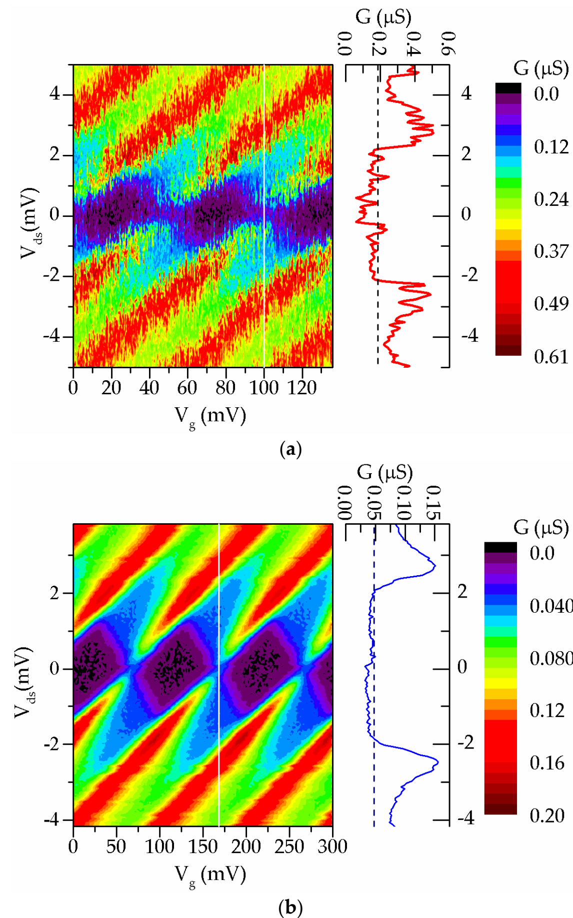

Figure 14. Comparison of electrical characteristics for Ni-SiO_2-Ni devices measured at 0.4 K: (**a**) Coulomb diamonds of a device from batch A1 treated with double FGA along with a $G(V_{ds})$ cross section at V_g = 100 mV; and (**b**) Coulomb diamonds of a device from batch B1 treated with FGA+RHP along with a $G(V_{ds})$ cross section at V_g = 170 mV. The difference of CBO periods results from different device proximities to electrostatic gates, and hence a different gate capacitance.

Let us now compare the obtained experimental results with the expected performance based on the dimensions of imaged SETs (Figure 2g). In the case of identical junctions and a gate capacitance much smaller than that of the junctions, $C_s = C_d >> C_g$, the absolute values of the slopes of the Coulomb diamonds (positive slope, $\alpha = C_g/(C_s + C_g)$, and negative slope $\beta = -C_g/C_d$) are expected to be nearly the same, and the highly asymmetric shape of the diamonds (e.g., Figures 7a and 11) thus indicates a variation in the thickness of the two tunnel junctions most likely due to non-uniformities in the barrier dielectric. Figure 15a shows experimentally obtained data from one FGA+RHP treated device with nearly identical slopes $|\alpha| \approx |\beta|$. Simulations performed based on an orthodox theory model [20] enable fairly accurate extraction of the junction parameters. While variations of junction capacitances

(~20%) and conductances (<50%) are fairly reasonable given potential variations in the thickness and junction areas, the absolute values of the capacitances appear to be significantly larger than expected from the parallel-plate model: $C_d \approx C_s = \varepsilon_0 \varepsilon A/d$ = 28–40 aF (ε = 3.9 for SiO_2, A = 900–1200 nm^2, and d = 1.17 nm, the nominal thickness of 13 cycles of PEALD SiO_2). A comparison of dimensions for devices fabricated using the cross-tie technique (Figure 1) and half-damascene process (Figure 2) shows a very significant narrowing of the island produced by the half-damascene technique. This is clearly beneficial because it lowers the junction capacitance and thus increases the charging energy. However, 3D simulations of the island total capacitance in half-damascene geometry show that the island capacitance can be more than double what would be expected from the parallel plate model due to fringing fields (Figure 16b). Thus the 3D capacitance simulation of Figure 16b (C_{Island} = 121 aF) provides a good match to the fitted simulation of Figure 15b ($C_{Island} = C_d + C_s + C_g$ = 110 aF) and shows that fringing fields cannot be ignored for very small junctions.

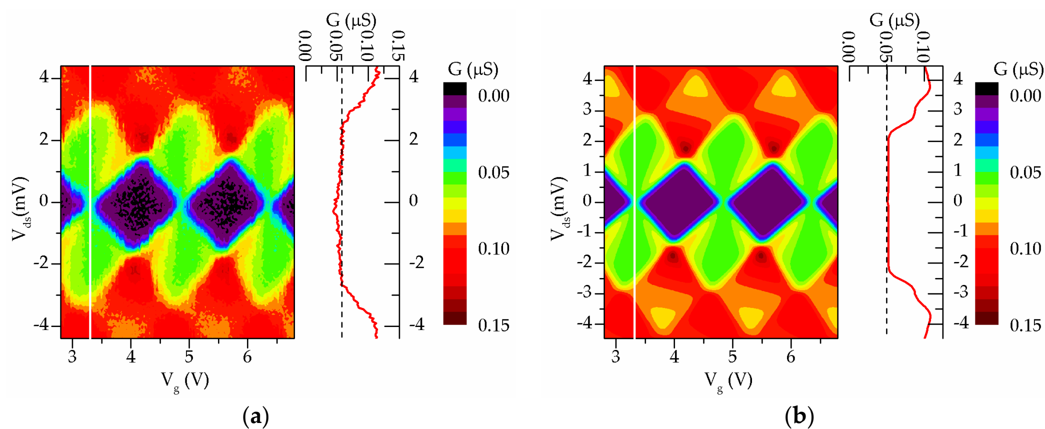

Figure 15. (**a**) Coulomb diamonds of a Ni-SiO_2-Ni device treated with FGA+RHP along with a $G(V_{ds})$ cross section at V_g = 3.3 V; and (**b**) simulations of an MIM SET along with a $G(V_{ds})$ cross section at V_g = 3.3 V using the following parameters: C_g = 0.106 aF, C_d = 47 aF, C_s = 63 aF, G_d = 0.35 μS, G_s = 0.50 μS, T = 0.5 K.

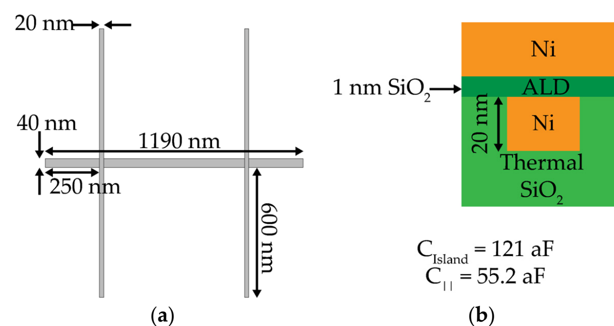

Figure 16. 3D simulation of the total island capacitance in a half-damascene geometry: (**a**) Dimensions of the island (horizontal grey line) and source and drain (vertical grey lines). The island is inlaid in thermal SiO_2 (ε = 3.9) and the source and drain are on top of the PEALD dielectric layer (ε = 3.9) surrounded by air (ε = 1); (**b**) Cross section of island inlaid in SiO_2 dielectric. The simulated total island capacitance C_{Island} is for 1 nm of PEALD SiO_2 (approximately the same thickness as 12 cycles of SiO_2, ε = 1). $C_{||}$ is the expected island capacitance using the parallel plate model of the two tunnel junctions for the given dimensions. Based on our simulations, the actual island capacitance can be more than twice the calculated value using the parallel plate approximation.

3.2.4. SET Devices with Ni-SiN_x-Ni Tunnel Junctions

As mentioned earlier, two approaches can be used to fix the problem of native metal oxides forming during the ALD process: chemically reducing the oxide (as described in the previous section) or using a dielectric that does not contain oxygen. The devices studied in this section used the latter approach and were prepared using the half-damascene process flow described above with PEALD of 21 cycles of SiN_x, to form a dielectric barrier (with approximate thickness of 1.05 nm). Bis(diethylamino)silane ($C_8H_{22}N_2Si$) and H_2 + N_2 plasma were the precursors used in the PEALD process in an Oxford FlexAL system. In contrast with previous sections, where oxygen-containing dielectrics were used (Al_2O_3 and SiO_2), no post-PEALD treatment was used in this process. An experimental diamond plot for a typical device is shown in Figure 17.

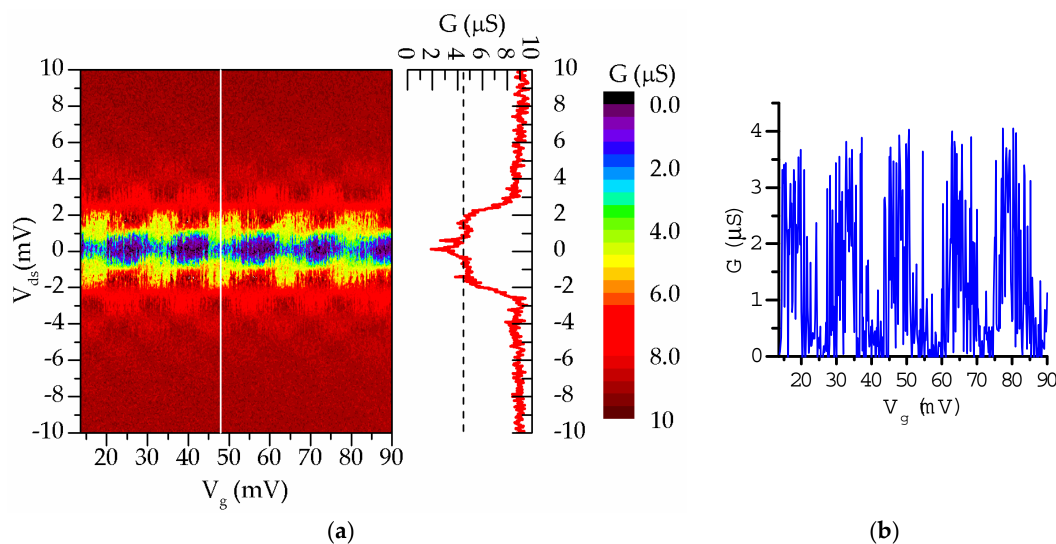

Figure 17. (**a**) Typical Coulomb diamond plot for a Ni-SiN_x-Ni SET with 21 cycles of SiN_x (~1 nm) along with a $G(V_{ds})$ cross section at V_g = 47 mV (a peak of CBOs); and (**b**) CBOs from the same device exhibiting RTS noise.

Reduction of the conductance at the CBO peak to nearly $G_0/2$ along with constant $G(V_{ds})$ ~G_0 when $|V_{ds}|$ >> $2E_c/e$ (Figure 17a) is indicative of negligible presence of thermally activated NiO in the junctions and confirms that the presence of the oxidizing pulse (O_2, O_3, or H_2O) in the ALD process is the main origin of the parasitic native oxide formation on the island. Moreover, since SiN_x is hydrophobic and does not contain oxygen, the oxidation of the top metal while being deposited on the SiN_x barrier is negligible. Experiments once again reveal a very large level of switching RTS noise similar to that observed for Pt-Al_2O_3-Pt and Ni-SiO_2-Ni devices described in the previous sections. The noise analysis performed in [49] pinpoints the location of the traps within the junctions (either in the dielectric or at the metal-dielectric interfaces). Silicon nitride is known as a trap-rich material where the abundance of traps is generally associated with silicon atoms replacing nitrogen atoms, resulting in silicon dangling bonds, referred to as *K*-center defects [50]. Other defects can be associated with hydrogen, which is typically present in the SiN_x matrix [51].

4. Conclusions

In this work SETs have been fabricated using thermal ALD and plasma enhanced-ALD to deposit tunnel barriers of Al_2O_3, SiO_2, combinations of the two, and SiN_x. Table 1 provides a summary of the different metals, dielectrics, and treatments and the most important observations relating to each. This demonstrates the ability of ALD to controllably deposit a variety of films on metal substrates including Ni and Pt. The two major interrelated issues with this technique have been: (1) oxidation of

the metal leads during ALD; and (2) the formation of traps near the island, most likely in the barrier dielectric or at the metal-dielectric interfaces that lead to strong RTS-type electrical noise. In the case of Ni-SiO_2-Ni SETs, it has been shown that both issues can be mitigated by a combination of forming gas annealing during fabrication and hydrogen plasma treatment after fabrication. Here post-fabrication RHP treatment appeared the most important factor in noise mitigation, potentially due to annealing of charged defects in SiO_2 dielectric. Likewise, due to the instability of platinum oxide, ridding platinum-based devices of their native oxide has proven possible using argon anneal, however these devices also exhibited time instabilities caused potentially by reoxidation of Pt at Pt/Al_2O_3 interfaces. In addition, the choice of SiN_x as the tunnel barrier seems to avoid parasitic oxide formation in the tunnel junctions so that no in-fabrication or post-fabrication is needed to restore the MIM behavior in the SETs, but lowering the electrical noise has proved to be more elusive. Further research is needed to determine the source of the traps and to investigate how post-fabrication hydrogen plasma is effective in passivating these traps, and what species cause the oxidation of the metal layer deposited on top of the ALD oxide. Future work will also explore amorphous metal thin films [52] (unlike the polycrystalline films used in this work) and the effects of surface morphology on barrier uniformity.

Table 1. Summary of SET fabrication processes, treatments, and observations. Post-fab indicates a treatment after fabrication and post-ALD indicates a treatment after the respective ALD process.

Fabrication Process	Source/ Drain Metal	Island Metal	Dielectric	Cycles (nm)	Treatment	Observations
Cross-tie	Pt	Pt	ALD Al_2O_3 (H_2O-based)	9 (~1 nm)	none	Non-MIM behavior, long-term instability
Cross-tie	Pt	Pt	ALD Al_2O_3 (H_2O-based)	9 (~1 nm)	Post-fab: 5 min, Ar 375 °C	All shorts
Cross-tie	Pt	Pt	ALD Al_2O_3 (O_3-based)	9 (~1 nm)	none	Highly resistive
Cross-tie	Pt	Pt	ALD Al_2O_3 (O_3-based)	9 (~1 nm)	Post-fab: 5 min, Ar 375 °C	Stable but noisy
Cross-tie	Pt	Pt	PEALD SiO_2	15 (~1.5 nm)	none	All shorts
Cross-tie	Ni	Ni	PEALD SiO_2	2 (~0.2 nm)	none	Low conductance, non-MIM behavior
Cross-tie	Ni	Ni	PEALD SiO_2	2 (~0.2 nm)	Post-ALD: 2 min, 5% H_2 in Ar 400 °C	Evidence of "pinholes"
Cross-tie/ Half-Damascene	Ni	Ni	PEALD SiO_3	12 (~1.1 nm)	Post-ALD: (FGA) 30 min, 5% H_3 in Ar 400 °C Post-Fab: (FGA) 10 min, 5% H_2 in Ar 300 °C	Effectiveness limited by agglomeration and noisy
Cross-tie/ Half-Damascene	Ni	Ni	PEALD SiO_2	12 (~1.1 nm)	Post-ALD: (RHP) 5 min, H_2 plasma 100W 300 °C	Non-MIM behavior, noisy
Cross-tie/ Half-Damascene	Ni	Ni	PEALD SiO_2	12 (~1.1 nm)	Post-ALD: RHP Post-Fab: RHP	Highest conductance, non-MIM behavior, noisy when V_{ds} > 15 mV
Cross-tie/ Half-Damascene	Ni	Ni	PEALD SiO_2	12 (~1.1 nm)	Post-ALD: FGA Post-Fab: RHP	Best Performance
Half-Damascene	Ni	Ni	PEALD SiN_x	21 (~1 nm)	none	Noisy, but no evidence of NiO

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References

1. Fulton, T.A.; Dolan, G.J. Observation of single-electron charging effects in small tunnel junctions. *Phys. Rev. Lett.* **1987**, *59*, 109–112. [CrossRef] [PubMed]
2. Kuzmin, L.S.; Pashkin, Y.A.; Tavkhelidze, A.N.; Ahlers, F.J.; Weimann, T.; Quenter, D.; Niemeyer, J. An all-chromium single electron transistor: A possible new element of single electronics. *Appl. Phys. Lett.* **1996**, *68*, 2902–2904. [CrossRef]
3. Scherer, H.; Weimann, T.; Hinze, P.; Samwer, B.W.; Zorin, A.B.; Niemeyer, J. Characterization of all-chromium tunnel junctions and single-electron tunneling devices fabricated by direct-writing multilayer technique. *J. Appl. Phys.* **1999**, *86*, 6956–6964. [CrossRef]
4. Sillanpää, M.A.; Hakonen, P.J. Titanium single-electron transistor fabricated by electron-beam lithography. *Phys. E Low Dimens. Syst. Nanostruct.* **2002**, *15*, 41–47. [CrossRef]
5. Hobbs, P.C.D.; Laibowitz, R.B.; Libsch, F.R. Ni–NiO–Ni tunnel junctions for terahertz and infrared detection. *Appl. Opt.* **2005**, *44*, 6813–6822. [CrossRef] [PubMed]
6. Zorin, A.B.; Ahlers, F.J.; Niemeyer, J.; Weimann, T. Background charge noise in metallic single-electron tunneling devices. *Phys. Rev. B* **1996**, *53*, 13682–13687. [CrossRef]
7. Pashkin, Y.A.; Nakamura, Y.; Tsai, J.S. Room-temperature Al single-electron transistor made by electron-beam lithography. *Appl. Phys. Lett.* **2000**, *76*, 2256–2258. [CrossRef]
8. Zimmerman, N.M.; Huber, W.H.; Simonds, B.; Hourdakis, E.; Fujiwara, A.; Ono, Y.; Takahashi, Y.; Inokawa, H.; Furlan, M.; Keller, M.W. Why the long-term charge offset drift in Si single-electron tunneling transistors is much smaller (better) than in metal-based ones: Two-level fluctuator stability. *J. Appl. Phys.* **2008**, *104*, 033710. [CrossRef]
9. Rippard, W.H.; Perrella, A.C.; Albert, F.J.; Buhrman, R.A. Ultrathin aluminum oxide tunnel barriers. *Phys. Rev. Lett.* **2002**, *88*, 046805. [CrossRef] [PubMed]
10. Likharev, K.K. Single-electron devices and their applications. *Proc. IEEE* **1999**, *87*, 606–632. [CrossRef]
11. Karbasian, G.; McConnell, M.S.; Orlov, A.O.; Rouvimov, S.; Snider, G.L. Experimental demonstration of single electron transistors featuring SiO_2 plasma-enhanced atomic layer deposition in Ni-SiO_2-Ni tunnel junctions. *J. Vac. Sci. Technol. A* **2016**, *34*, 01A122. [CrossRef]
12. Karbasian, G.; Fay, P.J.; Xing, H.; Jena, D.; Orlov, A.O.; Snider, G.L. High aspect ratio features in poly(methylglutarimide) using electron beam lithography and solvent developers. *J. Vac. Sci. Technol. B* **2012**, *30*, 06FI01. [CrossRef]
13. Karbasian, G.; Orlov, A.O.; Snider, G.L. Fabrication of nanodamascene metallic single electron transistors with atomic layer deposition of tunnel barrier. *J. Vac. Sci. Technol. B* **2015**, *33*, 06FG02. [CrossRef]
14. McConnell, M.S.; Schneider, L.C.; Karbasian, G.; Rouvimov, S.; Orlov, A.O.; Snider, G.L. Atomic layer deposition of Al_2O_3 for single electron transistors utilizing Pt oxidation and reduction. *J. Vac. Sci. Technol. A* **2016**, *34*, 01A139. [CrossRef]
15. George, H.C.; Orlov, A.O.; Snider, G.L. Platinum single-electron transistors with tunnel barriers made by atomic layer deposition. *J. Vac. Sci. Technol. B* **2010**, *28*, C6L6–C6L8. [CrossRef]
16. Kulik, I.O.; Shekhter, R.I. Kinetic phenomena and charge discreteness effects in granulated media. *Zhur. Eksp. Teor. Fiz.* **1975**, *68*, 623–640.
17. Beenakker, C.W.J. Theory of Coulomb-blockade oscillations in the conductance of a quantum dot. *Phys. Rev. B* **1991**, *44*, 1646–1656. [CrossRef]
18. Zhou, Y.; Yin, J.; Xu, H.; Xia, Y.; Liu, Z.; Li, A.; Gong, Y.; Pu, L.; Yan, F.; Shi, Y. A $TiAl_2O_5$ nanocrystal charge trap memory device. *Appl. Phys. Let.* **2010**, *97*, 143504. [CrossRef]
19. Song, X. Fundamental Studies of Titania-Based High Dielectric Constant Materials. Ph.D. Thesis, University of Illinois at Chicago, Ann Arbor, MI, USA, 2007.
20. Pierre, M.; Hofheinz, M.; Jehl, X.; Sanquer, M.; Molas, G.; Vinet, M.; Deleonibus, S. Background charges and quantum effects in quantum dots transport spectroscopy. *Eur. Phys. J. B* **2009**, *70*, 475–481. [CrossRef]
21. Groner, M.D.; Elam, J.W.; Fabreguette, F.H.; George, S.M. Electrical characterization of thin Al_2O_3 films grown by atomic layer deposition on silicon and various metal substrates. *Thin Solid Films* **2002**, *413*, 186–197. [CrossRef]
22. Schneider, L.C. Fabrication of Single Electron Transistors Using Atomic Layer Deposition. Master's Thesis, University of Notre Dame, Notre Dame, IN, USA, 2014.

23. Wilk, G.D.; Muller, D.A. Correlation of annealing effects on local electronic structure and macroscopic electrical properties for HfO_2 deposited by atomic layer deposition. *Appl. Phys. Let.* **2003**, *83*, 3984–3986. [CrossRef]
24. Fernandez, M.P.H.; Chamberland, B.L. A new high-pressure form of PtO_2. *J. Less Common Met.* **1984**, *99*, 99–105. [CrossRef]
25. Friebel, D.; Miller, D.J.; O'Grady, C.P.; Anniyev, T.; Bargar, J.; Bergmann, U.; Ogasawara, H.; Wikfeldt, K.T.; Pettersson, L.G.M.; Nilsson, A. In situ X-ray probing reveals fingerprints of surface platinum oxide. *Phys. Chem. Chem. Phys.* **2011**, *13*, 262–266. [CrossRef] [PubMed]
26. Roschier, L.; Hakonen, P.; Bladh, K.; Delsing, P.; Lehnert, K.W.; Spietz, L.; Schoelkopf, R.J. Noise performance of the radio-frequency single-electron transistor. *J. Appl. Phys.* **2004**, *95*, 1274–1286. [CrossRef]
27. Kano, S.; Azuma, Y.; Tanaka, D.; Sakamoto, M.; Teranishi, T.; Smith, L.W.; Smith, C.G.; Majima, Y. Random telegraph signals by alkanethiol-protected Au nanoparticles in chemically assembled single-electron transistors. *J. Appl. Phys.* **2013**, *114*, 223717. [CrossRef]
28. Xiangning, L.; Tomcsanyi, M.; Orlov, A.O.; Kosel, T.H.; Snider, G.L. Strong cotunneling suppression in a single-electron transistor with granulated metal film island. *Appl. Phys. Let.* **2006**, *89*, 43511.
29. Beloborodov, I.S.; Lopatin, A.V.; Vinokur, V.M.; Efetov, K.B. Granular electronic systems. *Rev. Mod. Phys.* **2007**, *79*, 469. [CrossRef]
30. Kolkovsky, V.; Stübner, R.; Langa, S.; Wende, U.; Kaiser, B.; Conrad, H.; Schenk, H. Influence of annealing in H atmosphere on the electrical properties of Al_2O_3 layers grown on p-type Si by the atomic layer deposition technique. *Solid State Electron.* **2016**, *123*, 89–95. [CrossRef]
31. Simmons, J.G. Generalized formula for electric tunnel effect between similar electrodes separated by a thin insulating film. *J. Appl. Phys.* **1963**, *34*, 1793–1803. [CrossRef]
32. Kessels, E.; Potts, S.H.P.; van de Sanden, R. Plasma Atomic Layer Deposition. In *Atomic Layer Deposition of Nanostructured Materials*; Nicola Pinna, M.K., Ed.; Wiley: Weinheim, Germany, 2011; pp. 131–157.
33. Knechten, C.A.M. *Plasma Oxidation for Magnetic Tunnel Junctions*; Eindhoven University of Technology: Eindhoven, The Netherlands, 2005.
34. Foroughi Abari, A. Atomic Layer Deposition of Metal Oxide Thin Films on Metallic Substrates. Ph.D. Thesis, University of Alberta, Alberta, AB, Canada, 2012.
35. Faes, A.; Jeangros, Q.; Wagner, J.B.; Hansen, T.W.; Van Herle, J.; Brisse, A.; Dunin-Borkowski, R.; Hessler-Wyser, A. In situ Reduction and Oxidation of Nickel from Solid Oxide Fuel Cells in a Transmission Electron Microscope. *ECS Trans. (Electrochem. Soc.)* **2009**, *25*, 1985–1992.
36. Lee, J.-S.; Kim, B.-S. Synthesis and Related Kinetics of Nanocrystalline Ni by Hydrogen Reduction of NiO. *Mater. Trans.* **2001**, *42*, 1607–1612. [CrossRef]
37. Utigard, T.A.; Wu, M.; Plascencia, G.; Marin, T. Reduction kinetics of Goro nickel oxide using hydrogen. *Chem. Eng. Sci.* **2005**, *60*, 2061–2068. [CrossRef]
38. Mani, S.; Saif, T.; Han, J.H. Effect of annealing on the conductivity of electroless deposited Ni nanowires and films. *IEEE Trans. Nanotechnol.* **2006**, *5*, 138–141. [CrossRef]
39. Grigoras, K.; Franssila, S.; Airaksinen, V.M. Investigation of sub-nm ALD aluminum oxide films by plasma assisted etch-through. *Thin Solid Films* **2008**, *516*, 5551–5556. [CrossRef]
40. Pauleau, Y. Interconnect Materials. In *Microelectronic Materials and Processes*; Levy, R.A., Ed.; Springer: Dordrecht, The Netherlands, 1989; pp. 635–678.
41. Nagao, K.; Neaton, J.B.; Ashcroft, N.W. First-principles study of adhesion at Cu/SiO_2 interfaces. *Phys. Rev. B* **2003**, *68*, 125403. [CrossRef]
42. Srolovitz, D.J.; Safran, S.A. Capillary instabilities in thin films. II. Kinetics. *J. Appl. Phys.* **1986**, *60*, 255–260. [CrossRef]
43. Tu, X.; Gallon, H.J.; Whitehead, J.C. Plasma-assisted reduction of a NiO/Al_2O_3 catalyst in atmospheric pressure H_2/Ar dielectric barrier discharge. *Catal. Today* **2013**, *211*, 120–125. [CrossRef]
44. Zhang, X.; Sun, W.-J.; Chu, W. Effect of glow discharge plasma treatment on the performance of Ni/SiO_2 catalyst in CO_2 methanation. *J. Fuel Chem. Technol.* **2013**, *41*, 96–101. [CrossRef]
45. Nazarov, A.; Lysenko, V.; Nazarova, T. Hydrogen plasma treatment of silicon thin-film structures and nanostructured layers. *Semicond. Phys. Quantum Electron. Optoelectron.* **2008**, *11*, 101–123.
46. Peña, O.; Muhl, S.; López, W.; Rodríguez-Fernández, L.; Ruvalcaba-Sil, J.L. Hydrogen plasma etching of silicon dioxide in a hollow cathode system. *Thin Solid Films* **2010**, *518*, 3156–3159. [CrossRef]

47. Machlup, S. Noise in semiconductors: Spectrum of two-parameter random signal. *J. Appl. Phys.* **1954**, *25*, 341–343. [CrossRef]
48. Karbasian, G. Fabrication of metallic single electron transistors featuring plasma enhanced atomic layer deposition of tunnel barriers. Ph.D. Thesis, University of Notre Dame, Ann Arbor, MI, USA, 2015.
49. Karbasian, G.; Orlov, A.O.; Mukasyan, A.S.; Snider, G.L. Single-Electron Transistors Featuring Silicon Nitride Tunnel Barriers Prepared by Atomic Layer Deposition. In Proceedings of the 2nd Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, EUROSOI-ULIS 2016, Vienna, Austria, 25–27 January 2016; Institute of Electrical and Electronics Engineers Inc.: Vienna, Austria, 2016; pp. 32–35.
50. Vianello, E.; Driussi, F.; Blaise, P.; Palestri, P.; Esseni, D.; Perniola, L.; Molas, G.; De Salvo, B.; Selmi, L. Explanation of the Charge Trapping Properties of Silicon Nitride Storage Layers for NVMs-Part II: Atomistic and Electrical Modeling. *IEEE Trans. Electron. Dev.* **2011**, *58*, 2490–2499. [CrossRef]
51. Sonoda, K.; Tsukuda, E.; Tanizawa, M.; Yamaguchi, Y. Electron trap level of hydrogen incorporated nitrogen vacancies in silicon nitride. *J. Appl. Phys.* **2015**, *117*, 104501. [CrossRef]
52. Cowell, E.W.; Alimardani, N.; Knutson, C.C.; Conley, J.F.; Keszler, D.A.; Gibbons, B.J.; Wager, J.F. Advancing MIM electronics: Amorphous metal electrodes. *Adv. Mater.* **2011**, *23*, 74–78. [CrossRef] [PubMed]

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