Strained Silicon Single Nanowire Gate-All-Around TFETs with Optimized Tunneling Junctions

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Abstract: In this work, we demonstrate a strained Si single nanowire tunnel field effect transistor (TFET) with gate-all-around (GAA) structure yielding I_{on}-current of 15 µA/µm at the supply voltage of V_{dd} = 0.5V with linear onset at low drain voltages. The subthreshold swing (SS) at room temperature shows an average of 76 mV/dec over 4 orders of drain current I_d from 5×10^{-6} to 5×10^{-2} µA/µm. Optimized devices also show excellent current saturation, an important feature for analog performance.

Keywords: tunnel field effect transistor (TFET); band-to-band tunneling (BTBT); trap-assisted tunneling (TAT); gate-all-around (GAA) nanowires (NWs)

1. Introduction

Scaling of complementary metal oxide semiconductor (CMOS) technology has brought about significant improvements in terms of power dissipation, device density, switching frequency, and costs reductions. Continued reduction of device dimensions into the nanometers range faces major issues with the high leakage current, unscalability of supply voltage V_{dd}, and lowered I_{on}/I_{off} switching ratio. The main constraint of metal-oxide-semiconductor field-effect transistor (MOSFET) for addressing these issues is the inverse subthreshold swing SS ($=dV_g/dlog(I_d)$), which is limited to 60 mV/dec at room temperature. Therefore, any attempt to scale V_{dd} by adjusting threshold voltage V_{th} will lead to exponentially higher I_{off}-current, deteriorating the switching ratio. To enable further V_{dd} scaling, steep slope device concepts (SS < 60 mV/dec) are required. The tunnel field effect transistor (TFET) is a promising alternative following the experimental demonstration of its sub-60 mV/dec swing [1]. TFET relies on quantum band-to-band tunneling (BTBT) to inject carriers from the source to the channel while cutting off the high-energy tail of the Fermi distribution, essentially having a similar effect to cooling down the distribution. Various research studies have demonstrated TFETs with SS < 60 mV/dec based on different materials like Si [2], Ge [3], SiGe [4], and III-V [5]. In comparison to the other materials, silicon-based TFETs generally show better performance in terms of minimum SS and switching ratio, mainly due to the maturity of silicon fabrication technology. Moreover, silicon TFETs are compatible with the conventional CMOS fabrication process, which keeps the costs low and makes it feasible to realize complementary TFET circuits [6,7].

By employing innovative materials, like high-k oxide and thin strained silicon, and highly scaled device structures, like nanowires (NWs), silicon TFETs have achieved promising results for both n- and p-type devices [8]. It is worth noting that these devices were based on an array of nanowires. The final results reflect the average behavior of all the NWs, dismissing the variations of each individual NW in

the array. This stems from the fact that the tunneling probability at the source of TFETs has exponential dependence on process-related parameters, such as nanowire shape and doping profile. By means of simulation, C.-J. Chen et al [9] have shown that TFETs are more susceptible to process variations than MOSFETs. Consequently, a single NW is superior for optimization of TFETs. In this work, we seek to fabricate gate-all-around (GAA) TFETs based on a single NW with a top-down approach to optimize the key fabrication processes, namely ion implantation and dopant activation, thus enabling us to draw specific conclusions at each step to further improve the I_{on}-current and average SS.

2. Device Fabrication

Single nanowire GAA TFETs were fabricated on strained silicon-on-insulator (sSOI) wafers with 15 nm biaxially strained silicon ($\varepsilon_{biax,tensile}$ = 0.8%) and 145 nm buried oxide (BOX). Strained silicon, due to its lower effective mass m^* and lower bandgap E_g, can achieve better tunneling current [10]. Figure 1 shows the process steps as well as schematics of the final device structure. The single NW was fabricated by a top-down process including e-beam lithography, subsequent reactive ion etching (RIE), and HF dip to suspend the nanowire. The final NW cross-section dimensions are 35 nm × 10 nm. After cleaning the substrate using RCA procedure, 3 nm HfO_2 by atomic layer deposition (ALD) and 60 nm TiN using atomic vapor deposition (AVD) were deposited as the high-k/metal gate stack. Then it was patterned using e-beam lithography and etched back by dry and wet etching. A very thin layer of 1.7 nm Ni was deposited by physical vapor deposition (PVD) to form a high quality $NiSi_2$ layer at the source and drain by annealing the substrate at 550 °C in forming gas for 30 s. The unreacted Ni residuals were selectively removed in a mixture of $H_2O:H_2SO_4$. Ni silicide formed by this method yields good gate alignment without encroachment of silicide in the channel region [11]. Implantation was carried out into the silicide using boron and phosphorous ions with various energies and tilt angles. For each step of the ion implantation, the other side of the device was protected by polymethyl methacrylate (PMMA) photoresist in order to form p^+ and n^+ junctions. After implantations, the dopants were activated at various temperatures in N_2 environment, as will be discussed in the next section. Finally, the substrate was passivated by SiO_2 and final Al contacts were formed. Figure 2 shows a side view scanning electron microscope (SEM) image of the finished structure, where the gate completely wraps around the nanowire, leading to improved electrostatic control.
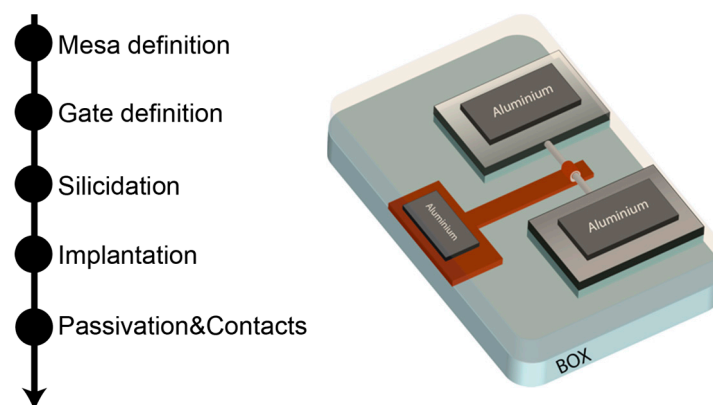

Figure 1. Fabrication process steps as well as schematics of the final device structure of the single nanowire (NW) tunnel field effect transistors (TFETs).
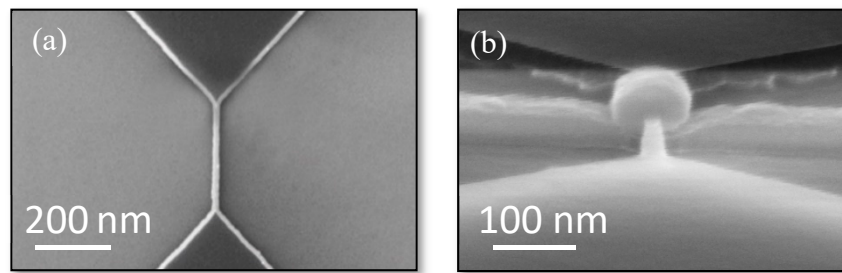
Figure 2. (**a**) Top view of a scanning electron microscope (SEM) image of a suspended silicon NW before gate fabrication process. (**b**) Side view of the final single NW TFET. It is clear that the gate metal completely wraps around the NW creating a gate-all-around (GAA) structure. The NW cross-section amounts to 35 nm × 10 nm.

3. Device Characteristics

In this part, we will evaluate the effect of implantation and fabrication parameters on the optimized performance of TFETs for high I_{on} current and minimum average SS. The first set of devices (Set 1) were implanted with P^+ ions to a dose of 1×10^{15} cm^{-2} at an energy of 3 keV and B^+ ions to a dose of 5×10^{14} cm^{-2} at 1.5 keV both at 45° tilt. The reason for a lower B^+ dose is to suppress the n-branch of the ambipolar behavior. Samples were activated at two different temperatures of 500 °C and 600 °C for 20 s. Figure 3a depicts the measured transfer characteristics I_d-V_{gs} of the device for a p-TFET. As evident from the figure, the TFET activated at the higher temperature shows degraded SS and lower I_{on} current compared to the device activated at 500 °C. This is due to the fact that the higher temperature annealing causes more extended diffusion of dopants, hence decreasing the steepness of the tunneling junction. Figure 3b shows the output I_d-V_{ds} characteristics for devices at $V_{ov} = -1$ V, which is defined as $V_{ov} = V_{gs} - V_{off} = -1$ V for an $I_{off} = 1$ nA/um. The typical super-linear onset of drain current I_d at small V_{ds} is present in the I_d-V_{ds} curves. The super-linear onset stems from drain-induced barrier thinning (DIBT) [12], which can be mitigated by increasing the dopant concentration at the tunneling junction [13]. In other words, for both temperature cases the dopant concentration at the source is lower than the optimum value and needs to be further increased.
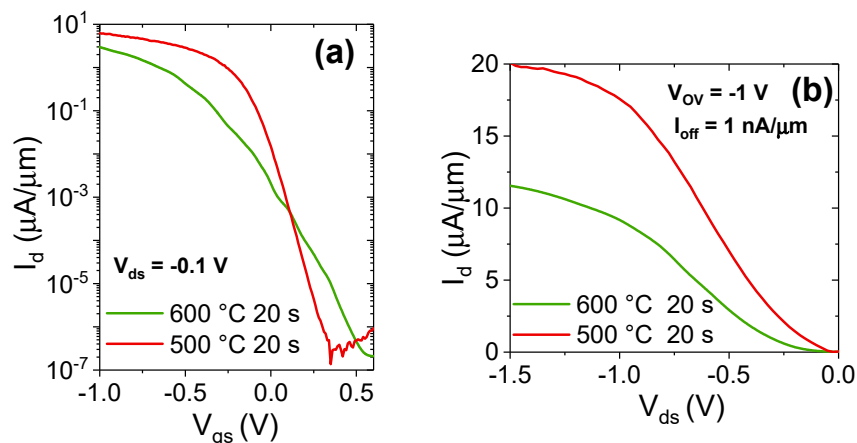

Figure 3. Measurement results of Set 1 devices. (**a**) I_d-V_g transfer characteristics for p-TFETs annealed at two different activation temperatures. (**b**) I_d-V_{ds} output characteristics for the corresponding devices, showing the super-linear onset of the I_d-V_{ds} curves.

To optimize the device performance, another set of TFETs (Set 2) were fabricated with different implantation and activation parameters. P ions with a dose 5×10^{15} cm^{-2} and at an energy of 3 keV

and B ions with a dose of 1×10^{15} cm^{-2} at 1.5 keV were implanted at a tilt of $+/-$ 45°, respectively. The implantation doses were increased to provide enough dopant concentration at the junctions after activation. The annealing was carried out at 550 °C for 10 s to drive out the dopants to the silicide/channel interface for dopant segregation. The annealing time and temperature were decreased in order to achieve sharper junctions. Figure 4a,b shows the measured transfer characteristics I_d-V_{gs} for the Set 2 devices of both p- and n-TFETs, respectively. A TFET works in both modes, p- and n-type, due to the presence of tunneling junctions at both the source and drain side, which causes undesired ambipolar switching, a typical behavior of a TFET. Moreover, the p-TFET shows higher on current I_{on} than n-TFET, corresponding to an I_{on} of 2.41 µA/µm for p-TFET and 0.78 µA/µm for n-TFET respectively, at $V_{ds} = V_{on} = V_g - V_{off} = -0.5$ V for an $I_{off} = 1$ nA/µm. The reason that n-TFETs show lower current could be due to the broader tunneling junction caused by faster B diffusion. For further analysis, Figure 4c,d shows the corresponding output characteristics I_d-V_{ds} for p- and n-TFET. The p-TFET shows very good current saturation and more importantly a linear onset. On the other hand, the n-TFET still shows a super-linear onset. Due to the higher diffusion coefficient of boron in silicon in comparison to phosphorus, annealing at 550 °C for 10 s is still not optimal for n-TFETs.
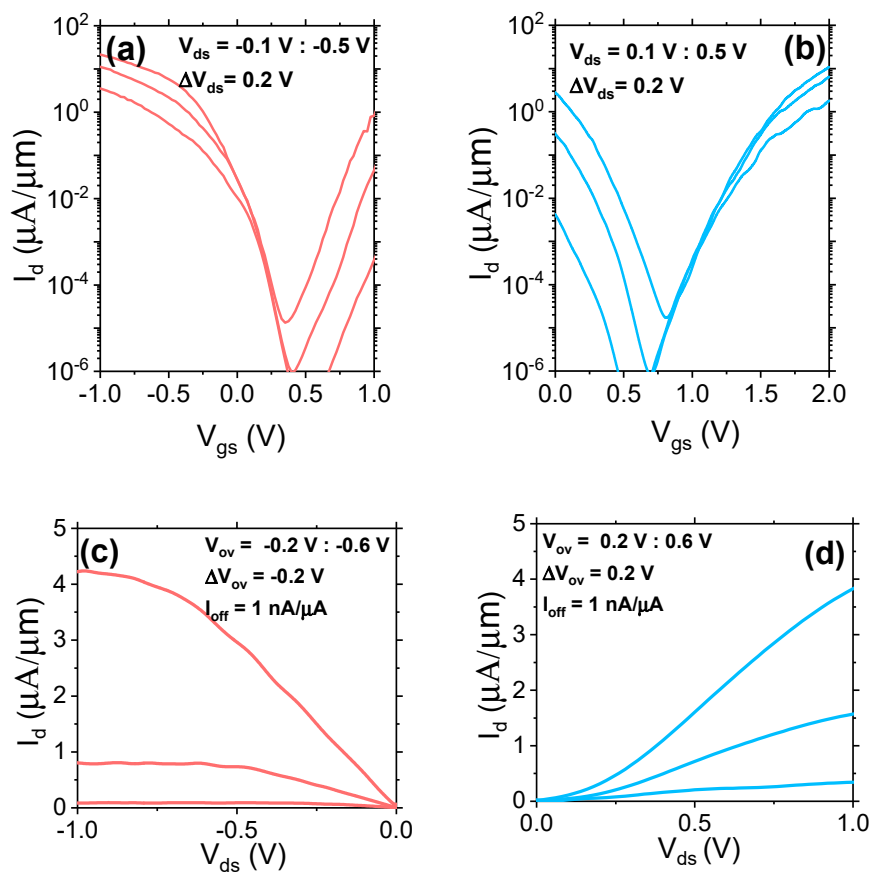

Figure 4. Measurement results of Set 2 devices: transfer characteristics I_d-V_g for p-TFET (**a**), and n-TFET (**b**); Output characteristics I_d-V_{ds} for the corresponding devices (**c,d**). The p-TFET device shows a linear onset, indicating higher concentration of the n$^+$/channel junction.

Thus, Set 3 of TFETs was fabricated with the aim to optimize the super-linear onset of n-TFET. In this case, 1×10^{15} cm^{-2} P$^+$ ions at 3 keV and 1×10^{15} cm^{-2} B$^+$ ions at 0.8 keV both without tilt (in normal direction) were implanted for source and drain, respectively. The dopants were activated at 500 °C for 10 s. This combination of implantation tilt, energy, and activation were chosen to achieve steeper boron junctions. Figure 5a,b shows the transfer and output characteristics of the

n-TFET device. The output characteristics show very good linear behavior by increasing V_{ds} as well as excellent current saturation. The latter is a key performance parameter for analog applications, for example, a current mirror. Moreover, the on current was also improved compared to the Set 2 devices, showing $I_{on} = 15\ \mu A/\mu m$ at $V_{ov} = V_{gs} - V_{off} = 0.5\ V$ with an $I_{off} = 1\ nA/\mu m$. The average SS was also improved to 76 mV/dec over 4 orders of drain current I_d. The minimum SS is still above 60 mV/dec, which could be attributed to the undesired effect of trap-assisted tunneling (TAT) caused by interface traps [14,15]. Figure 5c presents the I_d-V_{gs} characteristics for the p-i-n diode forward biased with various V_d, as illustrated in the inset. The curves show typical forward p-i-n diode behavior—much higher currents than TFET and the current decreases with decreasing absolute V_d. This also provides evidence of the TFET operations for the results shown in Figure 5a,b. Table 1 summarizes the fabrication parameters and the device performance.
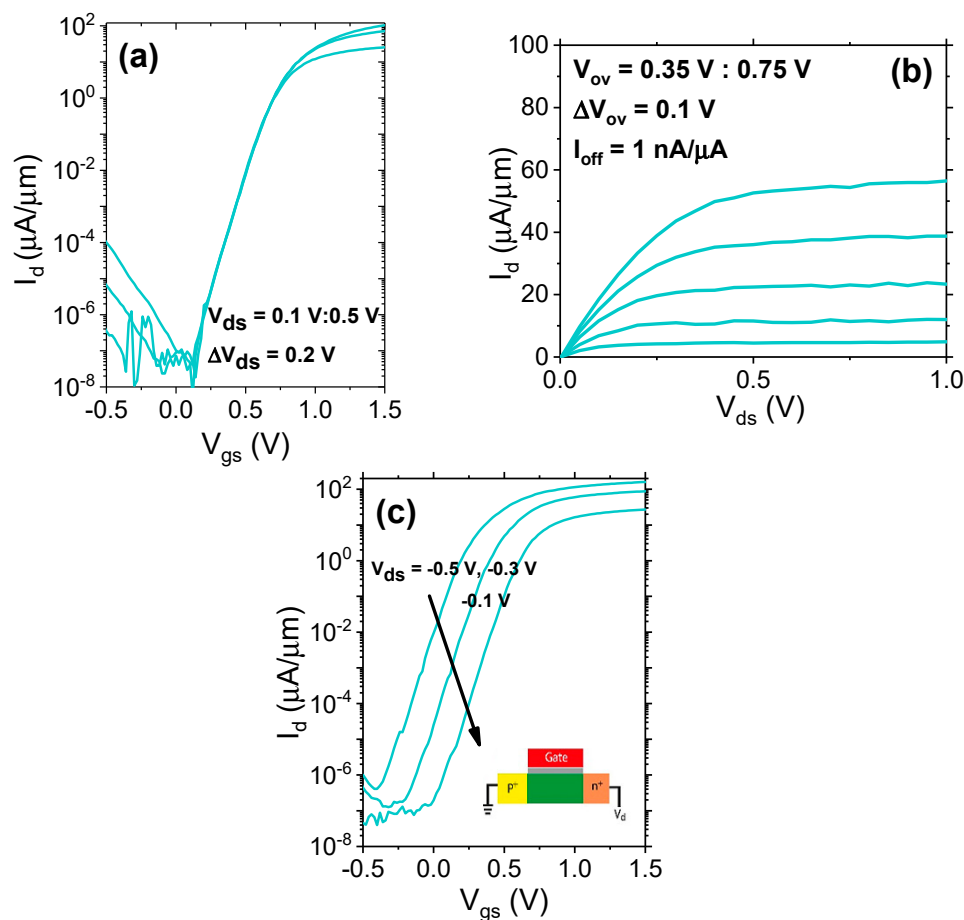

Figure 5. Measurement results of Set 3 devices: (**a**) Transfer characteristics I_d-V_g of the optimized n-TFET, (**b**) corresponding output characteristics I_d-V_{ds} of the fabricated device showing good saturation and linear onset. The device shows very high on-currents of 15 μA/μm at $V_{dd} = 0.5\ V$. (**c**) Forward biased I_d-V_{gs} characteristics of the p-i-n diode, showing typical forward I-V curves for the diode.

Table 1. A summary of different implantation and activation parameters and the corresponding results. I_{on} was extracted at $V_{ds} = V_{on} = V_g - V_{off} = -0.5$ V for $I_{off} = 1$ nA/μm. SS_{avg} is the average subthreshold swing from the minimum of drain current for 4 orders of magnitude at $V_{ds} = 0.1$ V.

Set	Implantation	Activation	I_{on} μA/μm	SS_{avg} mV/dec	Linear Onset
pTFET (Set1)	P 1×10^{15} cm^{-2} 45° B 5×10^{14} cm^{-2} 45°	500 °C 20 s	8.52	84	No
pTFET (Set1)	P 1×10^{15} cm^{-2} 45° B 5×10^{14} cm^{-2} 45°	600 °C 20 s	3.94	126	No
pTFET (Set2)	P 5×10^{15} cm^{-2} 45° B 1×10^{15} cm^{-2} 45°	550 °C 10 s	2.41	102	Yes
nTFET (Set2)	P 5×10^{15} cm^{-2} 45° B 1×10^{15} cm^{-2} 45°	550 °C 10 s	0.78	153	No
nTFET (Set3)	P 1×10^{15} cm^{-2} 0° B 1×10^{15} cm^{-2} 0°	500 °C 10 s	15	76	Yes

4. Conclusions

By proposing the advantage of a single nanowire over an array of nanowires in studying the effect of different process steps, we have investigated how ion implantation and dopant activation parameters impact the performance of strained silicon single NW GAA TFETs. The goal was to improve the TFETs in terms of I_{on}-current and average subthreshold swing. The best result was achieved for n-TFETs with ion implantation in the normal direction to the nanowire surface and dopant activation at a moderate temperature of 500 °C, as compared to the annealing temperature of 550 °C for p-TFETs. Such optimized n-TFETs deliver high I_{on}-currents of 15 μA/μm at $V_{dd} = 0.5$ V and a low average subthreshold swing of 76 mV/dec over 4 decades of drain current.

Author Contributions: K.N. fabricated and measured the devices and wrote the paper; S.T. performed the e-beam lithography; A.T. deposited the gate oxide and metal layers; S.M. and Q.-T.Z. contributed to the analysis of data and writing of the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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