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Bias Stability Enhancement in Thin-Film Transistor with a Solution-Processed ZrO_2 Dielectric as Gate Insulator

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Abstract: In this paper, a high-k metal-oxide film (ZrO_2) was successfully prepared by a solution-phase method, and whose physical properties were measured by X-ray diffraction (XRD), X-ray reflectivity (XRR) and atomic force microscopy (AFM). Furthermore, indium–gallium–zinc oxide thin-film transistors (IGZO-TFTs) with high-k ZrO_2 dielectric layers were demonstrated, and the electrical performance and bias stability were investigated in detail. By spin-coating 0.3 M precursor six times, a dense ZrO_2 film, with smoother surface and fewer defects, was fabricated. The TFT devices with optimal ZrO_2 dielectric exhibit a saturation mobility up to 12.7 $cm^2\ V^{-1}\ s^{-1}$, and an on/off ratio as high as 7.6×10^5. The offset of the threshold voltage was less than 0.6 V under positive and negative bias stress for 3600 s.

Keywords: thin-film transistors; high dielectric constant; solution process; bias stability

1. Introduction

Due to their high mobility, good transparency to visible light, good uniformity and reasonable electrical stability, metal-oxide thin-film transistors (TFTs) have attracted great attention in the field of active matrix devices such as liquid crystal displays (LCDs) and organic light-emitting diodes (OLEDs) [1–4]. The gate dielectric plays an important role in TFTs because it manipulates the conductance of the semiconducting channel by accumulating charge carriers. Moreover, its electrical insulation to minimize a leakage current is another critical requirement for minimal static dissipation [5], which simultaneously affects the transfer performance and the stability and lifetime of TFT devices.

Recently, considerable efforts have been devoted to fabricating metal-oxide-based TFTs with high dielectric constant (high-k) gate dielectrics. High-k dielectrics can increase the capacitive coupling between the gate and the active channel layer, which not only increases the driving current, but also reduces the operating voltage. Moreover, high-k materials are highly desirable for improving the electrical performance, reducing the size of the device, as well as reducing energy consumption [6]. Nowadays, a number of high-k metal-oxide dielectrics (such as Al_2O_3 [7], ZrO_2 [8], HfO_2 [9], TiO_2,

Y_2O_3 [10], Ta_2O_5 and CeO_2) have been widely studied and used as an alternative to conventional SiO_2 dielectric layers (k = 3.9) with low leakage current density. Among these gate oxides, zirconium oxide (ZrO_2) is one of the attractive materials because of its excellent physical properties, for example, high dielectric constant (23–29), good thermal stability, wide band gap (5–7 eV), and large transparency in the visible and infrared ranges [11,12].

Various vacuum preparation technologies (such as sputter deposition) have been used to prepare metal-oxide films. However, these methods require high-vacuum conditions and a photolithography patterning process that leads to high costs and cumbersome fabrication procedures [2,5,13,14]. To overcome these problems, alternative film-deposition methods have been proposed [15]. The solution-phase processes (such as spin-coating, spray-coating and ink-jet printing) possess many advantages of scalability, roll-to-roll manufacturing and low-cost fabrication processability. For instance, solution-processed ZrO_2 films has attracted much interest, since they have the advantages of low cost, easy chemical composition control and compatibility for large-scale roll-to-roll production [16]. Gong et al. [17] fabricated high-quality ZrO_2 films by a combination of a solution-phase process and ultraviolet (UV) irradiation. The ZrO_2 films with 1 h UV curing showed a leakage current of 1.7×10^{-6} A/cm^2 at -3 V, a bandgap of 6.13 eV, and a high dielectric constant of 17.8. Naik et al. [18] reported on solution-processed bottom-gate, bottom-contact indium–zinc–tin oxide (IZTO) TFTs with a mobility of >2 cm^2 V^{-1} s^{-1}. The solution-processed ZrO_x film, with a thickness of 40 nm, showed a leakage current less than 10^{-10} A/µm.

However, solution-processed TFTs suffer from severe bias-stress instability for device operation because of inherently rich and undefined defect states, such as pores and organic impurities [19]. For instance, Kim et al. [20] fabricated a zinc–tin oxide (ZTO)/indium–gallium–zinc oxide (IGZO) dual-active-layered ZTO/IGZO TFT (DALZI TFT) and an unpassivated IGZO TFT, which exhibited voltage shifts of -1.86 V and -19.59 V, respectively, under negative bias illumination stress conditions (stress time = 1000 s). Lee et al. [21] reported on an IGZO TFT with a solution-processed Al_2O_3 gate dielectric, and the threshold voltage shift of the IGZO TFT was +3.66 V under a gate bias of +20 V for 3600 s. Some methods, such as increasing annealing temperature or using a UV/ozone treatment, have been used to solve this problem [22–24]. Liu et al. [23] reported an In_2O_3 thin-film transistor using a solution-processed ZrO_2 dielectric. The ZrO_2 film, with a leakage current density of 10^{-9} A/cm^2 at 2 MV/cm, was processed by a UV/ozone treatment and annealed at 500 °C. The threshold voltage shift was 0.22 V for In_2O_3 TFTs under PBS with a V_{GS} value of 1.5 V for 7200 s. Solution-processed amorphous indium–zinc–tin oxide (a-IZTO) thin-film transistors (TFTs) with spin-coated zirconium oxide (ZrO_x) as the gate insulator were presented by Naik et al. [18]. The ZrO_x gate insulator was processed without and with UV/O_3 treatment. The threshold voltage shift was 1.13 V for the untreated ZrO_x-based TFT and was 0.64 V for the UV/O_3-treated ZrO_x-based TFTs. Ha et al. [24] reported on a solution-processed zinc–tin–oxide (ZTO)/ZrO_2 TFT with a 90-nm-thick ZrO2 dielectric annealed at 500 °C for 1 h. The TFT exhibited very small hysteresis windows in both dark and illuminated conditions, and the shift in V_{th} was 0.4 V of negative bias-stress under illumination over 5000 s.

In this paper, solution-processed ZrO_2 dielectric films were demonstrated at a deposition temperature of 400 °C. The electrical properties of ZrO_2 films were characterized by using metal–insulator–metal (MIM) structures, and the physical properties were measured by X-ray diffraction (XRD), X-ray reflectivity (XRR) and atomic force microscopy (AFM). IGZO-TFTs with solution-processed ZrO_2 dielectrics were fabricated on glass substrates. By decreasing the precursor concentration and increasing the spin-coating times, an optimal thickness of ZrO_2 film was achieved, which showed a smooth surface and reduced internal defects. Consequently, the resulting TFT devices had not only good electrical properties but also improved bias stability. When under positive bias and negative bias stress over 3600 s, the offset of threshold voltage was less than 0.6 V. Compared with the previous reports of other groups, our work proposes a simple and feasible way to reduce the defect state of the insulating thin films without a special thermal annealing process such as UV

treatment. Therefore, it will help improve the bias stability of TFTs and promote the development of solution-method TFTs in practical applications.

2. Materials and Methods

2.1. Preparation of ZrO_2 Film

ZrO_2 solution was synthesized by dissolving $ZrCl_2O{\cdot}8H_2O$ (Richjoint, Shanghai, China) in a 2-methoxyethanol (2ME) (Fuyu Fine Chemical, Tianjin, China) solvent. The solution was stirred at 300 r/min at room temperature for 2 h, and was then aged for at least one day [25]. The precursor solution was spin-coated on the indium tin oxide (ITO) substrate at 5000 rpm for 40 s. If multiple spin-coating was used, the wet films were pre-annealed at 300 °C for 5 min after each spin. Finally, the films were post-annealed at 400 °C on the hotplate for 1 h to drive off the solvent and promote the oxidation reaction.

2.2. Fabrication of TFTs

A 150-nm-thick ITO deposited by direct current (DC) sputtering on glass substrates was used as a bottom electrode. ZrO_2 films were formed by spin-coating several times to acquire a certain thickness. 10-nm-thick IGZO was deposited by direct current (DC) pulse sputtering with a pressure of 1 mTorr (O:Ar = 5%) and patterned by shadow mask. Then, the IGZO film was annealed at 300 °C for 1 h. The IGZO target is composed of the atomic ratio of In:Ga:Zn:O = 1:1:1:4. Finally, the Al source/drain electrodes with 100-nm-thickness were deposited by direct current (DC) sputtering at room temperature. The channel width (W) and length (L) of TFTs were 530 μm and 270 μm, thus the W/L ratio was 1.96.

2.3. Characterization

An MIM structure (ITO/ZrO_2/Al) was used to measure the leakage current density and capacitance of the ZrO_2 films. X-ray diffraction (XRD) (EMPYREAN, PANalytical, Almelo, The Netherlands) was used to investigate the crystalline phase of the ZrO_2 film fabricated on the glass substrate. The thickness and roughness of the ZrO_2 films were measured by X-ray reflectivity (XRR) using the same equipment. The thickness can be obtained by fitting the interference fringe of the X-ray. The surface topography of the films was evaluated by atomic force microscopy (AFM) (BY3000, Being Nano-Instruments, Beijing, China) in noncontact mode. The electrical characteristics of TFTs were measured using a semiconductor parameter analyzer (Agilent4155C, Agilent, Santa Clara, CA, USA) under an ambient atmosphere. The current–voltage (I–V) and capacitance–frequency (C–f) characteristics of the MIM capacitor were measured by the Keithley4200 (Tektronix, Beaverton, OR, USA) parameter analyzer under an ambient condition.

3. Results and Discussion

In our experiment, we spun the 0.3 M zirconia precursor on glass substrates one, two, three, four, five and six times. It was found that the thickness of ZrO_2 films increased almost linearly with increasing spin-coating times. Figure 1 is the XRR fitting results of the ZrO_2 films with varying thicknesses. From the fitting results, the thickness of the single-spin-coating film was about 22 nm, and a 130 nm ZrO_2 film can be obtained by six-times spin-coating. Obviously, a thicker film would render a smaller leakage current density. Also, the 0.6 M ZrO_2 precursor was swirled for one, two and three times. The thickness of the ZrO_2 film obtained by using the 0.6 M precursor is about two-fold thicker than that of the ZrO_2 film obtained by using 0.3 M precursor. Additional details are listed in Table 1.

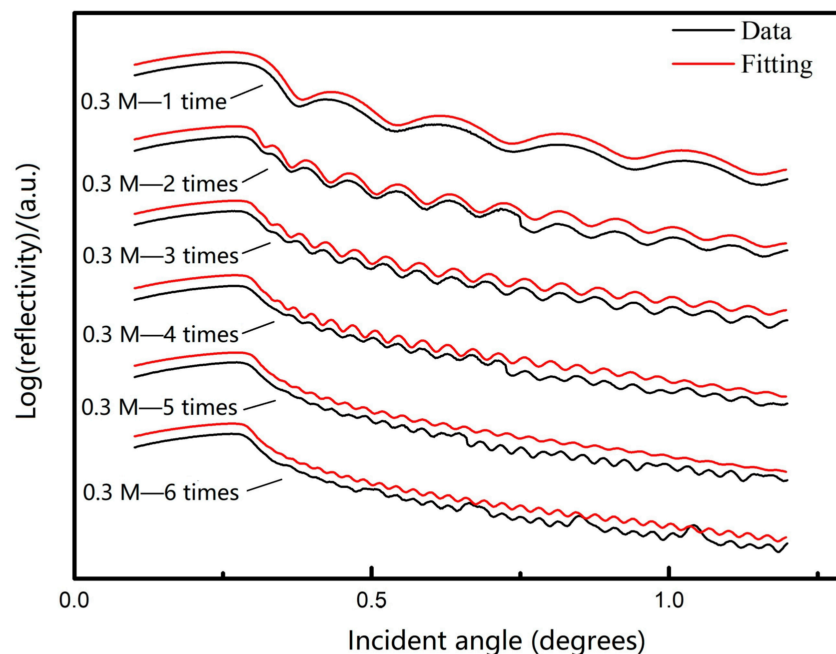

Figure 1. X-ray reflectivity measurements of 0.3 M precursor-based ZrO_2 films of different coating times.

Table 1. The density, thickness and roughness of 0.3 M precursor-based ZrO_2 films of different coating times. The roughness for glass substrate is 0.79 ± 0.32 nm.

Concentration	Layer	Density (g/cm^3)	Thickness (nm)	Roughness (nm)
0.3 M	1	4.86	19.98	0.46
0.3 M	2	4.70	43.53	0.46
0.3 M	3	4.83	66.98	0.26
0.3 M	4	4.78	91.61	0.49
0.3 M	5	4.76	118.89	0.55
0.3 M	6	4.77	129.29	0.41
0.6 M	3	4.70	132.62	0.43

The crystalline phase of the ZrO_2 films with dissimilar thicknesses (67 nm, 130 nm) annealed at different temperatures was investigated by XRD. Figure 2 is the XRD spectra of the ZrO_2 films. The 67-nm-thick film annealed at 400 °C had a clear crystal peak, while the 130-nm-film was still amorphous. We presumed that the thicker film may inhibit the transfer of heat and the crystallization of ZrO_2 film in the post-annealing processing.

To increase the thickness of ZrO_2 film, increasing the concentration of precursor or spin-coating times is an effective method. From the XRR fitting results, the ZrO_2 films obtained by spin-coating 0.6 M precursor for three times, and 0.3 M precursor for three and six times, show a corresponding thickness of 132 nm, 67 nm and 130 nm, respectively. Figure 3 shows the leakage current density of the above ZrO_2 films. The ZrO_2 film with 67 nm thickness demonstrated the largest leakage current density. For ZrO_2 films with 132 nm and 130 nm thicknesses, they exhibited comparable leakage current density despite the difference in the precursor concentration and times. A thick ZrO_2 film may inhibit the crystallization of the film that led to the reduction in leakage current density.

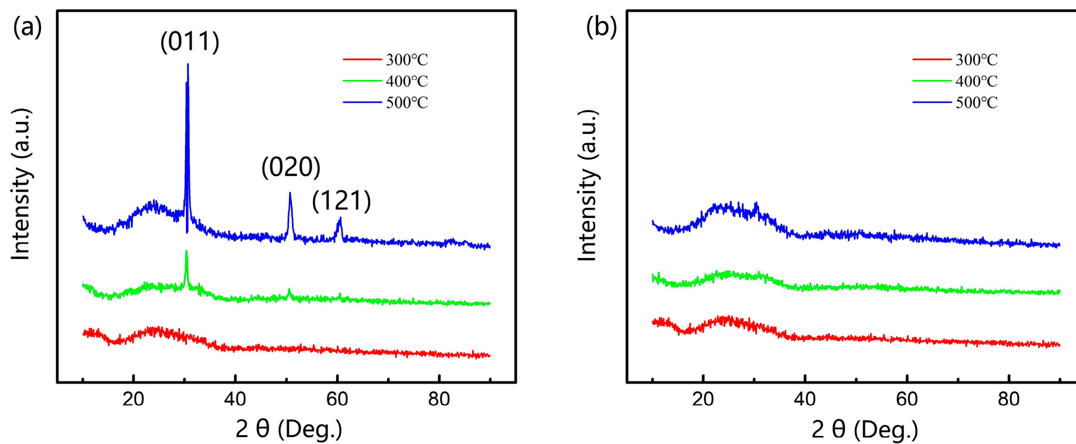

Figure 2. XRD spectra of ZrO_2 films with different post-annealing temperatures. ZrO_2 film of (**a**) 67 nm and (**b**) 130 nm.

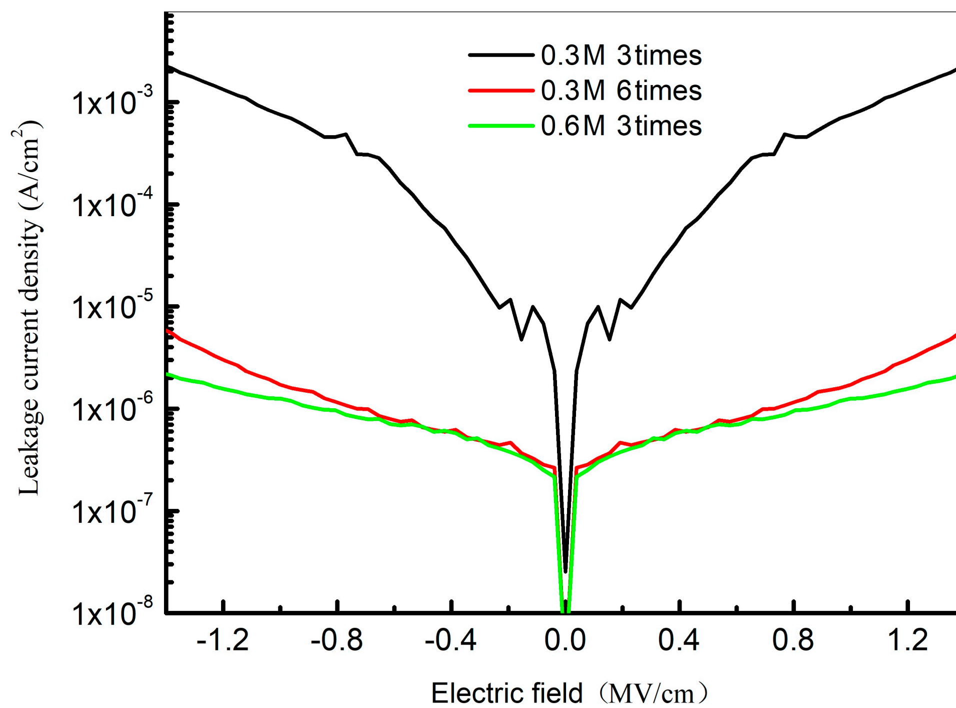

Figure 3. The leakage current density of the ZrO_2 films with altering thicknesses.

Figure 4 shows the device architecture of IGZO-TFTs. IGZO-TFTs were prepared based on the dielectric films obtained by spin-coating with 0.6 M precursor for three times and 0.3 M precursor for six times. The corresponding bias stability is illustrated in Figures 5 and 6. The field effect mobility in the saturation region ($V_{ds} \geq V_{gs} - V_{th}$) and subthreshold swing (SS) were separately obtained by using the following equations:

$$I_{ds} = \frac{1}{2}\frac{W}{L}\mu C_i (V_{gs} - V_{th})^2, \tag{1}$$

$$SS = \frac{dV_{gs}}{d \log I_{ds}}. \tag{2}$$

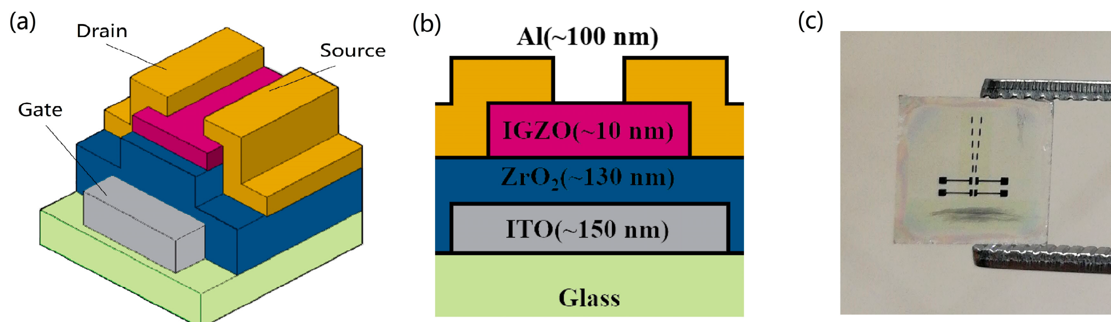

Figure 4. (**a**) Schematic showing the cross-section of IGZO-TFT with ZrO_2 dielectric layer. (**b**) Thickness of each layer. (**c**) Photograph of the fabricated TFT.

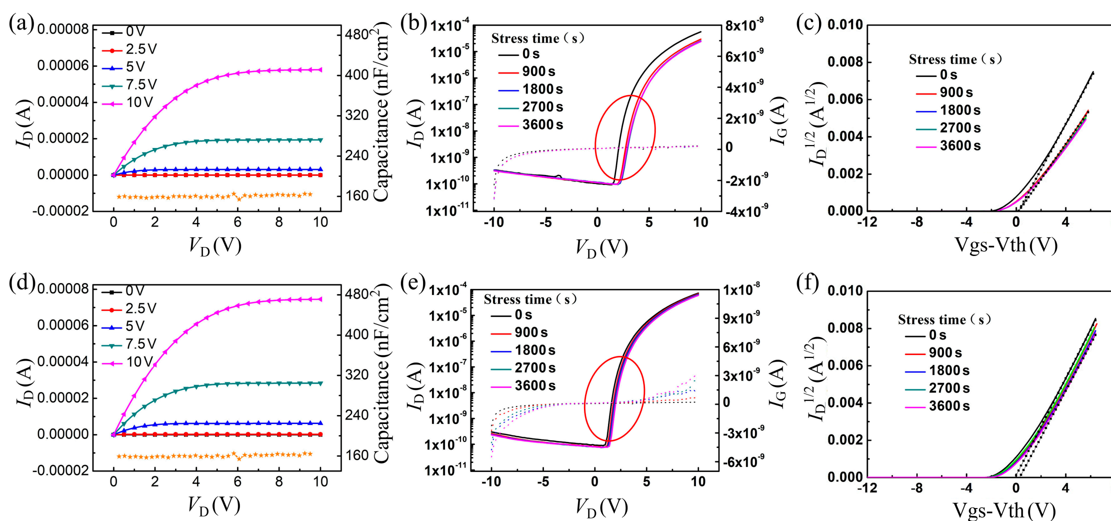

Figure 5. Bias stability of the TFT with ZrO_2 film fabricated by spin-coating of 0.3 M precursor for 6 times. (**a**) Output curves and gate capacitance as a function of voltage. (**b**) Transfer curves with gate-leakage current curves of positive bias stress. (**c**) Plots of sqrt I_{ds} (drain/source current) versus gate overdrive of positive bias stress. (**d**) Output curves and gate capacitance as a function of voltage. (**e**) Transfer curves with gate-leakage current curves of negative bias stress. (**f**) Plots of sqrt I_{ds} (drain/source current) versus gate overdrive of negative bias stress.

W, L, μ_{sat}, C_i, V_{th} and I_{ds} are the channel width, channel length, saturation mobility, capacitance, threshold voltage and drain current, respectively, and V_{ds} and V_{gs} separately represent the source-drain voltage and gate-source voltage. The regions from which SS has been extracted are noted on the figures. The capacitance of the ZrO_2 film is around 130 nF/cm^2. The channel width (W) is 530 µm and the length (L) is 270 µm (W/L ratio is 1.96).

The TFT with the ZrO_2 film achieved by spin-coating with 0.3 M precursor for six times (device A) had a saturation mobility of 12.7 cm^2 V^{-1} s^{-1} and an on/off ratio of 7.6 × 10^5, while the TFT with the ZrO_2 film achieved by spin-coating with 0.6 M precursor for three times (device B) exhibited a saturation mobility of 10 cm^2 V^{-1} s^{-1} and an on/off ratio of 6.4 × 10^5. Also, the device A had excellent bias stability, with an offset of the threshold voltage less than 0.6 V under positive bias, and negative bias stress over 3600 s. For comparison, Ding et al. [26] fabricated the IGZO-TFT with bottom gate and staggered electrodes using atomic-layer-deposited Al_2O_3 as gate insulator. The TFT device showed a threshold voltage shift of 1.5 V under 10 V gate voltage for 1 h. Li et al. [27] reported on the SiNx/IGZO-TFT with reactive sputtered SiOx as passivation layer, and the device exhibited a V_{th} shift of 1.3 V after applying positive bias stress of 20 V for 10,000 s. However, in our study, the device B not only had a lower saturation mobility, but exhibited a larger threshold voltage shifting under the bias

stress test, with a voltage shifting of 1.6 V under positive bias stress over 3600 s. Additional details are listed in Table 2. The trend of parameters in Table 2 is shown in Figures 7 and 8.

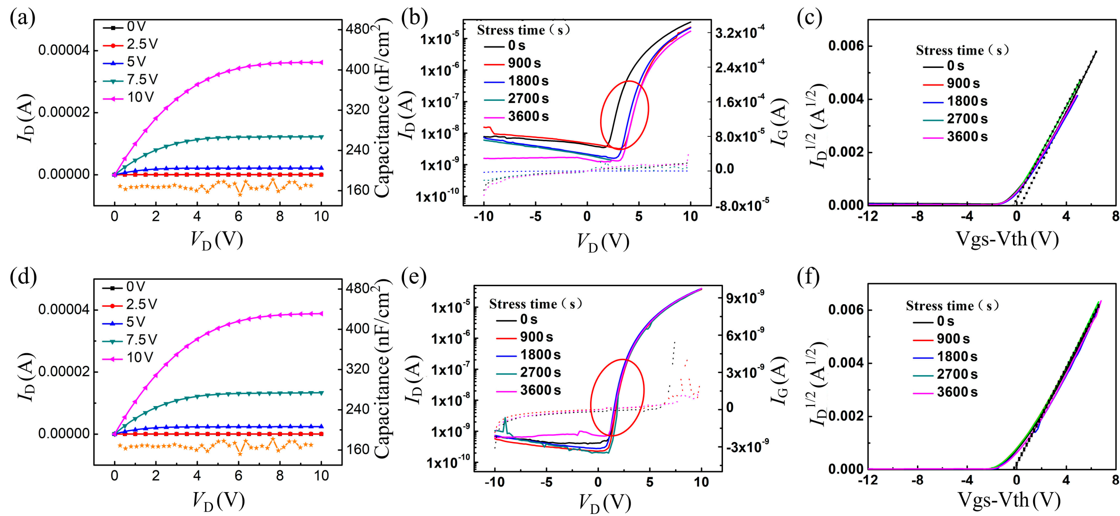

Figure 6. Bias stability of the TFT with ZrO_2 film fabricated by 0.6 M precursor spin-coating 3 times. (**a**) Output curves and gate capacitance as a function of voltage. (**b**) Transfer curves with gate-leakage current curves of positive bias stress. (**c**) Plots of sqrt I_{ds} (drain/source current) versus gate overdrive of positive bias stress. (**d**) Output curves and gate capacitance as a function of voltage. (**e**) Transfer curves with gate-leakage current curves of negative bias stress. (**f**) Plots of sqrt I_{ds} (drain/source current) versus gate overdrive of negative bias stress.

Table 2. Electrical characteristics of the devices. Device A: The TFTs with the ZrO_2 films obtained by spin-coating with 0.3 M precursor for 6 times. Device B: The TFTs with the ZrO_2 films obtained by spin-coating with 0.6 M precursor for 3 times.

Device	Stress Time (s)	Negative Bias Stress (NBS)				Positive Bias Stress (PBS)			
		μ_{sat} (cm^2 V^{-1} s^{-1})	I_{on}/I_{off} ($\times 10^5$)	SS (V/dec)	V_{th} (V)	μ_{sat} (cm^2 V^{-1} s^{-1})	I_{on}/I_{off} ($\times 10^5$)	SS (V/dec)	V_{th} (V)
Device A	0	12.7 ± 0.34	7.6 ± 0.51	0.34 ± 0.06	3.34 ± 0.05	11.9 ± 0.32	5.6 ± 0.42	0.37 ± 0.05	3.81 ± 0.07
	900	12.4 ± 0.35	7.6 ± 0.55	0.35 ± 0.07	3.55 ± 0.08	8.5 ± 0.21	2.6 ± 0.22	0.45 ± 0.05	4.28 ± 0.06
	1800	12.3 ± 0.30	7.5 ± 0.55	0.34 ± 0.04	3.63 ± 0.06	7.7 ± 0.20	2.2 ± 0.19	0.46 ± 0.04	4.40 ± 0.04
	2700	12.2 ± 0.31	7.0 ± 0.52	0.35 ± 0.05	3.70 ± 0.04	7.5 ± 0.20	2.2 ± 0.19	0.47 ± 0.02	4.40 ± 0.02
	3600	12.1 ± 0.31	6.8 ± 0.50	0.35 ± 0.06	3.67 ± 0.05	7.4 ± 0.20	2.1 ± 0.18	0.48 ± 0.02	4.43 ± 0.02
Device B	0	9.8 ± 0.10	0.92 ± 0.058	0.55 ± 0.06	3.49 ± 0.16	9.5 ± 0.28	0.090 ± 0.0062	0.70 ± 0.05	3.62 ± 0.03
	900	9.7 ± 0.02	1.5 ± 0.098	0.49 ± 0.03	3.52 ± 0.06	8.6 ± 0.42	0.067 ± 0.0051	0.74 ± 0.02	5.10 ± 0.06
	1800	9.9 ± 0.02	1.3 ± 0.084	0.51 ± 0.04	3.42 ± 0.03	8.5 ± 0.37	0.13 ± 0.0098	0.70 ± 0.03	4.96 ± 0.01
	2700	9.9 ± 0.96	1.8 ± 0.15	0.44 ± 0.14	3.27 ± 0.04	7.8 ± 0.41	0.12 ± 0.0098	0.69 ± 0.03	5.11 ± 0.03
	3600	9.5 ± 0.48	0.58 ± 0.056	0.58 ± 0.04	3.17 ± 0.05	7.1 ± 0.04	0.13 ± 0.011	0.69 ± 0.03	5.18 ± 0.03

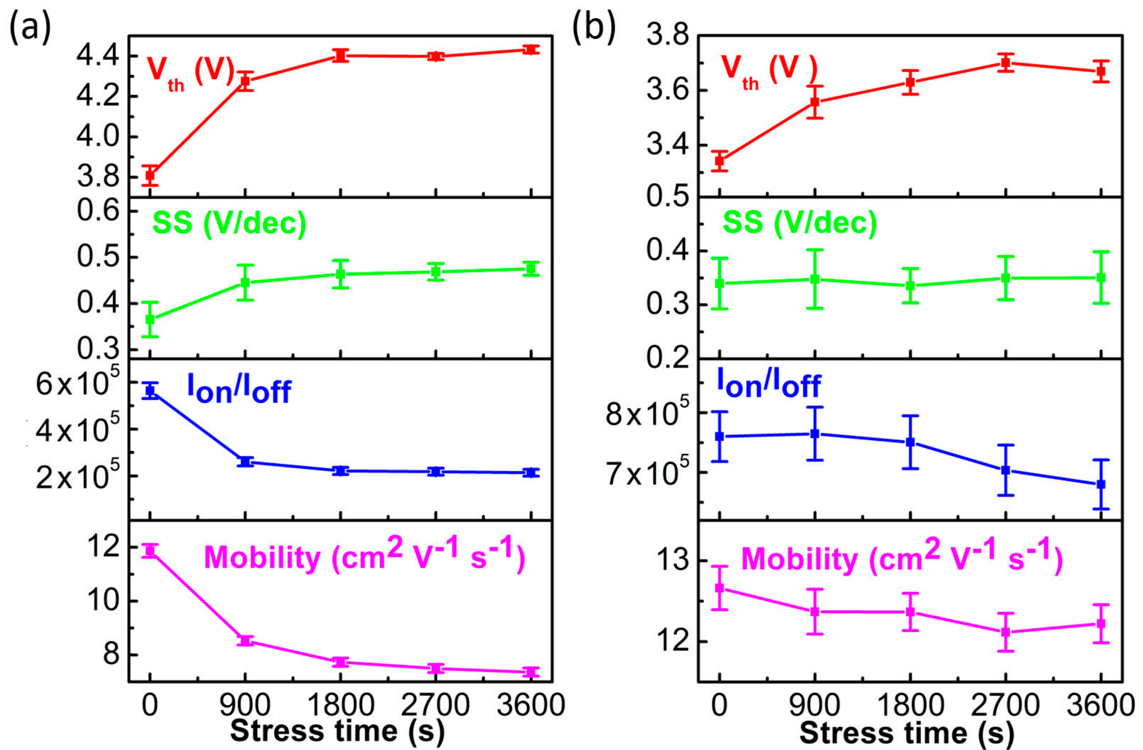

Figure 7. The trend of electrical characteristics of the TFT with ZrO_2 film fabricated by 0.3 M precursor spin-coating 6 times. (**a**) Positive bias stress. (**b**) Negative bias stress.

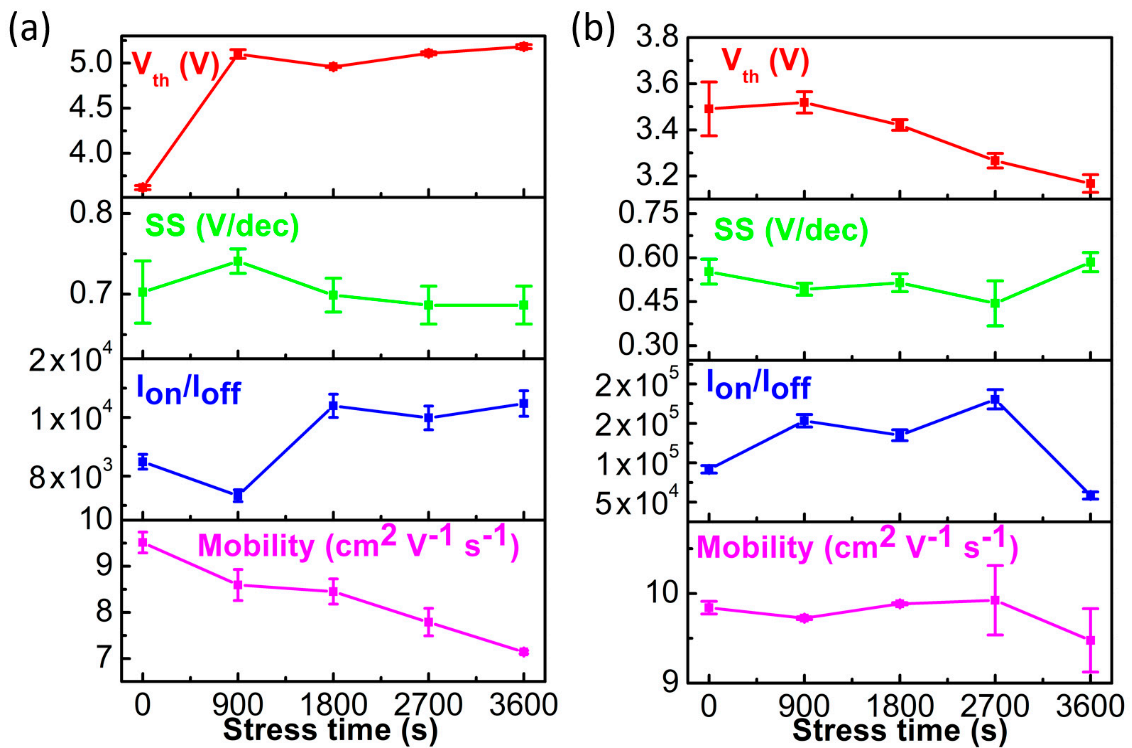

Figure 8. The trend of electrical characteristics of the TFT with ZrO_2 film fabricated by 0.6 M precursor spin-coating 3 times. (**a**) Positive bias stress. (**b**) Negative bias stress.

The leakage current densities (shown in Figure 3) of ZrO_2 films obtained by spin-coating with 0.6 M and 0.3 M precursor for three and six times, respectively, were quite similar. However, the bias stability of the TFTs based on them were greatly different. Figure 9 shows the top view and polarizing graphs of the MIM structure. In order to compare the electrical homogeneity of the insulating films mentioned above, we select nine feature points on the insulating film to measure the leakage current density, as shown in Figure 9. Figure 10 shows the leakage current density of each feature point. Table 3 shows the statistics of electrical properties of each feature point. It can be seen that the ZrO_2 film achieved by spin-coating with 0.3 M precursor for six times had better electrical uniformity.

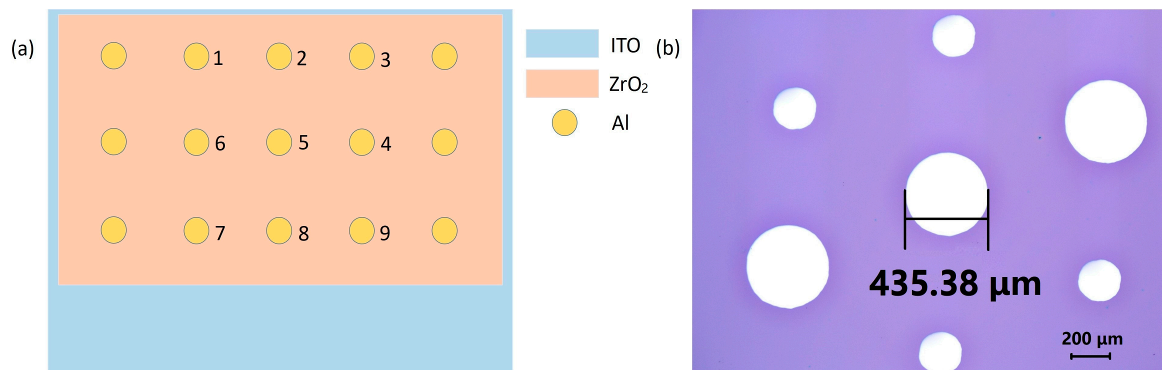

Figure 9. The overlook view of the MIM structure. (**a**) Overlook view. (**b**) Polarizing photograph.

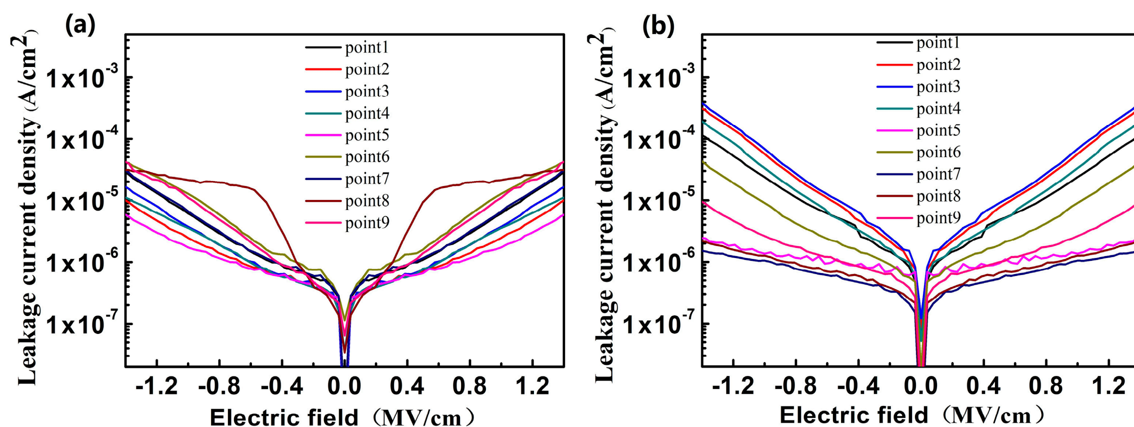

Figure 10. The leakage current density of each feature point on the ZrO_2 film. (**a**) 0.3 M precursor spin-coating 6 times. (**b**) 0.6 M precursor spin-coating 3 times.

Table 3. The statistics of electrical properties of each feature point.

ZrO_2 Films	Leakage Current Density (A/cm^2) (10 V)			
	Average Value	Maximum Value	Minimum Value	Standard Deviation
0.6 M precursor spin-coating 3 times	6.9×10^{-6}	2.1×10^{-5}	5.1×10^{-7}	7.8×10^{-6}
0.3 M precursor spin-coating 6 times	1.6×10^{-6}	3.4×10^{-6}	4.0×10^{-7}	9.39×10^{-7}

Figure 11 is the AFM diagram of ZrO_2 films fabricated by spin-coating with 0.6 M precursor for three times and 0.3 M precursor for six times. Both of them had low roughness, and the root mean square of ZrO_2 films in devices A and B were 0.16 nm and 0.18 nm, respectively. After the precursor was spin-coated, a wet film was formed containing a large number of ions. The high-concentration

precursor (0.6 M) might lead to high surface roughness due to the irregular arrangement of atoms during the annealing process, during which Zr and O elements moved and recombined to form Zr–O bonding. From the results above, the ZrO_2 films in device A showed smoother surface, lower leakage current density and better electrical uniformity. A smooth surface morphology may result in the alleviation of electron trapping at the channel–insulator interface, which is a great contribution to improve the electrical properties and bias stability of TFTs [28–30].

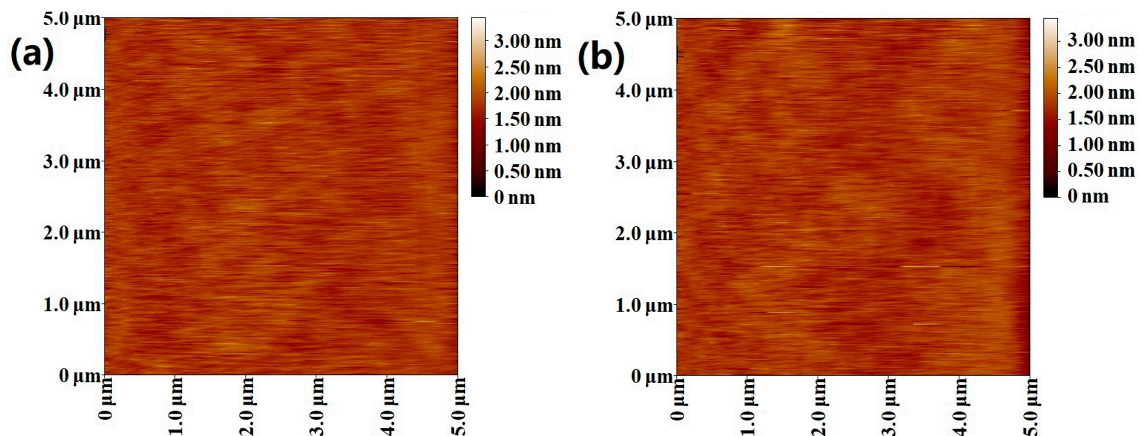

Figure 11. Atomic force microscopy (AFM) diagrams of ZrO_2 films. (**a**) 0.3 M precursor spin-coating 6 times. (**b**) 0.6 M precursor spin-coating 3 times.

From the XRR fitting results, the densities of ZrO_2 films fabricated by spin-coating with 0.3 M precursor for six times and 0.6 M precursor for three times were 4.77 and 4.70 g/cm^3, respectively. The relative porosity volume can be calculated from the densities of ZrO_2 films using the following equation:

$$q = \frac{\rho_1 - \rho}{\rho_1 - \rho_2},$$

where q, ρ, $\rho1$ and $\rho2$ represent the relative porosity volume, film density, bulk ZrO_2 density (5.68 g/cm^3) and void density (air), respectively. The calculated relative porosity volume of 0.3 M ZrO_2 dielectric layer and 0.6 M ZrO_2 dielectric layer were 16.02% and 17.26%, respectively. Figure 12 shows a schematic diagram describing the internal defects of ZrO_2 films. The solution-processed films may have many pores and impurities, which were possibly formed during vaporization, decomposition and condensation processes [31]. The advantage of multilayered stacks of ZrO_2 films is that the pinholes and pore regions of the sub layers may be filled by the subsequent solution process. Another advantage is that the multilayer structure can make the direct penetration of each layer more random, and it is not easy to form a direct penetration channel that runs through all layers. Furthermore, the wet film obtained by low-concentration precursor is thinner during each spin-coating. The conduction of heat is more efficient in a thinner wet film during the pre-annealing process, which is helpful to reduce the impurities and defects.

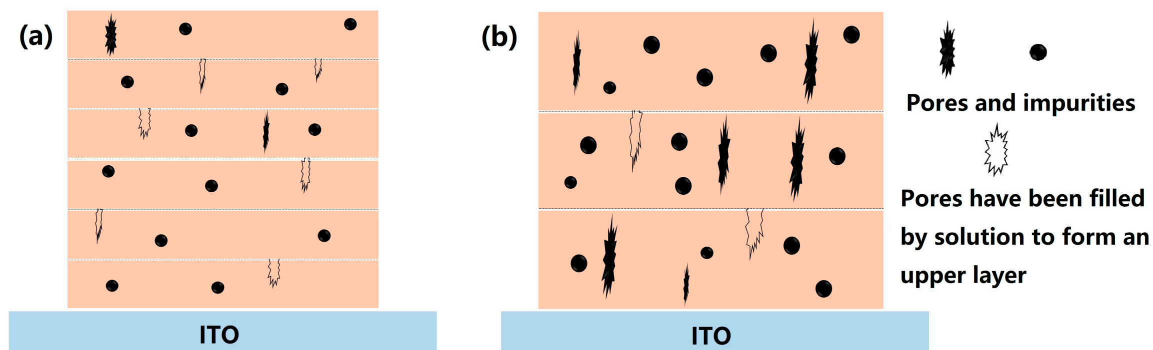

Figure 12. Cross-sectional schematic diagrams of ZrO_2 films. (**a**) 0.3 M precursor spin-coating 6 times. (**b**) 0.6 M precursor spin-coating 3 times. The interfacial pores and pinholes in the sublayer filled by solution to form an upper layer.

4. Conclusions

In this paper, we explored the influence of the spin-coating times and the precursor concentration on the dielectrics of solution-processed ZrO_2 films. It is interesting that a thicker film may inhibit the crystallization of the film during the post-annealing process, thus improving the dielectric properties. Moreover, ZrO_2 films fabricated by spin-coating with 0.3 M precursor for six times had lower leakage current density and better electrical uniformity than the film fabricated by spin coating with 0.6 M precursor for three times, thus rendering excellent electrical properties and bias stability of the TFT device. Two possible mechanisms for the improvement of device characteristics have been concluded. (1) The pinholes or pore sites of the sublayer may be filled by a subsequent solution process in the multilayered structure, so there are fewer impurities and defects in the films. (2) The conduction of heat is more efficient in a thinner wet film during vaporization, decomposition and condensation processes, which is beneficial to the reduction of impurities and defects.

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References

1. Park, J.S.; Maeng, W.-J.; Kim, H.-S.; Park, J.-S. Review of recent developments in amorphous oxide semiconductor thin-film transistor devices. *Thin Solid Films* **2012**, *520*, 1679–1693. [CrossRef]
2. Fortunato, E.; Barquinha, P.; Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **2012**, *24*, 2945–2986. [CrossRef] [PubMed]
3. Xu, W.; Dai, M.; Liang, L.; Liu, Z.; Sun, X.; Wan, Q.; Cao, H. Anomalous bias-stress-induced unstable phenomena of InZnO thin-film transistors using Ta_2O_5 gate dielectric. *J. Phys. D Appl. Phys.* **2012**, *45*. [CrossRef]
4. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **2004**, *432*, 488–492. [CrossRef] [PubMed]

5. Park, S.; Kim, C.-H.; Lee, W.-J.; Sung, S.; Yoon, M.-H. Sol-gel metal oxide dielectrics for all-solution-processed electronics. *Mater. Sci. Eng. R Rep.* **2017**, *114*, 1–22. [CrossRef]
6. Li, X.F.; Xin, E.L.; Zhang, J.H. Low-Temperature Solution-Processed Zirconium Oxide Gate Insulators for Thin-Film Transistors. *IEEE Trans. Electron Devices* **2013**, *60*, 3413–3416.
7. Chen, R.S.; Zhou, W.; Zhang, M.; Kwok, H.S. High performance self-aligned top-gate ZnO thin film transistors using sputtered Al_2O_3 gate dielectric. *Thin Solid Films* **2012**, *520*, 6681–6683. [CrossRef]
8. Cho, J.; Choi, P.; Lee, N.; Kim, S.; Choi, B. Dielectric Properties of Solution-Processed ZrO_2 for Thin-Film Transistors. *J. Nanosci. Nanotechnol.* **2016**, *16*, 10380–10384. [CrossRef]
9. Lin, W.K.; Liu, K.C.; Chang, S.T.; Li, C.S. Room temperature fabricated transparent amorphous indium zinc oxide based thin film transistor using high-kappa HfO_2 as gate insulator. *Thin Solid Films* **2012**, *520*, 3079–3083. [CrossRef]
10. Bobade, S.M.; Shin, J.H.; Cho, Y.J.; You, J.S.; Choi, D.K. Room temperature fabrication Oxide TFT with Y_2O_3 as a gate oxide and Mo contact. *Appl. Surf. Sci.* **2009**, *255*, 7831–7833. [CrossRef]
11. Liao, L.; Bai, J.; Lin, Y.-C.; Qu, Y.; Huang, Y.; Duan, X. High-Performance Top-Gated Graphene-Nanoribbon Transistors Using Zirconium Oxide Nanowires as High-Dielectric-Constant Gate Dielectrics. *Adv. Mater.* **2010**, *22*, 1941–1945. [CrossRef] [PubMed]
12. Zhang, W.; Cui, Y.; Hu, Z.G.; Yu, W.L.; Sun, J.; Xu, N.; Ying, Z.F.; Wu, J.D. Structural, optical and electrical properties of high-k ZrO_2 dielectrics on Si prepared by plasma assisted pulsed laser deposition. *Thin Solid Films* **2012**, *520*, 6361–6367. [CrossRef]
13. Jang, J.; Kitsomboonloha, R.; Swisher, S.L.; Park, E.S.; Kang, H.; Subramanian, V. Transparent High-Performance Thin Film Transistors from Solution-Processed SnO_2/ZrO_2 Gel-like Precursors. *Adv. Mater.* **2013**, *25*, 1042–1047. [CrossRef] [PubMed]
14. Lim, K.-H.; Huh, J.-E.; Lee, J.; Cho, N.-K.; Park, J.-W.; Nam, B.-I.; Lee, E.; Kim, Y.S. Strong Influence of Humidity on Low-Temperature Thin-Film Fabrication via Metal Aqua Complex for High Performance Oxide Semiconductor Thin-Film Transistors. *ACS Appl. Mater. Interfaces* **2017**, *9*, 548–557. [CrossRef] [PubMed]
15. Lim, K.-H.; Lee, J.; Huh, J.-E.; Park, J.; Lee, J.-H.; Lee, S.-E.; Kim, Y.S. A systematic study on effects of precursors and solvents for optimization of solution-processed oxide semiconductor thin-film transistors. *J. Mater. Chem. C* **2017**, *5*, 7768–7776. [CrossRef]
16. Gong, Y.; Zhao, K.; He, H.; Cai, W.; Tang, N.; Ning, H.; Wu, S.; Gao, J.; Zhou, G.; Lu, X.; et al. Solution processable high quality ZrO_2 dielectric films for low operation voltage and flexible organic thin film transistor applications. *J. Phys. D Appl. Phys.* **2018**, *51*. [CrossRef]
17. Gong, Y.; Zhao, K.; Yan, L.; Wei, W.; Yang, C.; Ning, H.; Wu, S.; Gao, J.; Zhou, G.; Lu, X.; et al. Room Temperature Fabrication of High Quality ZrO_2 Dielectric Films for High Performance Flexible Organic Transistor Applications. *IEEE Electron Device Lett.* **2018**, *39*, 280–283. [CrossRef]
18. Naik, B.R.; Avis, C.; Chowdhury, M.D.H.; Kim, T.; Lin, T.; Jang, J. Improvement in performance of solution-processed indium-zinc-tin oxide thin-film transistors by UV/O_3 treatment on zirconium oxide gate insulator. *Jpn. J. Appl. Phys.* **2016**, *55*. [CrossRef]
19. Jeong, Y.; Bae, C.; Kim, D.; Song, K.; Woo, K.; Shin, H.; Cao, G.; Moon, J. Bias-Stress-Stable Solution-Processed Oxide Thin Film Transistors. *ACS Appl. Mater. Interfaces* **2010**, *2*, 611–615. [CrossRef] [PubMed]
20. Kim, C.H.; Rim, Y.S.; Kim, H.J. The effect of a zinc-tin-oxide layer used as an etch-stopper layer on the bias stress stability of solution-processed indium-gallium-zinc-oxide thin-film transistors. *J. Phys. D Appl. Phys.* **2014**, *47*. [CrossRef]
21. Yih-Shing, L.; Yu-Hsin, W.; Tsung-Cheng, T.; Tsung-Eong, H. Positive bias stress instability of In-Ga-Zn-O thin-film transistors with Al_2O_3/TEOS oxide gate dielectrics. In Proceedings of the 2017 24th International Workshop on Active-Matrix Flatpanel Displays and Devices, Kyoto, Japan, 4–7 July 2017; pp. 205–206.
22. Kim, S.J.; Yoon, D.H.; Rim, Y.S.; Kim, H.J. Low-Temperature Solution-Processed ZrO_2 Gate Insulators for Thin-Film Transistors Using High-Pressure Annealing. *Electrochem. Solid State Lett.* **2011**, *14*, E35–E37. [CrossRef]
23. Liu, A.; Liu, G.X.; Zhu, H.H.; Xu, F.; Fortunato, E.; Martins, R.; Shan, F.K. Fully Solution-Processed Low-Voltage Aqueous In_2O_3 Thin-Film Transistors Using an Ultrathin ZrOx Dielectric. *ACS Appl. Mater. Interfaces* **2014**, *6*, 17364–17369. [CrossRef] [PubMed]

24. Ha, T.-J.; Dodabalapur, A. Photo stability of solution-processed low-voltage high mobility zinc-tin-oxide/ZrO_2 thin-film transistors for transparent display applications. *Appl. Phys. Lett.* **2013**, *102*. [CrossRef]
25. Cai, W.; Zhu, Z.; Wei, J.; Fang, Z.; Ning, H.; Zheng, Z.; Zhou, S.; Yao, R.; Peng, J.; Lu, X. A Simple Method for High-Performance, Solution-Processed, Amorphous ZrO_2 Gate Insulator TFT with a High Concentration Precursor. *Materials* **2017**, *10*. [CrossRef] [PubMed]
26. Ding, X.; Zhang, J.; Zhang, H.; Ding, H.; Huang, C.; Li, J.; Shi, W.; Jiang, X.; Zhang, Z. ZrO_2 insulator modified by a thin Al_2O_3 film to enhance the performance of InGaZnO thin-film transistor. *Microelectron. Reliab.* **2014**, *54*, 2401–2405. [CrossRef]
27. Ding, X.; Zhang, H.; Zhang, J.; Li, J.; Shi, W.; Jiang, X.; Zhang, Z. IGZO thin film transistors with Al_2O_3 gate insulators fabricated at different temperatures. *Mater. Sci. Semicond. Process.* **2015**, *29*, 69–75. [CrossRef]
28. Li, J.; Zhou, F.; Lin, H.-P.; Zhu, W.-Q.; Zhang, J.-H.; Jiang, X.-Y.; Zhang, Z.-L. Effect of reactive sputtered SiOx passivation layer on the stability of InGaZnO thin film transistors. *Vacuum* **2012**, *86*, 1840–1843. [CrossRef]
29. Verlaak, S.; Arkhipov, V.; Heremans, P. Modeling of transport in polycrystalline organic semiconductor films. *Appl. Phys. Lett.* **2003**, *82*, 745–747. [CrossRef]
30. Jeong, J.K.; Yang, H.W.; Jeong, J.H.; Mo, Y.G.; Kim, H.D. Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors. *Appl. Phys. Lett.* **2008**, *93*. [CrossRef]
31. Kim, D.J.; Kim, D.L.; Rim, Y.S.; Kim, C.H.; Jeong, W.H.; Lim, H.S.; Kim, H.J. Improved Electrical Performance of an Oxide Thin-Film Transistor Having Multistacked Active Layers Using a Solution Process. *ACS Appl. Mater. Interfaces* **2012**, *4*, 4001–4005. [CrossRef] [PubMed]

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