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High Performance GAA SNWT with a Triangular Cross Section: Simulation and Experiments

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Abstract: In this paper, we present a gate-all-around silicon nanowire transistor (GAA SNWT) with a triangular cross section by simulation and experiments. Through the TCAD simulation, it was found that with the same nanowire width, the triangular cross-sectional SNWT was superior to the circular or quadrate one in terms of the subthreshold swing, on/off ratio, and SCE immunity, which resulted from the smallest equivalent distance from the nanowire center to the surface in triangular SNWTs. Following this, we fabricated triangular cross-sectional GAA SNWTs with a nanowire width down to 20 nm by TMAH wet etching. This process featured its self-stopped etching behavior on a silicon (1 1 1) crystal plane, which made the triangular cross section smooth and controllable. The fabricated triangular SNWT showed an excellent performance with a large Ion/Ioff ratio (~10^7), low SS (85 mV/dec), and preferable DIBL (63 mV/V). Finally, the surface roughness mobility of the fabricated device at a low temperature was also extracted to confirm the benefit of a stable cross section.

Keywords: silicon nanowire; triangular cross section; simulation; experiment; TMAH; low temperature; mobility

1. Introduction

The semiconductor industry is driven by the continuous device scaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) according to Moore's Law. However, with the feature size stepping into the nano-scaled regime, the traditional planar device is confronted with great challenges, such as a weaker electrostatic controllability and larger body leakage. Recently, enormous attention has been paid to gate-all-around silicon nanowire transistors (GAA SNWT) due to their extraordinary electrostatic controllability, and they are considered as one of the most promising candidates in the sub-10nm technology node.

However, GAA SNWT still has some issues relating to its performance and process which need to be addressed before it is used in commercial applications. Firstly, the short channel effect (SCE) is a critical factor affecting the device's static power consumption and driving performance. In principle, it can be effectively suppressed by continuously reducing the line width of nanowires. Many research institutions have already done a lot of work in this area [1–5]. However, some issues still emerge, such as the limitation of the lithography patterning and the geometry variation from process instability [6]. Therefore, it is necessary to suppress SCE by optimizing the structure besides the line width, such as the cross-sectional shape, thereby improving the device performance.

The second challenge comes from the lack of a feasible method for fabricating three-dimension suspended silicon nanowire with an accurately controlled size and cross-sectional shape [7], which is beneficial to the device variability suppression and mobility enhancement. Meanwhile, this silicon

nanowire process flow should be highly compatible with the traditional CMOS technology considering its manufacturability.

For the first challenge, we proposed a triangular shape to be the optimized cross section for the nanowire and to confirm its advantages in scalability and performance by TCAD simulation. For the second issue, we adopted the anisotropic TMAH wet etching process to form the suspended nanowire channel with a stable, smooth, and precisely-size-controlled inverted triangular cross section shape. The low-temperature mobility characterization was then carried out to evaluate the benefit to the suppression of surface roughness scattering by the self-limited structure.

2. Simulation

2.1. Device Parameters

GAA SNWTs with three typical cross-sectional shapes, including triangles, squares, and circles, were simulated by TCAD tool Synopsys Sentaurus. The schematic structure of the device with three different cross-sectional shapes is shown in Figure 1. Considering the consistency in fabrication, the three nanowires were set as the same line width D. Some key process parameters were based on the requirements for a 5 nm technology node in IRDS 2017 [8].

Owing to the excellent controllability of the channel potential in GAA SNWTs, the silicon film thickness or line width of nanowire can be relaxed to L_g [9]. Therefore, the nanowire width of the GAA SNWTs was set to 16 nm according to IRDS 2017, and the gate length was set to the range of 12 to 28 nm. The other device parameters are listed in Table 1. The models we used in Sentaurus tools include Mobility (PhuMob &high field saturation & Enormal), Effective Intrinsic Density, Recombination (SRH(DopingDep)), and Quantum Potential model.

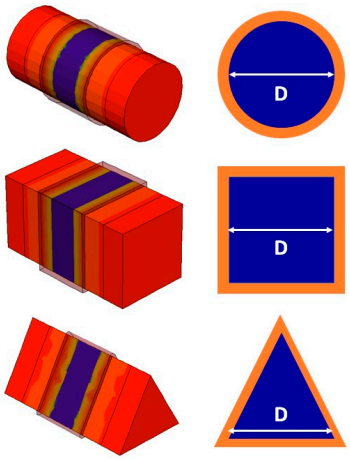

Figure 1. Schematic structure of GAA SNWTs with three cross-sectional shapes used in the simulation.

Table 1. Device parameters used in the simulation.

Device Parameter	Value
Gate length (nm)	12~28
Gate overlap length (nm)	0
Nanowire width (nm)	16
EOT (nm)	0.67
Channel doping concentration (cm^{-3})	1×10^{16}
Source/Drain extension doping concentration (cm^{-3})	5×10^{19}
Source/Drain doping concentration (cm^{-3})	1×10^{20}
Doping gradient (nm/dec)	1

2.2. Simulation Results

Figure 2a–c shows the trends of V_{th}, SS, and DIBL as a function of gate length in different cross-sectional GAA SNWTs. From Figure 2a, it can be noticed that the triangular devices have the lowest V_{th} roll-off, whether in the linear region or the saturation region. Here, the V_{th} values of long channel devices with three cross-sectional shapes differ from each other, which is mainly due to the different work functions of the gate material. For the triangular, circular, and square devices, they are 4.37 eV, 4.53 eV, and 4.60 eV, respectively. This is to maintain the same off-state current of 100 nA/μm when comparing the on-state current of short channel devices. In addition, it can also be found from Figure 2b,c that the triangular devices also have smaller DIBL and SS under the same gate length condition. Even for GAA SNWTs with the same linewidth of 16 nm, only the triangular devices can successfully reduce the gate length to 16 nm under the requirement of SS < 67mV/dec, which met IRDS 2017 requirements on the 5 nm technology node [8], as shown in Figure 2d. Additionally, compared to the worst quadrate GAA SNWTs, the gate length of triangular one is reduced by approximately 8 nm.

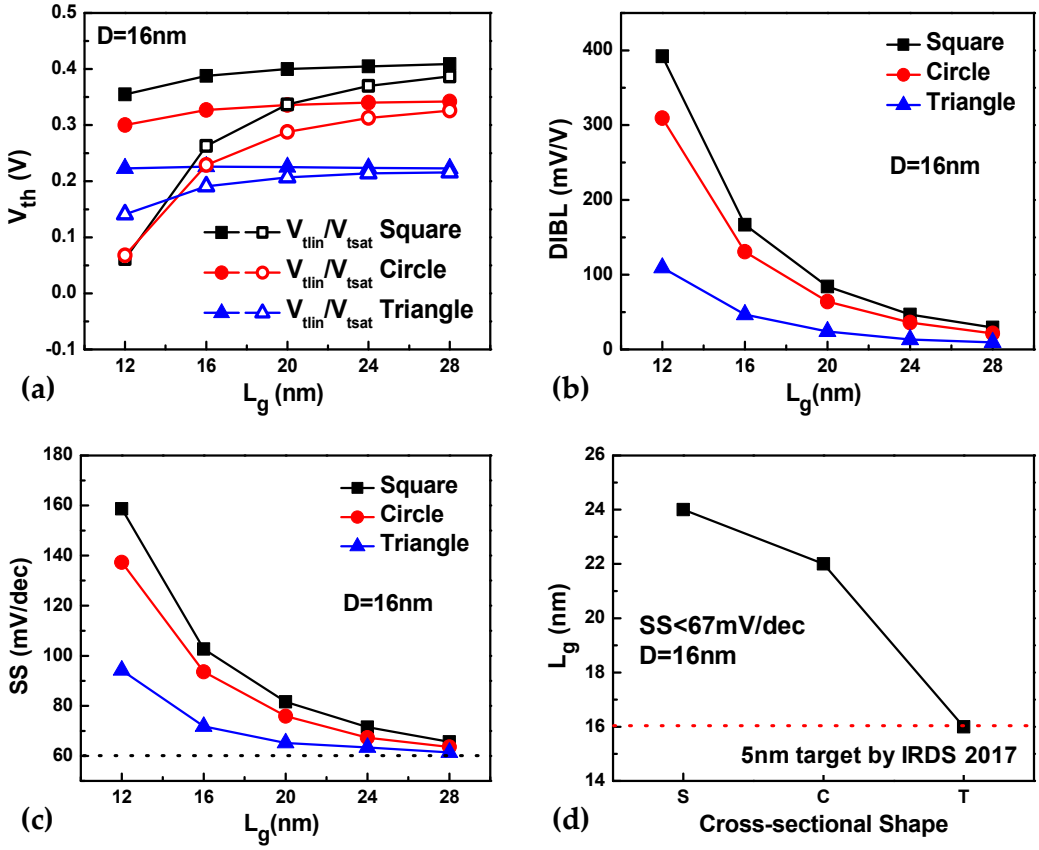

Figure 2. (**a**–**c**) The trend of V_{th}, SS, and DIBL for different cross-sectional shapes of GAA SNWTs as a function of gate length; (**d**) The ability to scale down GAA FETs with different cross-sections.

The electrostatic controllability and short channel effects affect not only static power consumption, but also driving capability. Given the fixed off-state current, SCE determines the threshold voltage level, which will impact the device's overdrive voltage—V_{gs}-V_{th}, and hence on-state current. Figure 3 shows the relationship between the off-state current and the on-state current for GAA SNWTs with three cross-sections under different gate length conditions. From Figure 3, it is noticed that the triangular devices have the best on/off ratio. Under the same off-state current of 100 nA/μm, due to better electrostatic control capability and SCE immunity, the triangular devices have a higher on-state current, reaching 940 μA/μm, which is nearly 10% higher than that of the circular devices, and nearly 36% higher than quadrate ones.

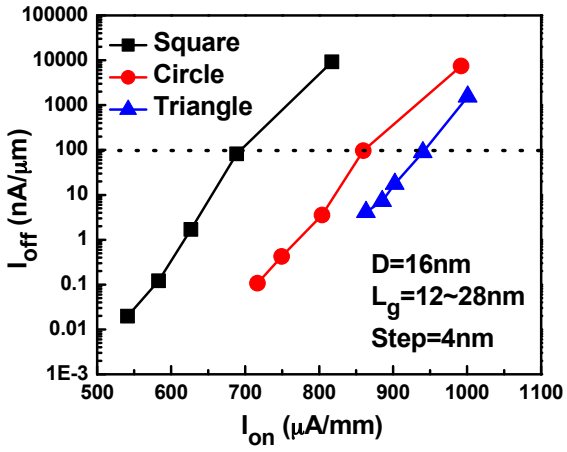

Figure 3. The relationship between the off-state and the on-state current of different cross-sectional GAA SNWTs with varying gate length.

2.3. Equivalent Model

In order to further investigate the advantages of triangular devices, we compared the trends of V_{th} and I_{on} with a cross-sectional area of different GAA SNWTs. From Figure 4, we can see that V_{th} and I_{on} have a linear correlation with the cross-sectional area, and are almost independent of cross-sectional shape, so the cross-sectional area is the root factor affecting the short channel effect of GAA SNWTs.

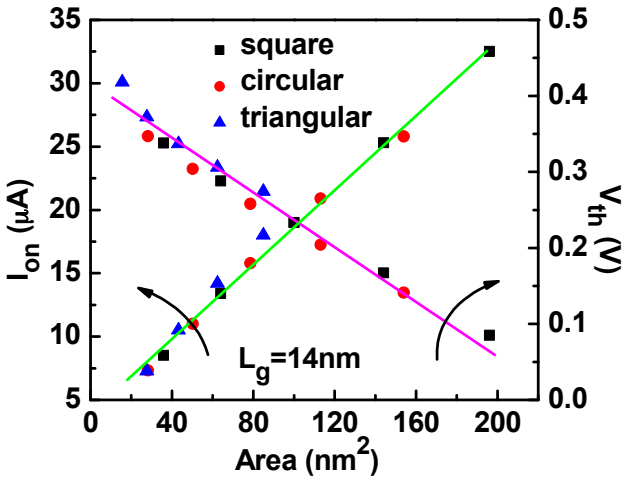

Figure 4. The trends of V_{th} and I_{on} with cross-sectional area in GAA SNWTs.

$$S_{square} = D^2,\ S_{circle} = \frac{\pi}{4}D^2,\ S_{triangle} = \frac{\sqrt{3}}{4}D^2 \quad (1)$$

For quadrate, circular, and triangular nanowire devices, the relationship between line width and cross-sectional area is shown in Equation (1). The triangular devices have the smallest cross-sectional area under the same line width condition, and thus have the strongest electrostatic control capability and can obtain the best device performance.

3. Experiments

According to the simulation results, triangular cross-sectional GAA SNWTs have superior SCE controllability compared to circular or quadrate ones, which makes them promising in a sub-5 nm node. However, another concern comes from the lack of a feasible method for forming such suspended silicon nanowire with an accurately controlled size and cross-sectional shape, which is quite critical to

the device variability suppression and mobility behavior. The existing works did not achieve either process variation suppression [10] or a precisely-controlled equilateral triangle [7,11], and also did not give the mobility characterization at a low temperature, which reflects the surface roughness scattering [12].

TMAH is the abbreviation for Tetramethylammonium Hydroxide, a kind of photoresist developer which was proven to be an excellent anisotropic si-etching solution. Therefore, we intended to the adopt TMAH wet etching technique to get the triangular nanowires, which can accurately control the size of nanowires and produce a nearly-equilateral triangle thanks to the extremely high anisotropic corrosion rate of (1 0 0) and (1 1 0) to (1 1 1) crystal plane by TMAH wet etching. Meanwhile, the wet etching technique can avoid surface damage induced by dry etching so that the channel mobility can be enhanced.

3.1. Key Process of Triangular Nanowire Formation

Owing to different atomic densities of crystal planes, the etching rate of TMAH on (1 1 1) is usually much smaller than that on (1 0 0) and (1 1 0), so the etching of TMAH can be self-stopped [13–15]. A schematic diagram of suspended triangular nanowires by TMAH wet etching is shown in Figure 5. This process can accurately control the size and shape of the silicon nanowires, which are formed from different initial line widths of the silicon Fin. The specific process flow is listed as follows:

1. Thermal oxidation to produce a silicon oxide buffer layer;
2. Chemical vapor deposition to produce silicon nitride as a hard mask layer;
3. Electron beam lithography and anisotropic dry etching to form a silicon nitride hard mask and silicon Fins;
4. Remove the native oxide on the silicon surface with a dilute hydrofluoric acid solution at room temperature;
5. Anisotropic wet etching silicon Fins at 35 °C and in 25% TMAH solution, so triangular silicon nanowires are formed under the silicon nitride hard mask, while the silicon substrate will also be etched to form a triangle;
6. Remove silicon nitride hard mask by 170 °C phosphoric acid;
7. Remove the silicon oxide buffer layer by diluted hydrofluoric acid at room temperature, and the triangular suspended silicon nanowires are achieved.

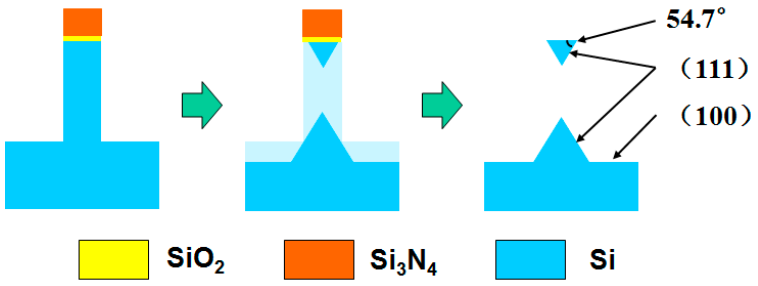

Figure 5. The diagram of triangular suspended nanowire by TMAH.

When the TMAH solution etches the side of the silicon Fin, the etching window is determined by the top silicon nitride hard mask and the bottom corners of silicon Fin. If the silicon Fins have a sufficient height and long enough etching time, both sides of the silicon Fins will be completely etched and lead to punch-through, an inverted triangular silicon nanowire will be formed under the silicon nitride hard mask, and a triangle bump on the silicon substrate will be simultaneously formed, as shown in Figure 5. At this time, the side surfaces formed by the wet etching are all (1 1 1) crystal planes, presenting an angle of 54.7° with the (1 0 0) crystal plane of the surface.

Figure 6 illustrates the SEM images of different TMAH etching times of the triangular device, and it is noted that even if the over-etching time has exceeded 10 s (over-etching time exceeds 50%) in Figure 6c, the width and cross section of the silicon nanowires remain basically the same, and only the sharp corners are slightly etched, indicating that the TMAH etching technology has the strong capability to suppress cross section fluctuations.

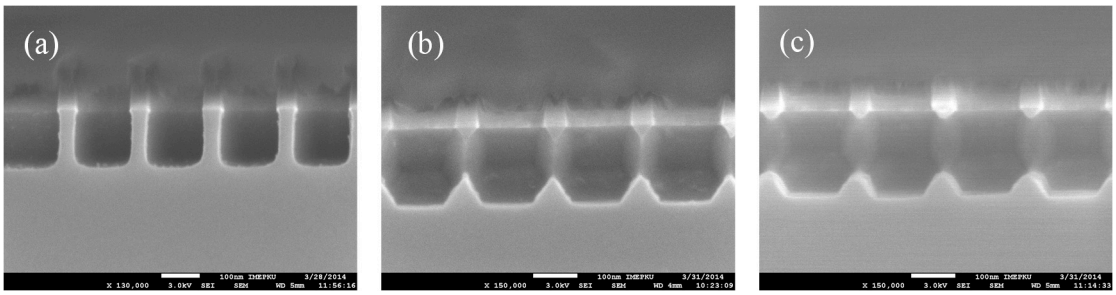

Figure 6. 35 °C, 25% TMAH solution is used to etch a silicon Fin with a 50 nm width. The SEM images obtained after different etching times (**a**–**c**): 0 s/20 s/30 s.

3.2. Fabrication of GAA SNWT with Triangular Cross Section

Based on the above analysis, we adopted the TMAH wet etching technique to fabricate a P-type inverted triangular cross-sectional GAA FET on a bulk-si substrate, as shown in Figure 7. The process flow is given as follows:

1. Channel Engineering

- thermal oxidation on a bulk silicon substrate to produce a silicon oxide buffer layer;
- chemical vapor deposition to produce a silicon nitride hard mask layer;
- optical lithography, anisotropic dry etching, and oxidation to produce LOCOS isolation, and active regions are achieved;
- chemical vapor deposition to produce a polysilicon hard mask layer;
- electron beam lithography and anisotropic dry etching to produce a polysilicon hard mask;
- electron beam lithography and anisotropic dry etching to form a silicon nitride hard mask and Si Fins;
- remove the native oxide on the silicon surface by the diluted hydrofluoric acid solution at room temperature;
- Si Fin anisotropic wet etching by TMAH solution to form inverted triangular nanowires under the silicon nitride hard mask;
- high-energy ion implantation is performed on the active region to generate N− doping as an N− well of PMOS;
- low-energy ion implantation is performed on the active region, and only the exposed area in the trench can generate N+ doping, preventing the bottom parasitic transistor from turning on;
- remove the silicon nitride hard mask and the silicon oxide buffer layer by phosphoric acid and diluted hydrofluoric acid, and suspended silicon nanowires are obtained;
- sacrificial oxidation to round the corner of triangular nanowires;
- remove sacrificial oxide by diluted hydrofluoric at room temperature;

2. Gate Engineering

- thermal oxidation to produce gate oxide;
- chemical vapor deposition to generate a polysilicon gate material layer;

- polysilicon gate ion implantation and rapid thermal annealing;
- electron beam lithography and anisotropic dry etching to produce the polysilicon gate;

3. Source and drain Engineering

- high-dose implantation is performed on large fan-out regions of source and drain, followed by rapid thermal annealing;
- chemical vapor deposition to produce the isolation layer;
- optical lithography and dry etching to form the contact holes;
- metal contacts and interconnections formation.

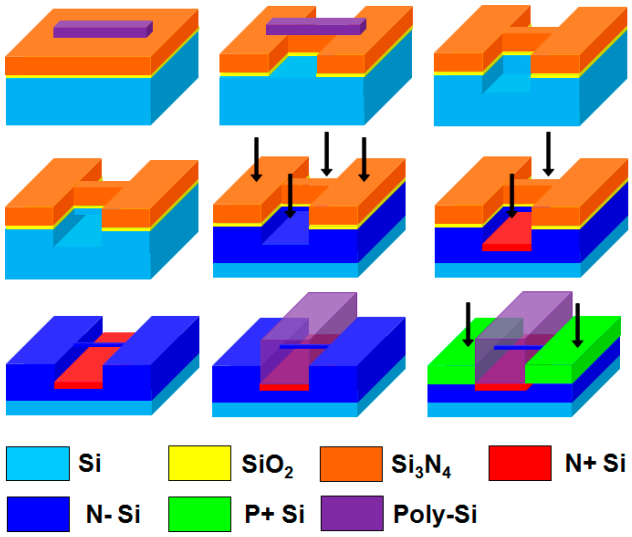

Figure 7. Process for fabricating P-type GAA SNWT by the TMAH wet etching technique on a bulk silicon substrate.

There is a bottom parasitic transistor below the silicon nanowire device, and we need to effectively suppress it. A common practice is to insert an isolation layer between the gate material and the parasitic transistor, but chemical planar polishing (CMP) equipment is required to complete the planarization treatment. Due to the lack of CMP, high-dose implantation in the trench is used here, which can greatly increase the channel doping concentration and the threshold voltage of the parasitic transistor, thereby preventing it from turning on. The silicon nanowire channel can still maintain a low doping concentration due to the protection of the silicon nitride hard mask. After the suspended silicon nanowires are formed, the triangular silicon nanowires are sacrificially oxidized slightly to make their sharp corners round, avoiding the reliability issues of the device.

4. Device Characteristics

Figure 8a is an SEM image of multiple suspended silicon nanowires formed by the TMAH wet etching technique. Each silicon nanowire has good uniformity. Figure 8b is a TEM cross-sectional view of the silicon nanowire after the gate oxidation process and gate material deposition, which turned out to be an inverted triangle, and the angle between the self-stopped (1 1 1) and the surface crystal plane is close to the theoretical 54.7°, almost reaching an equilateral triangle apex.

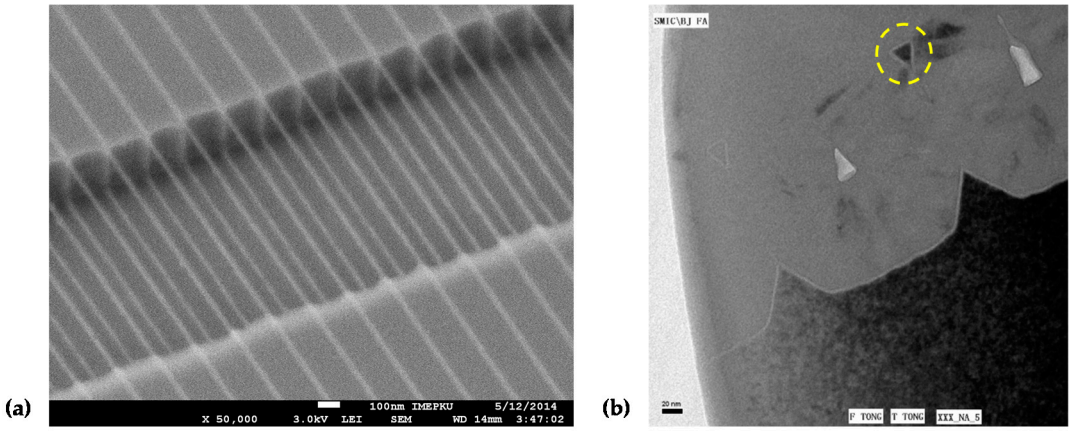

Figure 8. (**a**) SEM image of multiple suspended silicon nanowires formed by TMAH etching; (**b**) TEM image of silicon nanowires after gate oxidation and polysilicon gate deposition.

Figure 9a,b shows the transfer and output characteristics of a P-type GAA SNWT with a triangular cross section. The nanowire had a line width of 20 nm and a gate length of 140 nm. Under a bias voltage of 1.0 V, the on-state current normalized by the line width reached 1402 μA/μm, the leakage current was limited to 0.4 nA/μm, and the on/off ratio exceeded 10^6. Furthermore, the device had a low subthreshold slope of 85 mV/dec and DIBL of 63 mV/V.

Figure 10 illustrates the trends of subthreshold slope, DIBL, and threshold voltage with different gate lengths for the triangular GAA SNWTs. From Figure 10a, it can be found that the subthreshold slope remained almost constant as the gate length decreased, while the DIBL increased slightly. The reason why DIBL degraded with the gate length scaling more obviously is that the polysilicon gate overlapped the trench, resulting in the device's source and drain extension regions not being a nanowire structure, but the traditional planar structure. Hence, the high level drain voltage can impose a greater influence on the channel potential. In Figure 10b, the threshold voltage of the triangular GAA SNWTs in the linear and saturated region is almost constant as the gate length is varying, indicating that it had an excellent SCE suppressing capability.

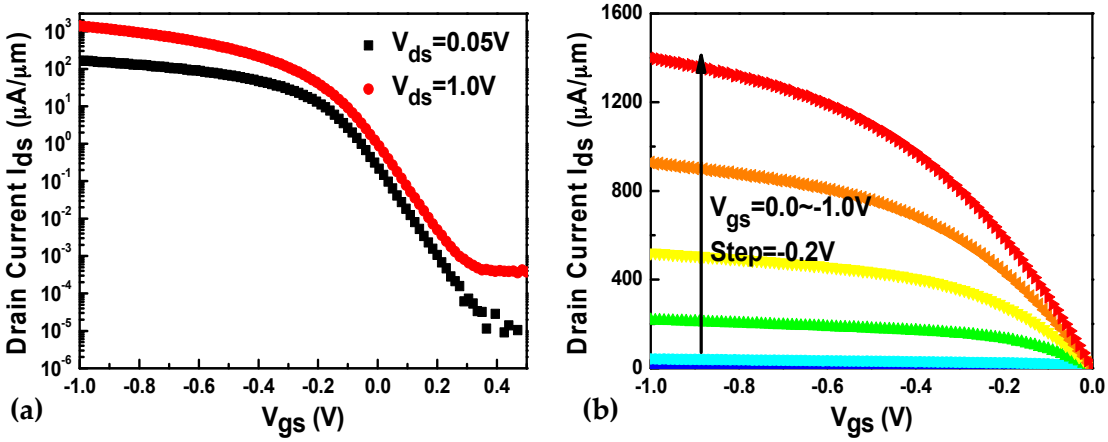

Figure 9. (**a**) Transfer characteristic; (**b**) output characteristic of P-type triangular GAA SNWT with D = 20 nm and L_g = 140 nm.

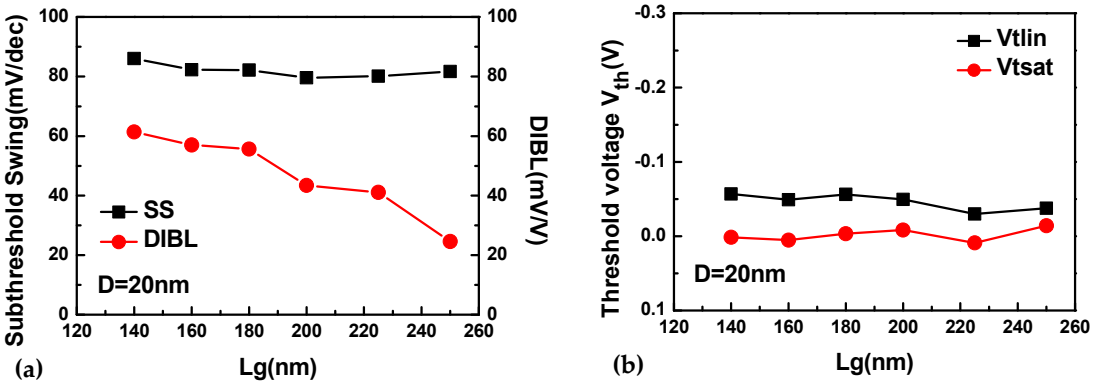

Figure 10. The trends of SS, DIBL, and V_{th} with L_g for triangular cross-sectional GAA SNWTs.

5. Mobility Model

In this section, we plan to characterize the carrier mobility in the fabricated GAA SNWTs by Bias-Temperature experiments so that surface roughness mobility can be obtained at a low temperature, which can verify the benefit to mobility resulting from the stable and smooth triangular cross-sectional shape.

The Y-function method can be used to extract the mobility of the fabricated triangular cross-sectional GAA SNWTs [16]. The Y function can be calculated as follows:

$$Y \equiv \frac{I_{ds}}{\sqrt{g_m}} = \sqrt{k_0 V_{ds}}(V_{gs} - V_{th}), \quad (2)$$

Here, k_0 is given by

$$k_0 = \frac{W_{eff}\mu C_{ox}}{L_{eff}}, \quad (3)$$

Firstly, the driving current I_{ds} and the transconductance g_m of the GAA SNWTs in the linear region were measured to obtain the Y function, and then the intercept of this straight line at the x-axis was the threshold voltage V_{th} and the mobility of the device was extracted by the slope k_0. This method can be adopted to extract the trends of mobility varying with temperature, as shown in Figure 11a.

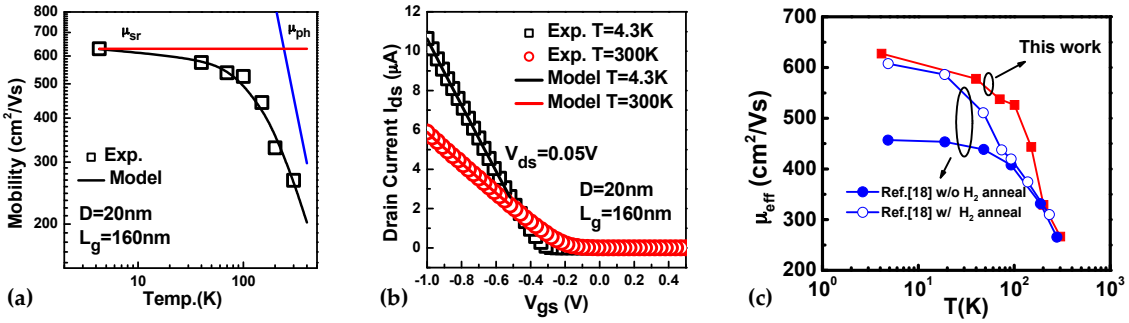

Figure 11. (**a**) The trend of mobility with temperature in GAA SNWTs; (**b**) comparison of current simulation results with experimental results of GAA SNWT at T = 4.3 K and 300 K, respectively; (**c**) effective electron mobility as a function of temperature for triangular GAA SNWT achieved by TMAH wet etching and quadrate SNWT with/without H_2 annealing.

It is noticed that the mobility is mainly determined by phonon scattering at room temperature, and the surface roughness scattering dominantly contributed to mobility when the temperature dropped below 70 K. Additionally, the Coulomb scattering had little effect on the mobility over the entire

temperature range because of the lower channel doping of the GAA SNWTs. Here, three kinds of mobility can be obtained by the following equations:

$$\frac{1}{\mu} = \frac{1}{\mu_{sr}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{coulomb}}, \tag{4}$$

$$\mu_{ph} = AT^{-\alpha}, \tag{5}$$

$$\mu_{Coulomb} = BT^{\alpha}, \tag{6}$$

Here, μ_{sr}, μ_{ph}, and $\mu_{Coulomb}$ denote the surface roughness mobility, the phonon scattering mobility, and the Coulomb scattering mobility, respectively. A and B are fitting coefficients, and α is the temperature coefficient. According to the scattering theory [17], α is set to 1.5. From Figure 11a, it can be seen that the modelling results can fit the experimental data quite well. The three fitting coefficients are μ_{sr} = 629 cm^2/Vs, A = 2.38 × 10^6 $cm^2K^{1.5}/Vs$, and B = 2.42 × 10^6 $cm^2/K^{1.5}Vs$. As shown in Figure 11b, the device current in the linear region at two different temperatures was calculated using the mobility obtained by this model, and the modelling results are also in good agreement with the experimental results. It is worth mentioning that the mobility in our work is higher than that in GAA SNWTs with or without H_2 annealing [18] in Figure 11c, indicating that the inverted triangle cross section achieved by TMAH wet etching can effectively reduce the influence of surface roughness scattering.

6. Conclusions

We demonstrated a gate-all-around silicon nanowire transistor (GAA SNWT) with a triangular cross section by simulation and experiments. Through three-dimensional simulation tool Sentaurus, it was found that with the same nanowire width, the triangular cross-sectional SNWT exhibited the lowest subthreshold swing, the highest on/off ratio, and the most excellent SCE immunity compared with the circular and quadrate ones, which may be attributed to the smallest equivalent distance from the nanowire center to the surface in triangular SNWTs. Then, P-type triangular GAA SNWTs with L_g = 140 nm and D = 20 nm were fabricated by the TMAH wet etching technique. Thanks to the anisotropic etching rate of the TMAH solution, a self-stopped etching behavior on a (1 1 1) crystal plane can be achieved, ensuring the accurately controlled size and cross-sectional shape of the channel. Finally, we measured and modelled the carrier mobility of fabricated devices with varying temperatures so as to extract the surface roughness mobility of 629 cm^2/Vs, confirming the benefit of a stable and smooth cross section obtained by TMAH treatment.

Author Contributions: Conceptualization, M.L.; Methodology, M.L.; Software, G.C.; Formal Analysis, M.L. and G.C.; Data Curation, G.C.; Writing—Original Draft Preparation, G.C.; Writing—Review & Editing, M.L.; Project Administration, M.L. and R.H.

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Conflicts of Interest: The authors declare no conflict of interest.

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