



Article Enhanced Pathological Element-Based Symbolic Nodal Analysis

Sujito ^{1,2}, Huu-Duy Tran ³, Yueh-Ling Lin ¹, Cong Chuan Pham ¹, Hung-Yu Wang ^{1,4,*} and Shun-Hsyung Chang ¹

- ¹ National Kaohsiung University of Science and Technology, Kaohsiung 807, Taiwan; sujito.ft@um.ac.id (S.); lingling@mail.wzu.edu.tw (Y.-L.L.); phamcongchuan88@gmail.com (C.C.P.); stephenshchang@me.com (S.-H.C.)
- ² Department of Electrical Engineering, Faculty of Engineering, State University of Malang, Malang 65145, Indonesia
- ³ Department of Physics, University of Dalat, Dalat City 670000, Vietnam; duyth@dlu.edu.vn
- ⁴ Graduate Institute of Clinical Medicine, Kaohsiung Medical University, Kaohsiung 807, Taiwan
- * Correspondence: hywang@nkust.edu.tw; Tel.: +886-911-623-509

Received: 16 November 2018; Accepted: 22 December 2018; Published: 27 December 2018



Abstract: An improved symbolic analysis procedure to enhance the analytic efficiency of the reported symbolic nodal analysis is presented. Two techniques are adopted in the proposed method to reduce the order of the system of equations when performing symbolic analysis. The first one uses voltage signal sources directly to perform symbolic analysis without replacing them with their nullor equivalences. The second one uses the nullor, grounded mirror, and floating mirror elements to model the active devices that involve differential or multiple single-ended signals. Practical examples are given which demonstrate the feasibility of the proposed methods.

Keywords: pathological element; floating mirror; symbolic nodal analysis

1. Introduction

Nullor and mirror pathological elements have been proven to be very valuable components for network analysis, synthesis and design [1–13]. The main reasons for the popularity of the nullor elements are their ability to model active circuits independently of the particular realization of the active devices. The symbolic circuit analysis can be carried out by only applying nodal analysis (NA). The pathological grounded voltage mirror (VM) and current mirror (CM) were defined in 1999 [14]. They can be used to represent active devices with current or voltage reversing properties in concise circuit structures compared to their nullor-equivalent counterparts. The grounded mirror (GM) elements have been further extended to include the floating mirror (FM) elements [15]. The FM elements were used to derive pathological sections to ideally represent various popular analog signal processing properties that involve differential or multiple single-ended signals. Therefore, many new active devices with such characteristics can be modeled using nullor-grounded mirror-floating mirror (NGMFM) elements in more compact forms compared with their grounded pathological equivalences [15–21].

The symbolic NA using RLC-grounded pathological equivalences instead of their RLC-nullor representations of circuits was presented in [20] and computational algorithm was reported in reference [21]. With a smaller number of nodal equations compared to previous method [22], it achieves a considerable reduction in the order of the system of equations and in the generation of nonzero coefficients into the nodal admittance matrix. As a result, the computational complexity during the solution of the system of equations is reduced. However, a limitation of the formulation methods in

references [20,21] is that the floating pathological elements cannot be included into the formulation process. Thus the compact NGMFM equivalent circuits cannot be used for NA. Some attention had been paid to the finding of nullor-grounded mirror (NGM) equivalences of the popular active devices with differential or multiple single-ended signal properties [23] and the addition of extra equations during performing symbolic NA [24]. Nevertheless, both approaches incur the increment on the order of the built nodal admittance matrices which complicate their solution process. Besides, in all of the symbolic NA articles in literature, the voltage signal sources are replaced by their nullor equivalences before applying NA.

In this paper, a systematic analytical procedure is proposed that performs efficient NA by using lower-complexity RLC-NGMFM networks. This proposed method makes good use of the compactness of floating mirror models and treats input voltage signal source as a grounded norator to avoid using its equivalent circuit. The effect on the reduction of the order of the system of equations matrix when performing symbolic NA is demonstrated by practical examples.

2. Pathological Section-Based Active Device Model

The definition of nullor, GM, and FM elements are shown in Figure 1. Despite the GMs being two-port network elements, they can be used as two terminal bi-directional elements with the reference node unused [10]. The GM elements in Figure 1c,e are respectively the special cases of their floating counterparts in Figure 1d,g. It can also be found that the grounded and floating two-output CMs in Figure 1f,h are simple extensions of the structures in Figure 1e,g, respectively. Figure 2 shows some pathological FM sections which represent analog signal processing properties involving differential or multiple single-ended signals. Figure 2a–d have been reported in reference [15]. The structure in Figure 2e is constructed by the floating two-output CM in Figure 1h for modeling the active devices with more current outputs. The sections in Figure 2a,b are called "floating VM sections" for the remainder of this article. The modelling of active devices using NGMFM elements was proposed in references [15–17]. In comparison with their representations using only nullor elements [18] or NGM elements [20,21,23], the NGMFM representations which have a smaller node count are more concise. In references [15–17], additional dummy pathological elements are added to the pathological representations of the balanced output second generation current conveyor (BOCCII), balanced output inverting second generation current conveyor (BOICCII), fully differential second generation current conveyor (FDCCII), double output CCII with two Z- outputs (DOCCII-), differential voltage current conveyor with a Z+ output terminal (DVCC+) and differential voltage current conveyor with a Zoutput terminal (DVCC-) to constitute complete sets of pathological pairs. However, the dummy pathological elements are not needed since each unknown terminal voltage (or branch current) can be obtained from other known terminal voltage(s) (or branch current(s)) according to the element properties. Figure 3 shows the modified NGMFM models of some aforementioned active devices and differential difference current conveyor (DDCC). All voltages and currents of the terminals of the active models in Figure 3 are still uniquely and definitely determined when performing NA since they result in the same number of removed unknown variables and nodal equations by using the proposed symbolic NA method in Section 3.

(a) Nullator	$V_1 \stackrel{I_1}{\bullet \bullet}$		$V_1 = V_2$ $I_1 = I_2 = 0$
(b) Norator	$V_1 \stackrel{I_1}{\bullet \bullet}$		V_1 and V_2 are arbitrary $I_1 = -I_2 =$ arbitrary
(c) Grounded VM	$V_1 \stackrel{I_1}{\longleftrightarrow}$		$V_2 \qquad V_1 = -V_2 \\ I_1 = I_2 = 0$
(d) Floating VM	I_1 $V_1 \Leftrightarrow$	$V_0 $	$V_{2} \qquad \begin{array}{c} V_{10} = -V_{20} \\ (V_{1} - V_{0} = V_{0} - V_{2}) \\ I_{1} = I_{2} = I_{0} = 0 \end{array}$
(e) Grounded CM	$V_1 \stackrel{I_1}{\longleftrightarrow}$	<u> </u>	V_2 V ₁ and V ₂ are arbitrary I ₁ = I ₂ = arbitrary
(f) Grounded two-outpu CM	$\begin{matrix} \mathbf{I}_1 \\ \mathbf{V}_1 \blacklozenge$		V_1, V_2 and V_3 are arbitrary $I_1 = I_2 = I_3 =$ arbitrary
(g) Floating CM	$V_1 \stackrel{I_1}{\bullet \bullet}$		V_2 V_{10} and V_{20} are arbitrary $I_1 = I_2 = I_0/2 = $ arbitrary
(h) Floating two-output CM	$V_1 \bullet \bullet$	$V_{3} \bullet I_{3} I_{2}$ $V_{0} \bullet I_{0}$	V_{2} V_{2} V_{2} V_{2} $V_{1} = I_{2} = I_{3} = I_{0}/3 = \text{arbitrary}$

Figure 1. Symbols and definitions of nullor and mirror elements.

(a) Differential voltage cell	$ \begin{array}{c} w \bullet \bullet \bullet \\ I_w \\ x \bullet \bullet \bullet \\ I_x \\ I_x \\ I_y \end{array} $	$V_y = V_w - V_x$ $I_w = I_x = I_y = 0$
(b) Differential voltage conveying cell	$w \xrightarrow{I_{w}} Z$ $I_{w} \xrightarrow{I_{z}} Y$ $x \xrightarrow{I_{x}} V$	$V_w - V_x = V_y - V_z$ $I_w = I_x = I_y = I_z = 0$
(c) Current replication cell	$a \underbrace{I_{a}}_{I_{a}} \underbrace{I_{c}}_{I_{c}} c$	$I_a = -I_b = I_c = I_m/2$
(d) Current replication cell	$a \bigoplus_{I_a} \bigoplus_{I_m} I_d d$ $b \bigoplus_{I_b} \bigcup_{I_c} I_c c$	$I_{a} = I_{d} = -I_{b} = -I_{c} = I_{m}/2$
(e) Ccurrent replication cell	$a \xrightarrow{I_a} \bigcup_{I_b} I_c c$ $x \xrightarrow{I_a} \bigcup_{I_y} I_z$	$I_a = I_b = I_c$ = -I_x = -I_y = -I_z = I_m/3

Figure 2. FM sections and their characteristics.

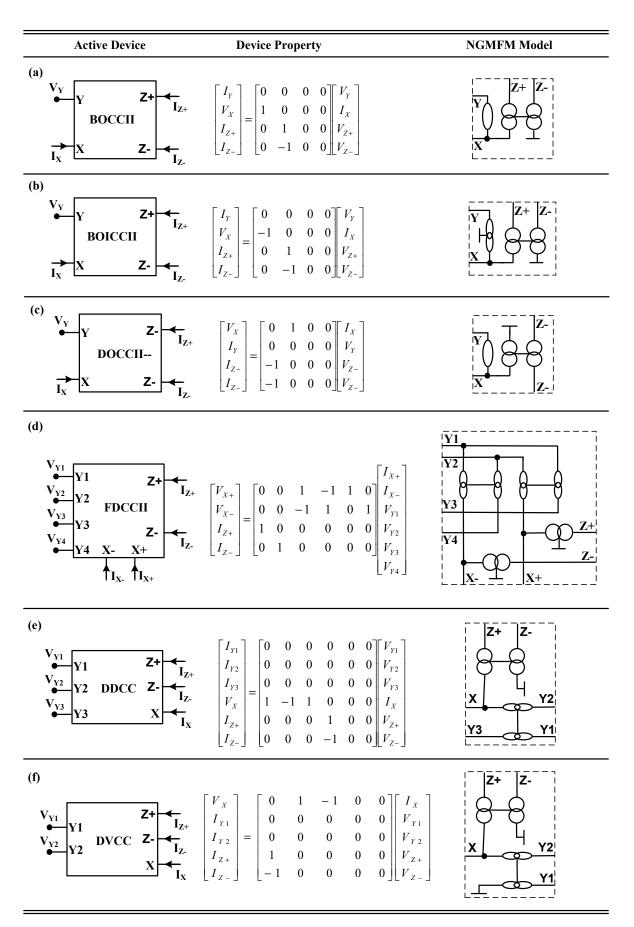


Figure 3. Symbol and NGMFM models of some active devices.

3. Symbolic NA of RLC-NGMFM Network

To perform symbolic NA on the RLC–NGMFM networks, the analytic steps in reference [20] are modified as below.

- Step 1: For the symbolic NA of an arbitrary interconnection of RLC–NGMFM networks with (N + 1) nodes (excluding the reference nodes between two mirror elements since we do not particularly wish to know the voltages of these reference nodes), select a ground node and label all other nodes from 1 to N. Mark the directions of current flow through each of norators, CMs, current replication cells and input voltage signal sources to build nodal equations.
- Step 2: Write the nodal admittance equations for each labeled node in matrix form as

$$\mathbf{I} = \mathbf{Y}_{N \times N} \, \mathbf{V} \tag{1}$$

I = { $I_1, I_2, ..., I_N$ }', where the *i*th component I_i is defined as the sum of the currents flowing into the *i*th node from the independent current sources, input voltage signal sources, norators, grounded CMs, or current replication cells. **Y**_{N × N} is the passive nodal admittance matrix. **V** is the unknown column vector { $V_1, V_2, ..., V_N$ }' of node voltages. It must be noted that the voltage of the node connected to input voltage signal source is regarded as an unknown voltage variable in this step.

- Step 3: For a norator that is connected between nodes *l* and *m*, for example, add the equation in row *m* to the equation in row *l* and delete row *m* of the nodal equations. This involves adding the *m*th row of **Y** to the *l*th row of **Y**. If *m* is the ground node, simply delete row *l* of the nodal equations. The number of rows of the **Y** matrix is thereby reduced by one. This operation is the same as supernode. Since the characteristic of an input voltage signal source is similar to a grounded norator, the treatment of each input voltage signal source is the same as a grounded norator.
- Step 4: For a grounded CM that is connected between the nodes e and f, for example, subtract the equation in row e from the equation in row f and delete row e of the nodal equations. This involves subtracting the eth row of **Y** from the fth row of Y. If e is the ground node, simply delete row f of the nodal equations. A similar manipulation process can be applied to grounded two-output CM. For a grounded two-output CM connected between the nodes e, f and g (none is grounded), subtract the equation in row e from the equation in row f, and subtract the equation in row e from the equation in row g and delete row e of the nodal equations. If one of the three nodes is grounded, this grounded two-output CM can be regarded as a grounded CM connected between two ungrounded nodes. One grounded CM (or grounded two-output CM) incurs the deletion of one row of the **Y** matrix. This operation is based on the similar properties of a grounded CM and a norator.
- Step 5: For a nullator that is connected between the nodes p and q, for example, add the elements of column q to the elements of column p and delete column q of **Y**. The reason is that $V_p = V_q$ so one unknown voltage variable can be omitted. If q is the ground node, simply delete column p of **Y**. The number of columns of the **Y** matrix is thereby reduced by one.
- Step 6: For a grounded VM that is connected between the nodes *r* and *s*, for example, subtract the elements of column *s* from the elements of column *r* and delete column *s* of **Y**. If *s* is the ground node, simply delete column *r* of **Y**. The number of columns of the **Y** matrix is thereby reduced by one. This operation is based on the similar properties of a grounded VM and a nullator.
- Step 7: For the differential voltage conveying cell in Figure 2b that is connected between the nodes w, x, y and z terminals, select the ungrounded node w, for example, then add the elements of column w to the elements of column x, add the elements of column w to the elements of column y and subtract the elements of column w from the elements of column z and then delete column w of **Y**. This operation is based on the voltage property ($V_w = V_x + V_y V_z$) of the differential voltage conveying cell. For the differential voltage cell in Figure 2a with voltage property

6 of 12

 $(V_w = V \text{ textsubscriptx} + V_y)$, the operation is similar to a differential voltage conveying cell except the discard of column *z* operation. It must be noted that each of floating VM sections incur the deletion of one column of **Y** matrix.

- Step 8: For the pathological current replication cell in Figure 2d that is connected between the nodes *a*, *b*, *c* and *d* terminals, for example, add the equation in row *a* to the equation in row *b*, add the equation in row *a* to the equation in row *a* and delete row *a* of the nodal equations. The above operation is based on the current property ($I_a = I_d = -I_b = -I_c$) of a current replication cell. A similar manipulation process can also be applied to the current replication cells in Figure 2c,e. It must be noted that each current replication cell in Figure 2c–e will incur the deletion of one row of **Y** matrix.
- Step 9: Move the terms of node voltages connected to input voltage signal sources in matrix V of (1) into matrix I of (1) since they are known variables. Then a square nodal admittance matrix can be obtained. The equations can be solved to obtain a unique solution for each unknown voltage variable.

4. Application Examples

To demonstrate the usage of the presented symbolic NA method and the proposed active models, three circuit examples are given below. Considering the FDCCII-based current-mode biquad in Figure 2 of reference [25], its NGMFM equivalence is given in Figure 4. The multiple-output FDCCII model is derived from the model in Figure 3d by replacing the CMs with the grounded two-output CM in Figure 1f and the current replication cell with seven outputs (the extended version of current replication cell in Figure 2e). Based on the steps 1–2 in Section 3, the nodal admittance equations in matrix form can be obtained as:

$$\begin{bmatrix} I_2 + I_{C2} - I_{C1} \\ I_3 + I_{C2} \\ -I_{C1} \\ -I_{C2} \end{bmatrix} = \begin{bmatrix} sC_2 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$
(2)

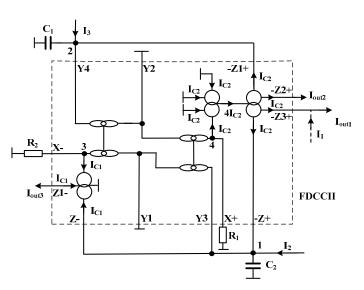


Figure 4. FDCCII-based current-mode biquad in Figure 2 of [23].

By applying the 3th to 4th steps of the proposed analytic procedure, as given by (3), one equation has been removed since one grounded two-output CM incurs the deletion of one row. Applying the 5th to 7th steps, two unknown voltage variables have been removed since each differential cell incurs the deletion of two columns of the nodal admittance matrix, as given by (4).

$$\begin{bmatrix} I_2 + I_{C2} \\ I_3 + I_{C2} \\ -I_{C2} \end{bmatrix} = \begin{bmatrix} sC_2 & 0 & -G_2 & 0 \\ 0 & sC_1 & 0 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$
(3)

$$\begin{bmatrix} I_2 + I_{C2} \\ I_3 + I_{C2} \\ -I_{C2} \end{bmatrix} = \begin{bmatrix} sC_2 & -G_2 \\ 0 & sC_1 \\ G_1 & 0 \end{bmatrix} \begin{bmatrix} V_{1,4} \\ V_{2,3} \end{bmatrix}$$
(4)

After applying the 8th step, the nodal admittance matrix equations are obtained as (5). The current replication cell in Figure 4 incurs the deletion of one equation. By solving (5), we can obtain the outputted currents as (6)–(8).

$$\begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} sC_2 + G_1 & -G_2 \\ G_1 & sC_1 \end{bmatrix} \begin{bmatrix} V_{1,4} \\ V_{2,3} \end{bmatrix}$$
(5)

$$I_{out2} = I_{C2} = -G_1 V_4 = \frac{-I_2 s C_1 G_1 - I_3 G_1 G_2}{s^2 C_1 C_2 + s C_1 G_1 + G_1 G_2}$$
(6)

$$I_{out1} = I_1 + I_{C2} = I_1 - G_1 V_4 = \frac{\left[I_1(s^2 C_1 C_2 + s C_1 G_1 + G_1 G_2) - I_2(s C_1 G_1) - I_3 G_1 G_2\right]}{s^2 C_1 C_2 + s C_1 G_1 + G_1 G_2}$$
(7)

$$I_{out3} = -I_{C1} = G_2 V_3 = \frac{-I_2(G_1 G_2) + I_3(sC_2 G_2 + G_1 G_2)}{s^2 C_1 C_2 + sC_1 G_1 + G_1 G_2}$$
(8)

The results are in according with the expressions in Equations (10)–(12) of [25], so the validity of the proposed method is confirmed.

The second application example, which takes into account the DDCC+-based filter in Figure 2a of [26], is a voltage-mode filter. Figure 5 depicts its NGMFM equivalence using the DDCC model in Figure 3e with omission of duplicated current at Z- terminal. According to steps 1–2 in Section 3 of the proposed method, the nodal admittance equations in matrix form can be obtained as (9).

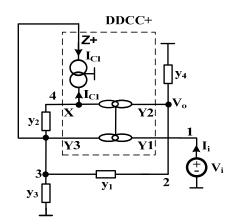


Figure 5. DDCC+-based voltage-mode filter in Figure 2(a) of [24].

Applying steps 3 and 4 respectively incur the deletion of one equation, so (9) becomes (10). Based on steps 5–8, the nodal admittance equations can be obtained as (11) because of the voltage property ($V_4 = V_3 - V_2 + V_1$) of the DDCC+. By applying step 9, the square nodal admittance matrix can be obtained, as given by (12). Thus the transfer function is computed from (12) and given by (13). The analyzed results are consistent with the expressions in Equation (11) of [26].

7 of 12

Appl. Sci. 2019, 9, 93

$$\begin{bmatrix} I_i \\ 0 \\ -I_{C1} \\ -I_{C1} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & y_1 + y_4 & -y_1 & 0 \\ 0 & -y_1 & y_1 + y_2 + y_3 & -y_2 \\ 0 & 0 & -y_2 & y_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$
(9)

$$\begin{bmatrix} 0\\0 \end{bmatrix} = \begin{bmatrix} 0 & y_1 + y_4 & -y_1 & 0\\ 0 & -y_1 & y_1 + 2y_2 + y_3 & -2y_2 \end{bmatrix} \begin{bmatrix} V_1\\V_2\\V_3\\V_4 \end{bmatrix}$$
(10)

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & y_1 + y_4 & -y_1 \\ -2y_2 & -y_1 + 2y_2 & y_1 + y_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$
(11)

$$\begin{bmatrix} 0\\ 2y_2V_1 \end{bmatrix} = \begin{bmatrix} y_1 + y_4 & -y_1\\ -y_1 + 2y_2 & y_1 + y_3 \end{bmatrix} \begin{bmatrix} V_2\\ V_3 \end{bmatrix}$$
(12)

$$\frac{V_2}{V_1} = \frac{V_o}{V_i} = \frac{2y_1y_2}{2y_1y_2 + y_1y_3 + y_1y_4 + y_3y_4}$$
(13)

To show the benefit of the proposed method, the formulation methods in references [18,20,23,24] are applied to the circuit in Figure 5. It can be found that both the DDCC+ equivalent nullor model in [18] and the DDCC+ equivalent NGM model in Figure 5 of reference [23] are more complicated (with a larger node count) compared to its NGMFM model. For the method in reference [24], the NGMFM active models are used. But the dimension of the admittance matrix is increased because additional equations may be added during its formulation process. Comparisons between the sizes of admittance matrix and the generation of nonzero coefficients based on different formulation methods are summarized in Table 1. We can see that by applying the formulation method described in Section 3, both the size of the admittance matrix and the count of non-zero coefficients are smaller than those generated with other formulation methods. Therefore, the proposed method achieves a more efficient symbolic NA.

Formulation Method	Admittance Matrix Size	Non-Zero Coefficients
Symbolic NA using NGM model [18]	5 imes 5	13
Symbolic NA using NGM model [20,23]	5×5	14
Symbolic NA using NGMFM model [24]	4 imes 4	10
Proposed method using NGMFM model	2×2	4

Table 1. Comparison of different formulation methods.

The third example considers the fully differential amplifier circuit in Figure 14 of reference [27]. To calculate the differential-mode output (V_{Od}) and common-mode output (V_{Oc}), the active device FDCCII is modeled by its NGMFM equivalent and the circuits are depicted in Figure 6a,b, respectively. The input and output voltages are defined as below.

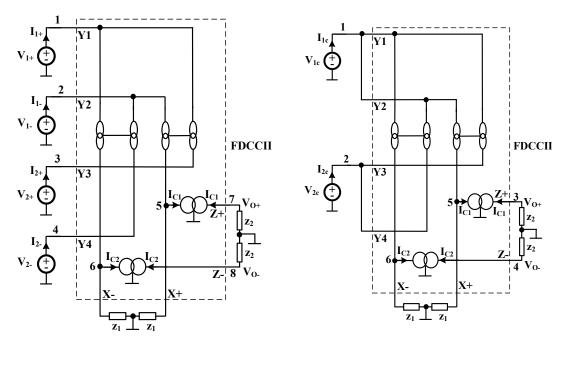
$$V_{id} = \frac{1}{2}(V_{i+} - V_{i-})$$

$$V_{ic} = \frac{1}{2}(V_{i+} + V_{i-}) \ (i = 1, 2)$$
(14)

$$V_{Od} = \frac{1}{2}(V_{O+} - V_{O-})$$

$$V_{Oc} = \frac{1}{2}(V_{O+} + V_{O-})$$
(15)

8 of 12



(a)

(b)

Figure 6. Pathological equivalent circuit of fully differential amplifier in Figure 14 of [27] for computing (a) Differential-mode output (b) Common-mode output.

According to Figure 6a, it is known that $V_{1-} = -V_{1+}$ and $V_{2-} = -V_{2+}$. We obtain $V_{1d} = V_{1+} = V_1$ = $-V_{1-} = -V_2$ and $V_{2d} = V_{2+} = V_3 = -V_{2-} = -V_4$ from (14). Based on steps 1 and 2 in Section 3, we can derive the system of equations in (8 × 8) matrix form as in (16). However, adopting the analytic method in reference [20,23], when we build the system of equations to compute the differential-mode output of the same circuit, 19 nodal admittance equations will be built. This is because each input voltage signal source is replaced by its nullor equivalence (thus additional 4 equations are added) and more complicated NGM model (there are 15 ungrounded nodes in the NGM model of FDCCII in Figure 5 of reference [23]) is used. Using the method in reference [24], the dimension of initial built the system of equations is (14 × 12) since there are 8 ungrounded nodes in the NGMFM model of FDCCII and 6 equations are added additionally.

By applying steps 3 and 4 in Section 3, the system of equations can be expressed as (17) since the voltage signal sources in Figure 6a are treated as grounded norators. Based on the property of differential voltage conveying cell, (namely, $V_5 = V_1 - V_2 + V_3$ and $V_6 = -V_1 + V_2 + V_4$) and applying steps 5–8, the system of equations (17) becomes (18). It is observed that the unknown voltage variables V_5 and V_6 in (17) are eliminated. After applying step 9, the matrix equations can be given by (19) since it is known that $V_1 = -V_2$ and $V_3 = -V_4$. Solving V_7 and V_8 , we can express the differential output function (V_{Od}) by (20).

$$\begin{bmatrix} 0\\0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & -y_1 & 0 & y_2 & 0\\ 0 & 0 & 0 & 0 & 0 & -y_1 & 0 & y_2 \end{bmatrix} \begin{bmatrix} V_1\\V_2\\V_3\\V_4\\V_5\\V_6\\V_7\\V_8 \end{bmatrix}$$
(17)
$$\begin{bmatrix} 0\\0 \end{bmatrix} = \begin{bmatrix} -y_1 & y_1 & -y_1 & 0 & y_2 & 0\\ y_1 & -y_1 & 0 & -y_1 & 0 & y_2 \end{bmatrix} \begin{bmatrix} V_1\\V_2\\V_3\\V_4\\V_7\\V_8 \end{bmatrix}$$
(18)

$$\begin{bmatrix} 2y_1V_{1,-2} + y_1V_{3,-4} \\ -2y_1V_{1,-2} - y_1V_{3,-4} \end{bmatrix} = \begin{bmatrix} y_2 & 0 \\ 0 & y_2 \end{bmatrix} \begin{bmatrix} V_7 \\ V_8 \end{bmatrix}$$
(19)

$$V_{Od} = \frac{1}{2}(V_7 - V_8) = \frac{y_1}{y_2}(2V_{1,-2} + V_{3,-4}) = \frac{y_1}{y_2}(2V_{1d} + V_{2d})$$
(20)

For the circuit in Figure 6b, V_{1c} (= V_1) and V_{2c} (= V_2) are respectively the common-mode input voltage signal sources. According to steps 1–2 in Section 3 of the proposed method, we can write the (6 × 6) nodal admittance equations in matrix form as (21). But the proposed methods in references [20,23] and reference [24] will need to build 15 and 10 nodal admittance equations, respectively. According to steps 3 and 4 in Section 3, the system of equations is reduced to (22). Based on the property of the differential voltage conveying cell, (i.e., $V_5 = V_2$ and $V_6 = V_2$) and applying steps 5–8 leads to the derivation of the system of equations of (23). After applying step 9, the formulation can be given by (24). Solving V_3 and V_4 , we can express the common-mode output function (V_{Oc}) by (25).

$$\begin{bmatrix} I_{1c} \\ I_{2c} \\ I_{C1} \\ I_{C2} \\ I_{C1} \\ I_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -y_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & -y_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & -y_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -y_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix}$$
(21)
$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -y_2 & 0 & y_1 & 0 \\ 0 & 0 & 0 & -y_2 & 0 & y_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix}$$
(22)

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & y_1 & -y_2 & 0 \\ 0 & y_1 & 0 & -y_2 \end{bmatrix} \begin{bmatrix} V_2 \\ V_3 \\ V_4 \end{bmatrix}$$
(23)
$$\begin{bmatrix} -y_1 V_2 \\ -y_1 V_2 \end{bmatrix} = \begin{bmatrix} -y_2 & 0 \\ 0 & -y_2 \end{bmatrix} \begin{bmatrix} V_3 \\ V_4 \end{bmatrix}$$
(24)

10 of 12

$$V_{Oc} = \frac{1}{2}(V_{O+} + V_{O-}) = \frac{1}{2}(V_3 + V_4) = \frac{y_1}{y_2}V_2 = \frac{y_1}{y_2}V_{2c}$$
(25)

The analyzed results of differential output function (V_{Od}) and common-mode output function (V_{Oc}) are in accordance with the functions given by (39) and (40) of reference [27], respectively.

5. Conclusions

In this paper, an improved formulation method with two techniques to enhance the efficiency of symbolic NA is presented. Both techniques are conducive to building smaller number of nodal equations when performing symbolic nodal analysis. It is especially practical when applied to popular high-noise-immunity circuits with differential voltage signal inputs. The proposed analytical procedure is expected to be realized in computer programs since it involves simple entries operations in matrix. Thus it is helpful in enhancing the efficiency of symbolic NA in analog design automation.

Author Contributions: Conceptualization, S. and Y.-L.L.; methodology, S. and H.-D.T.; theoretical verification, C.C.P. and H.-Y.W.; writing, review and editing, H.-Y.W. and S.-H.C.; project administration, S., H.-Y.W. and S.-H.C.; funding acquisition, H.-Y.W. and S.-H.C.

Funding: This research was funded by the Ministry of Research, Technology and Higher Education of the Republic of Indonesia (Grant No. 124.14/E4.4/2014, 7 July 2014) and the Ministry of Science and Technology of the Republic of China, grant number MOST 105-2923-E-992-302-MY3 and 107-2622-8-992-301-TE2.

Acknowledgments: The software and technical support from the Chip Implementation Center is gratefully acknowledged.

Conflicts of Interest: The authors declare no conflict of interest.

References

- 1. Tellegen, B.D.H. La recherche pour una série complète d'éléments de circuit ideaux nonlinéaires. *Rend. Semin. Mat. Fis. Milano* **1954**, 25, 134–144. [CrossRef]
- Carlosena, A.; Moschytz, G.S. Nullators and norators in voltage to current mode transformations. *Int. J. Circuit Theory Appl.* 1993, 21, 421–424. [CrossRef]
- 3. Kumar, P.; Senani, R. Bibliography on nullors and their applications in circuit analysis, synthesis and design. *Anal. Integr. Circuits Signal Process.* **2002**, *33*, 65–76. [CrossRef]
- 4. Swamy, M.N.S. Transpose of a multiterminal element and applications. *IEEE Trans. Circuits Syst. II* **2010**, *57*, 696–700. [CrossRef]
- 5. Mitra, S.K. Equivalent circuit of gyrators. *Electron. Lett.* **1967**, *3*, 333–334. [CrossRef]
- 6. Mitra, S.K. Non-reciprocal negative impedance inverter. *Electron. Lett.* **1967**, *3*, 388. [CrossRef]
- 7. Hashemian, R. Fixator-norator pairs vs direct analytical tools in performing analog circuit designs. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2014**, *61*, 569–573. [CrossRef]
- 8. Papazoglou, C.A.; Karybakas, C.A. A transformation to obtain CCII-based adjoint of op.-amp.-based circuits. *IEEE Trans. Circuits Syst. II* **1998**, 45, 894–898. [CrossRef]
- 9. Svoboda, J.A. Using nullors to analyse linear networks. *Int. J. Circuit Theory Appl.* **1986**, *14*, 169–180. [CrossRef]
- 10. Soliman, A.M. The inverting second generation current conveyors as universal building blocks. *AEU Int. J. Electron. Commun.* **2008**, *62*, 114–121. [CrossRef]
- 11. Leuciuc, A. Using nullors for realisation of inverse transfer functions and characteristics. *Electron. Lett.* **1997**, 33, 949–951. [CrossRef]
- 12. Floberg, H. Symbolic Analysis in Analog Integrated Circuit Design; Kluwer Academic: Boston, MA, USA, 1997.
- 13. Chipipop, B.; Surakampontorn, W. Realisation of current-mode FTFN-based inverse filter. *Electron. Lett.* **1999**, *35*, 690–692. [CrossRef]
- 14. Awad, I.A.; Soliman, A.M. Inverting second generation current conveyors: The missing building blocks, CMOS realizations and applications. *Int. J. Electron.* **1999**, *86*, 413–432. [CrossRef]
- 15. Saad, R.A.; Soliman, A.M. A new approach for using the pathological mirror elements in the ideal representation of active devices. *Int. J. Circuit Theory Appl.* **2010**, *38*, 148–178. [CrossRef]

- Soliman, A.M. On the DVCC and the BOCCII as adjoint elements. J. Circuits Syst. Comput. 2009, 18, 1017–1032.
 [CrossRef]
- 17. Soliman, A.M. Pathological representation of the two-output CCII and ICCII family and application. *Int. J. Circuit Theory Appl.* **2011**, *39*, 589–606. [CrossRef]
- 18. Huang, W.C.; Wang, H.Y.; Cheng, P.S.; Lin, Y.C. Nullor equivalents of active devices for symbolic circuit analysis. *Circuits Syst. Signal Process.* **2012**, *31*, 865–875. [CrossRef]
- 19. Tan, L.; Liu, K.; Bai, Y.; Teng, J. Construction of CDBA and CDTA behavioral models and the applications in symbolic circuit analysis. *Anal. Integr. Circuits Signal Process.* **2013**, *75*, 517–523. [CrossRef]
- 20. Wang, H.Y.; Huang, W.C.; Chiang, N.H. Symbolic nodal analysis of circuits using pathological elements. *IEEE Trans. Circuits Syst. II* **2010**, *57*, 874–877. [CrossRef]
- 21. Sanchez-Lopez, C.; Fernandez, F.V.; Tlelo-Cuautle, E.; Tan, S.X.D. Pathological element-based active device models and their application to symbolic analysis. *IEEE Trans. Circuits Syst. I* 2011, *58*, 1382–1395. [CrossRef]
- 22. Davies, A.C. Matrix analysis of networks containing nullators and norators. *Electron. Lett.* **1966**, *2*, 48–49. [CrossRef]
- 23. Sanchez-Lopez, C. Pathological equivalents of fully-differential active devices for symbolic nodal analysis. *IEEE Trans. Circuits Syst. I* 2013, 60, 603–615. [CrossRef]
- 24. Wang, H.Y.; Chang, S.H.; Chiang, N.H.; Nguyen, Q.M. Symbolic analysis using floating pathological elements. In *Genetic and Evolutionary Computing*; Springer: Cham, Switzerland, 2013; pp. 379–387.
- 25. Chang, C.M.; Al-Hashimi, B.M.; Wang, C.L.; Hung, C.W. Single fully differential current conveyor biquad filters. *IEE Proc. Circuits Devices Syst.* **2003**, *150*, 394–398. [CrossRef]
- 26. Ibrahim, M.A.; Kuntman, H.; Cicekoglu, O. New second-order low-pass, high-pass and band-pass filters employing minimum number of active and passive elements. In Proceedings of the International Symposium on Signals, Circuits and Systems, Iasi, Romania, 10–11 July 2003; pp. 557–560.
- 27. El-Adawy, A.A.; Soliman, A.M.; Elwan, H.O. A novel fully differential current conveyor and applications for analog VLSI. *IEEE Trans. Circuits Syst. II* **2000**, *47*, 306–313. [CrossRef]



© 2018 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).