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Impact of Silicon Substrate with Low Resistivity on Vertical Leakage Current in AlGaN/GaN HEMTs

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Abstract: The role of low-resistivity substrate on vertical leakage current (VLC) of AlGaN/GaN-on-Si epitaxial layers has been investigated. AlGaN/GaN high-electron-mobility transistors (HEMTs) grown on both p-type and n-type Si substrates with low resistivity are applied to analyze the vertical leakage mechanisms. The activation energy (E_a) for p-type case is higher than that for n-type at 0–600 V obtained by temperature-dependent current-voltage measurements. An additional depletion region in the region of 0–400 V forms at the AlN/p-Si interface but not for AlN/n-Si. That depletion region leads to a decrease of electron injection and hence effectively reduces the VLC. While in the region of 400–600 V, the electron injection from p-Si substrate increases quickly compared to n-Si substrate, due to the occurrence of impact ionization in the p-Si substrate depletion region. The comparative results indicate that the doping type of low-resistivity substrate plays a key role for VLC.

Keywords: p-type Si substrate; n-type Si substrate; vertical leakage current; electron injection; impact ionization

1. Introduction

Gallium-nitride (GaN)-based devices have recently attracted increasing attention for optoelectronic applications, such as light-emitting diodes (LED) [1], laser diodes (LD) [2], ultraviolet (UV) detectors [3,4], and power electronic devices [5]. Especially high-electron-mobility transistors (HEMTs) of GaN-based power devices on silicon (Si) substrates are considered promising candidates for high-power electronic applications because of their superior properties, such as high breakdown voltage, high current driving capability, and high thermal stability [6]. AlGaN/GaN heterostructures on Si substrate and their power devices have become frontier areas and hot spots in research in the international academia and industry, due to their unique advantages of low cost and capability with mainstream CMOS technology for the preparation of Si integrated circuits. However, several challenges remain that need to be resolved regarding Si substrate, in particular, stronger charge trapping effects caused by high-resistivity Si [7], degradation due to electron injection from Si [8], and breakdown related to the inversion channel at the AlN/Si interface in GaN-based HEMTs [9]. The breakdown of GaN-on-Si lateral devices is thought to be limited by top-to-bottom vertical leakage current (VLC) in the end [10]. Therefore, understanding the vertical leakage mechanisms related to Si substrate is an essential step toward potential power device applications.

There are several reports about the role of substrate on the vertical leakage in AlGaN/GaN-on-Si. Borga et al. concluded that the use of a highly resistive p-type silicon substrate could increase the vertical breakdown voltage of the transistors, as the fact that the voltage drop on the GaN buffer is mitigated by the partial depletion of the substrate [7]. Sayadi et al. showed that the generation of Shockley–Read–Hall (SRH) in the silicon depletion region impacts electron supply and current conduction [11]. However, they have not investigated the details on the VLC mechanisms in the case of low-resistivity Si substrates. Although Li et al. investigated the carrier transport from n+, n, p+ and p-Si (111) substrates through AlN nucleation layer on Si structure [12], they have not yet discussed the VLC in the whole AlGaN/GaN HEMTs. Owing to the advantage of low-resistivity Si substrates for the low curvature growth of AlGaN/GaN epilayers [13], these kinds of substrates are usually used to grow thick AlGaN/GaN epilayers. It is thus desirable to investigate the VLC in AlGaN/GaN HEMTs grown on low-resistivity substrates.

In this letter, we present an extensive analysis to reveal that the structures with low-resistivity p-Si substrates (named as p-type below) could reduce the electron injection from Si into the top layer and lead to lower VLC at low voltage values, in comparison to the case of that with low resistivity n-Si substrates (named as n-type below). The temperature-dependent current-voltage (I-V-T) measurements indicate that the substrate limitation greatly affects the VLC at low biases.

2. Experiments

Our study was carried out on AlGaN/GaN epitaxial layers grown on p-Si (111) and n-Si (111) substrates by metal organic chemical vapor deposition (MOCVD). The schematic of the epitaxial structure with p-type substrate is illustrated in Figure 1a. The epi-stacks consists of a 250 nm AlN nucleation layer on a p-Si substrate with a resistivity of 0.004 Ω·cm, a 4.36 μm graded $Al_xGa_{1-x}N$ (x = 0.01–0.68) transition layer, a 400 nm undoped GaN channel layer, and finally a 2 nm GaN cap on a 25 nm $Al_{0.2}Ga_{0.8}N$ barrier layer. The epitaxial structure for n-type is the same as that of p-type structure [Figure 1a] except the Si substrate with n-type doped (0.004 Ω·cm). The fabricated structure has two Ohmic contacts with one above the AlGaN layer and the other under the Si substrate. The top contact is formed by depositing Ti/Al/Ni/Au metal stacks, followed by rapid thermal annealing at 850 °C for 35 s in nitrogen atmosphere. The bottom contact is formed by Al deposition on the Si substrate. The current-voltage (I-V) characteristics were obtained in the dark using an Agilent's B1500A semiconductor device analyzer.

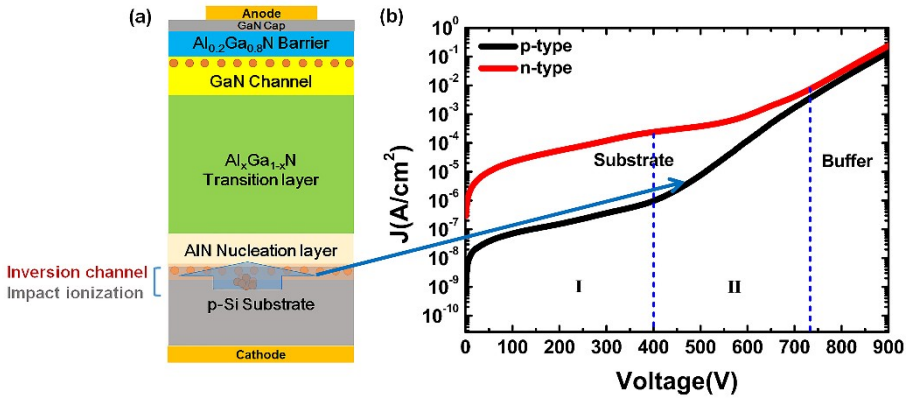

Figure 1. Growth structure with p-Si (111) substrate (**a**). Measured vertical leakage current of grown structures on p-Si and n-Si (111) substrate (**b**).

3. Results and Discussion

To investigate the effect of low-resistivity substrates on VLC of AlGaN/GaN epitaxial layers, vertical I-V measurements were performed on both samples, as shown in Figure 1b. Different I-V characteristics were investigated for the samples between the top contact (anode) on the AlGaN/GaN

surface and bottom contact (cathode) on the Si substrate. The voltage was swept up from 0 V to higher values with a step of 1 V during the forward-bias measurement. According to the difference of the slope of log J-V, the curves were divided into region I at low biases (0–400 V), and region II at high biases (400–740 V). It was found that the VLC of the p-type samples was reduced at region I and region II, compared to n-type, which shows the substrate effect. At region II for the p-type samples, VLC increases more rapidly compared to that in region I, and the log J-V curve exhibits a steeper slope than that for n-type. While at higher biases, the vertical current for p-type is the same with n-type. In that case, the effect of substrates is ignorable, and the buffer limitation plays a key role for both samples.

To investigate the role of different types of substrates on VLC conduction mechanisms, we conducted the I-V-T measurements for both samples, as shown in Figure 2a,b. For the p-type samples, a log J-V dependence can be observed at 0–400 V, which corresponds to the space-charge-limited current conduction mechanism [14]. The slope of log J-V starts to get larger from the kink at 400 V, as shown in Figure 2a, which is due to the Poole–Frenkel conduction at 400–600 V [15,16]. However, the log J-V dependence for n-type samples can be also observed in the whole range of 0–600 V, corresponding to the space-charge-limited current conduction mechanism [14].

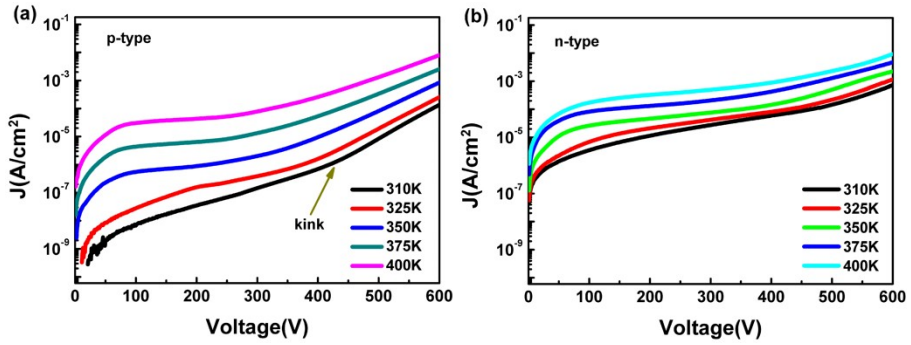

Figure 2. Temperature-dependent current-voltage (I-V) characteristics of p-type (**a**), n-type samples (**b**).

The effective energy barrier related to the VLC on different types of substrates has been investigated. The activation energy E_a refers to the barrier that electrons have to overcome for injecting from the Si substrate into GaN layers by thermionic emission. It is evaluated from the slope of ln J-1/T, as reported in literature [17,18]. In this work, E_a at 200 V, 300 V, 500 V, 600 V is measured on p-type (Figure 3a) and on n-type (Figure 3b) in the whole temperature range. E_a in p-type is larger than that in n-type at these biases. Further analysis of the E_a values at different biases is shown in Figure 3c. It can be observed that the E_a values of the p-type samples are always higher than that of n-type samples in the whole range (0–600 V). For p-type samples, E_a changes a little at low biases via the increase of voltages (0–400 V), while E_a decreases quickly at high biases (400–600 V). For n-type samples, the values of E_a did not change much in the whole region. That can be attributed to the fact that another conduction process exists for p-type Si samples, which is different from the n-type case. It clearly demonstrated the substrate limits of the leakage in the whole region (0–600 V).

According to the results above, the band diagrams of both samples are used to further analyze the impact of the low-resistivity Si substrates on the forward-bias leakage mechanisms. As shown in Figure 4a at 0–400 V, due to the generation of a space charge region at the AlN/p-Si interface, high E_a would occur, preventing electron injection from the p-Si substrate into the AlN layer, and hence reducing the leakage. While for n-type samples, as shown in Figure 4b, many electrons in n-Si substrate could be transported into the AlN layer, and the electron injection is increased at the lower E_a case, leading to larger VLC. Based on these mechanisms, phenomenon observed at low biases in Figure 1b can be well understood.

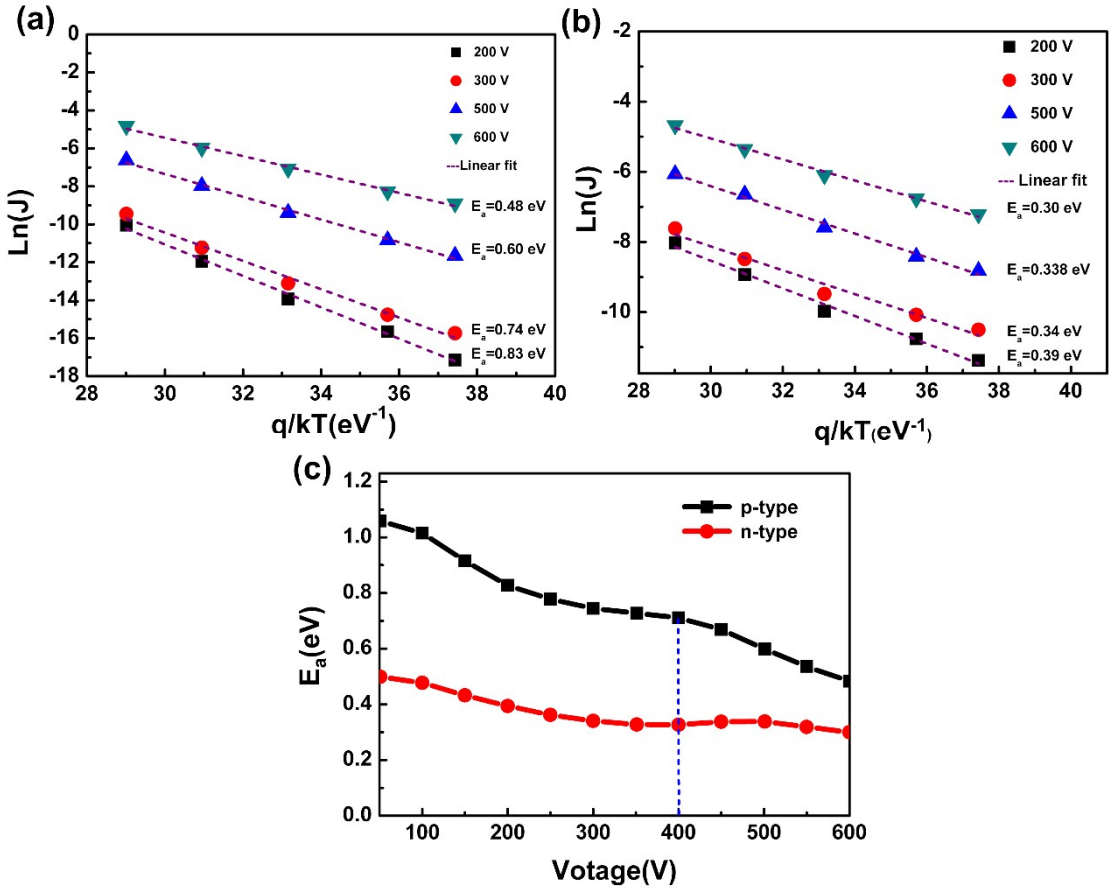

Figure 3. E_a extracted from ln J-1/T at different biases of p-type (**a**), and n-type (**b**) samples, (**c**) E_a-V(T) plots of p-type and n-type samples.

The AlN nucleation layer is very important for the growth of AlGaN/GaN-on-Si, but it leads to the formation of an additional AlN/Si interface. For the AlN/p-Si interface, the inversion channel responsible for VLC has been widely discussed in literature. Yang et al. found that a weak inversion channel would form at the high electric field in the AlN/Si interface, and the injection electrons originate from impact ionization of Si [19]. Yacoub et al. thought the inversion channel exists even without applying bias, which was confirmed by Hall measurements [20]. While several groups have already pointed out that the inversion channel could form under a certain voltage region, it could not be clearly characterized by capacitance voltage measurement, owning to the fact that the interface has a high acceptor trap density [11,12]. Thus, the existence of an inversion channel at the AlN/p-Si interface has been confirmed. In the present work, we found that the inversion channel at the AlN/Si interface appears for p-type samples, leading to the electron injection increasing [16], as shown in Figure 4c. When the applied voltages continue increasing, the electrons in the Si are accelerated because they obtain enough energy from the higher applied voltage (green arrow in E_c). The electron hole pairs are generated due to impact ionization (blue arrow between E_c with E_v). A lot of electrons coming from the impact ionization are injected into AlN layer, as shown in Figure 1a. However, the impact ionization in n-Si substrate does not occur for n-type samples [12], as shown in Figure 4d. So the E_a in n-type samples changes a little with voltages compared to p-type samples which drops quickly. As a result, the slope for p-type samples drops more quickly than that for n-type samples. In short, the substrates play a key role on VLC at the whole region of 0–600 V.

We summarize the recent state of the arts in Table 1. According to the results above, we can find that the difference in our work is that: (1) We find and clarify that the leakage mechanisms are different in the low and high bias ranges, and (2) we show a comparative study for AlGaN/GaN HEMTs on both

p-type and n-type substrates with low resistivity, while the literatures show the case of buffer only on both substrates.

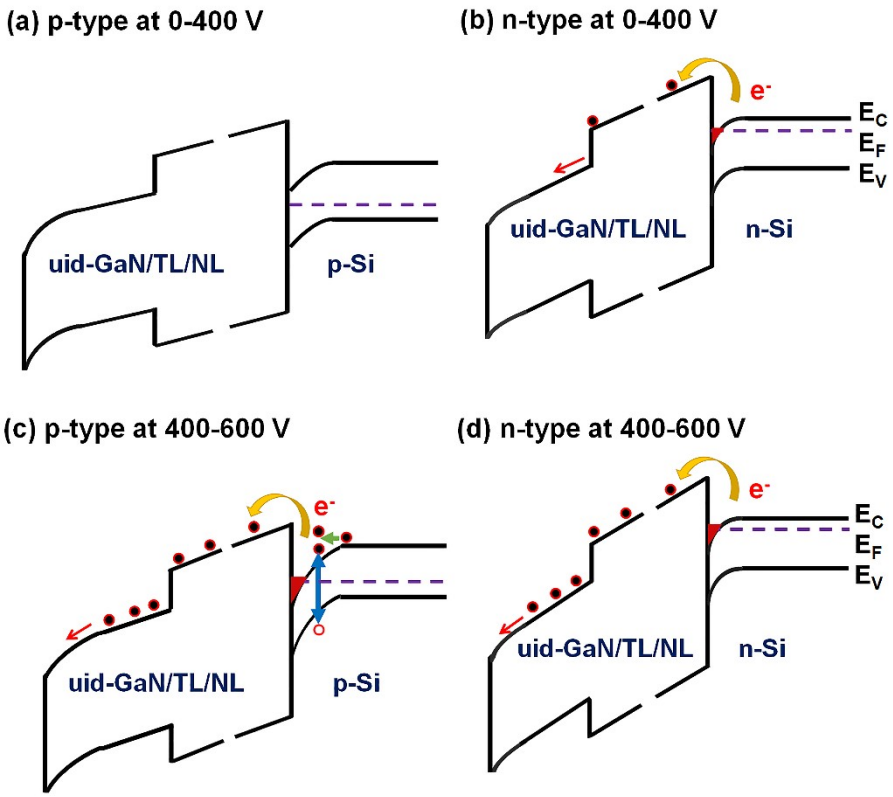

Figure 4. Band diagrams of the GaN-on-Si structure when the top surface is forward biased. (**a**) p-type, (**b**) n-type for 0–400 V and (**c**) p-type, (**d**) n-type for 400–600 V.

Table 1. Research status of vertical leakage mechanisms on Si substrate.

Sample Structure	Si Substrate	Vertical Leakage Mechanisms	Reference
TL/AlN/Si AlN/Si GaN-on-Si(p)	n^+ p	(i) p-type: SRH carrier generation in Si (ii) n^+-type: electron injection through AlN/Si barrier	[11]
AlN/Si	n^+, p^+ n, p	SCLC, VRH, and TAT models	[12]
GaN-on-Si	p Low resistivity	SCLC model	[14]
GaN-to-Si	p Low resistivity	(i) weak inversion in AlN/Si interface (ii) impact ionization in Si (iii) electron injection from Si into the Buffer	[19]
GaN-on-Si	p	(i) carrier injection from an inversion channel (ii) PF conduction	[20]
GaN-on-Si	p	PF conduction	[21]
(Al)GaN-on-Si		PF conduction (>200 V)	[22]
GaN-on-Si	n High resistivity	a combination of PF and hopping conduction	[23]
(Al)GaN-on-Si	p^+ n^+	(i) SCLC model at 0–400 V and PF conduction at 400–600 V for p-type (ii) SCLC model at 0–600 V for n-type (iii) impact ionization in p-Si	This work

4. Conclusions

In this work, we investigated the impact of different Si substrate types with low resistivity on the VLC in AlGaN/GaN epitaxial layers. The results indicate that a p-Si substrate based structure can form a depletion barrier and hence block the electron injection and finally reduce the VLC at 0–400 V compared to n-type. The temperature-dependent I-V and E_a-V results suggest that the sudden increase in the slope of the I-V curve for p-type samples is related to the impact ionization near the interface. Our results show that choice of the substrate greatly affects the VLC at lower voltage for AlGaN/GaN HEMTs.

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Conflicts of Interest: The authors declare no conflict of interest.

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