

Review

Atomic Layer Deposition (ALD) of Metal Gates for CMOS

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**Featured Application:** Metal gate of CMOS devices.

Abstract: The continuous down-scaling of complementary metal oxide semiconductor (CMOS) field effect transistors (FETs) had been suffering two fateful technical issues, one relative to the thinning of gate dielectric and the other to the aggressive shortening of channel in last 20 years. To solve the first issue, the high- κ dielectric and metal gate technology had been induced to replace the conventional gate stack of silicon dioxide layer and poly-silicon. To suppress the short channel effects, device architecture had changed from planar bulk Si device to fully depleted silicon on insulator (FDSOI) and FinFETs, and will transit to gate all-around FETs (GAA-FETs). Different from the planar devices, the FinFETs and GAA-FETs have a 3D channel. The conventional high- κ /metal gate process using sputtering faces conformality difficulty, and all atomic layer deposition (ALD) of gate stack become necessary. This review covers both scientific and technological parts related to the ALD of metal gates including the concept of effect work function, the material selection, the precursors for the deposition, the threshold voltage (V_t) tuning of the metal gate in contact with $\text{HfO}_2/\text{SiO}_2/\text{Si}$. The ALD of n-type metal gate will be detailed systematically, based mainly on the authors' works in last five years, and the all ALD gate stacks will be proposed for the future generations based on the learning.

Keywords: COMS; metal gate; atomic layer deposition; high- κ dielectric; threshold voltage; flatband voltage; effective work function; effective oxide thickness

1. Introduction

1.1. Scaling and Issues of SiO_2 /poly-Si Gate Stacks

Basic principle of FETs was proposed by Julius Edgar Lilienfeld in 1925 [1], in which, an electric field generated by a voltage applied to the gate electrode is used to control the flow of current between the drain and source electrodes. The metal–oxide–semiconductor field-effect transistor (MOSFET) was invented by Dawon Kahng and Martin Atalla in 1959 [2], in which the device structure is obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal on top, as shown in Figure 1a. The gate stack is equivalent to a planar capacitor, with one of the electrodes replaced by the semiconductor substrate. When a large enough voltage is applied to the gate (gate voltage $V_g >$ threshold voltage V_t), it modifies the distribution of charges in the doped bulk Si and form a conductive channel (inversion layer) near the SiO_2/Si interface and a depletion region below, as shown in Figure 1b, switching the device to its “on” state. If the gate voltage is lower than V_t , the transistor is switched “off”. By using different doped Si substrates, n-type and p-type MOSFETs could be made. In 1967, Frank Wanlass filed his patent of CMOSFETs [3], in which the two types of the MOSFETs are connected in a way shown in Figure 2 to form an inverter. When a gate voltage generates

an “on” in one MOSFET, it always give the “off” in the other one. The gate voltage change will switch simultaneously the states of the two MOSFETs. By doing this, the output voltage of the CMOSFETs will switch between high voltage (V_{dd}) and low voltage (V_{ss}). After the switching, or at the static state, there is always one device “off”, or no current (ideally) between the line V_{dd} and line V_{ss} . Such a low standby power characteristic of CMOSFET made it an enabler of Very Large Scale Integrated Circuit (VLSI) and Ultra-Large Scale IC (ULSI).

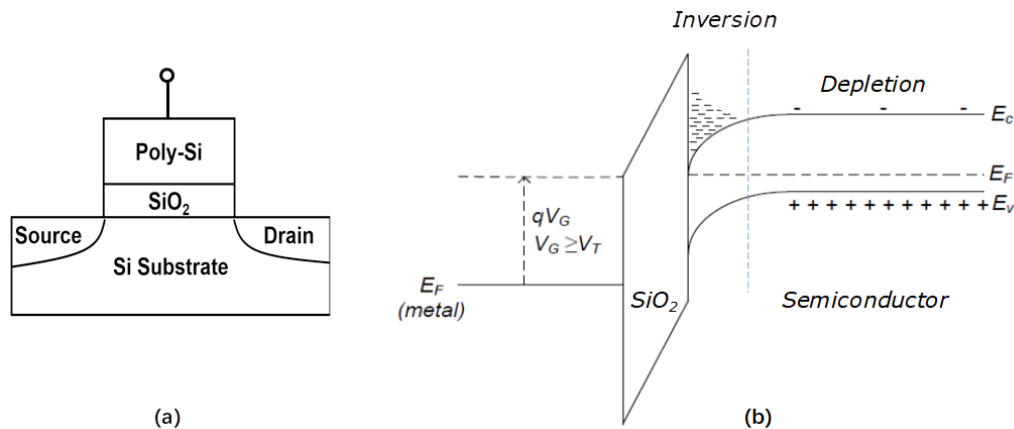


Figure 1. MOSFET (a) and its energy band structure (b), where q is the carrier density, V_G the gate voltage, V_t the threshold voltage, E_f the fermi level, E_c and E_v the conduction band and valence band edges, respectively.

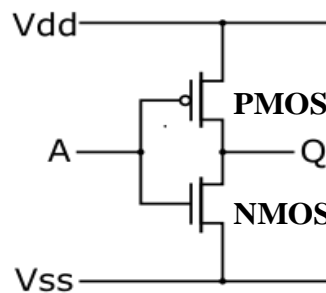


Figure 2. CMOSFETs, where input voltage is applied to A and output is extracted by the voltage of Q.

In the history of MOSFET technology development, the gate stack using SiO_2 as dielectric and poly-Si as gate electrode (Poly-Si/ SiO_2 /Si) was the most successful story. SiO_2 dielectric was used in the first Si MOSFET technology, together with aluminum (Al) metal gate. In 1971, poly-Si gate was induced to replace Al. In 1989, the dual gate technology by doping the poly-Si was employed in 800 nm node to simplify CMOS process. The Poly-Si/ SiO_2 /Si stack had been used for 10 generations, until 130 nm. During these years, switching performance of the devices was continuously improved, and device number per unit area increased, by scaling down the dimension of the MOSFETs.

For a MOSFET with thick enough SiO_2 , the leakage through it is negligible compared to that between the source and drain. As its thickness is reduced to nanometer level, the tunnel leakage due to quantum effect increases to large extent and finally dominates the device leakage [4]. According to the prediction of ITRS in 1999, the pure SiO_2 could not be used as the gate dielectric after 130 nm node.

For a gate dielectric layer of SiO_2 , the gate leakage density J_g could be described as

$$J_g = \frac{A}{T_{ox}^2} \exp\left\{-2T_{ox} \sqrt{\frac{2m^*q}{\hbar^2} \left(\Phi_B - \frac{V_{ox}}{2}\right)}\right\} \quad (1)$$

where T_{ox} is the layer thickness, Φ_B the potential barrier height between the metal and the SiO_2 , V_{ox} the voltage drop through the SiO_2 , m^* the electron effective mass in the dielectric, and A an experimental

constant. For a dielectric without defects, Φ_B could be determined by the energy band alignment as shown in Figure 3. For electron transportation, the barrier is conduction band offset given as ΔE_C . For hole transportation, it is valence band offset given as ΔE_V . It is easy to see that J_g strongly depends on Φ_B . In a real dielectric material, the barrier height is also relative to the defect density in SiO_2 . The defects could form energy levels in the SiO_2 band gap and trap the charges. Such a trap-assisted mechanism of charge transportation can be described as Frenkel-Poole emission or hopping conduction [4].

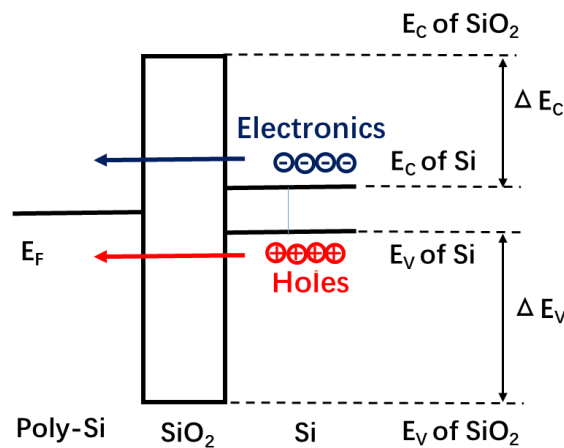


Figure 3. Band diagram of the poly-Si/SiO₂/Si gate stack.

The gate leakage depends strongly on T_{ox} , as shown in Equation (1) and Figure 4. For the layers thinner than 1 nm, the extremely high tunneling leakage will cause intolerable power consumption and joule heat.

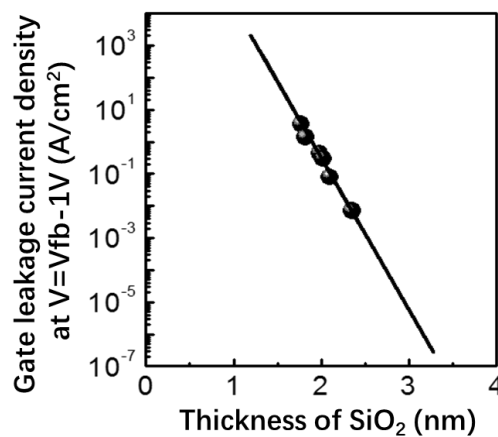


Figure 4. Gate leakage current density as a function of SiO₂ physical thickness.

Reliability degradation is an equally important issue attributed to the dielectric down-scaling. Degraeve gave a fundamental mechanism of dielectric breakdown in a thin SiO₂ film based on percolation model [5]. The breakdown occurs when the accumulation of different defects in the SiO₂ network reaches the threshold and builds a conductive filament. Such a failure mechanism explains well the sensitivity of breakdown to the film thickness.

Another issue of the conventional poly-Si/SiO₂ gate stack worsened by the dimension scaling is the boron penetration [6]. In a poly-Si gate, the carriers derive from the doped III or V valence elements. For a p-type poly-Si, boron is widely used as dopants. The boron ions in the heavily doped poly-Si could diffuse through the gate dielectric. For a thick dielectric layer, the diffusion could be very small. As the SiO₂ is scaled to nanometer thick, the out-diffused B dopants accumulating in the SiO₂ and

Si substrate would change the threshold voltage, increase the defect density and further worsen the leakage and reliability issues.

1.2. High- κ Dielectric and Effective Oxide Thickness (EOT)

The solution to the issues above is to use an alternative dielectric which has a dielectric constant, or κ -value, higher than SiO₂ and allows physical thickness larger than SiO₂ without tradeoff in gate capacitance. For a simplified model, the capacitance between the gate and the channel can be expressed as

$$C = \frac{\epsilon_0 \kappa S}{t} \quad (2)$$

where κ is the dielectric constant, ϵ_0 the permittivity of free space ($= 8.85 \times 10^{-3}$ fF/fm), S the area, and t the thickness of the dielectric. For SiO₂, κ is around 3.9. If a high κ material is used as gate dielectric, a thicker layer could give the same capacitance density, or for a high- κ layer of a given thickness ($t_{\text{high-}\kappa}$), the capacitance density generated equals to that of a SiO₂ layer of t_{ox} . This t_{ox} is called equivalent oxide thickness (EOT)

$$EOT = \frac{3.9}{\kappa} t \quad (3)$$

For example, to retain an EOT of 1nm for a dielectric with a κ -value ~ 20 , the physical thickness of the high- κ could be ~ 5 nm. The increase of the physical thickness could help to suppress the gate leakage.

First industrial application of alternative dielectric concept was to alloy nitrogen into SiO₂ to form so-called silicon oxynitrides, whose κ value is slightly higher than SiO₂ and thus allows larger physical thickness than SiO₂. The κ -value of pure Si₃N₄ is around 7, compared to that of SiO₂ about 4. That of SiO_xN_y is between 4 and 7, depending on the nitrogen concentration in the films. Encouraging results in leakage current reduction, boron diffusion control, and reliability enhancement were demonstrated by using SiO_xN_y to replace SiO₂ of the same EOT [7–9]. The leakage suppression of SiO_xN_y depends on the layer composition. A work done by Yang and Lucovsky [10], for instance, demonstrated a 100× leakage current reduction using a layer with a SiO₂: Si_xN_y ratio of 1:1 and EOT of 1.7 nm. The advantages of SiO_xN_y lie in that it guarantees the safety in contamination control, because nitrogen is a widely used element in IC production and the compatibility to conventional poly-Si. It has been found that the addition of N to SiO₂ can form Si–O–N network bonding and greatly block the boron diffusion through the dielectric [11,12]. The reason for using SiO_xN_y instead of pure Si₃N₄ is that the former shows much better channel mobility [13]. The mobility degradation attributes to the pentavalent N at interface, which induces defects and aggravate the interface scattering. For SiO_xN_y layers, especially those with graded N concentration, the interface defects density could be much less than the pure SiN_x. The SiO_xN_y dielectric was used for a few technology nodes. By increasing the N concentration node by node, the scaling strategy was successfully extended from 130 nm node to 65 nm node. The SiO_xN_y solution can only temporarily alleviate the gate leakage crisis. When EOT is below 1.3 nm, it does not work anymore and a new alternative has to be found from “real” high- κ candidates [14].

A high- κ dielectric must have a high κ -value, large enough band offsets with Si, and be thermally stable when contacted with the gate electrode and Si, and its impact to channel mobility must be acceptably small [15–17]. Figure 5 lists the dielectric properties of most important gate dielectric candidates. Among all of them, SiO₂ has the lowest dielectric constant and the largest conduction and valence band offsets. For the others, the band offsets decrease when the κ -value increases. The decrease in conduction band offset will trade off the positive effect in leakage suppression due to the thickness increase. Therefore, an ideal high- κ should have a balance between the κ value and band gap. The films with ultra-high κ value and very small band offsets, such as TiO₂, are thus out of consideration. Furthermore, ultra-high κ value means a very thick dielectric and a large thickness/length ratio. An undesirable effect, the fringing effect of the gate stack, will become extremely high [18].

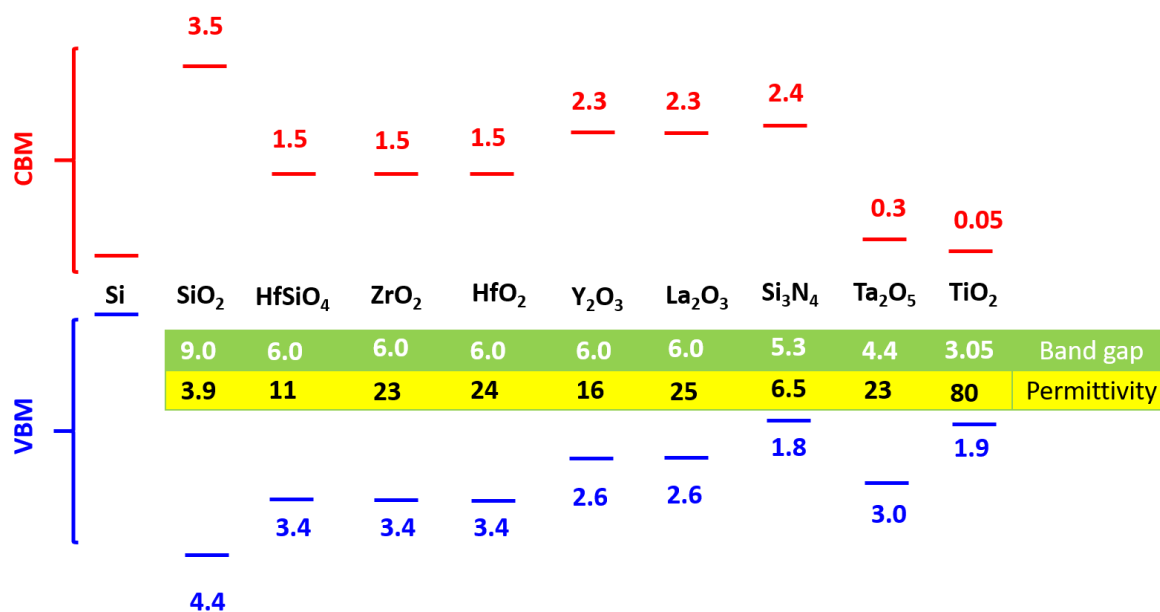


Figure 5. Comparison of the dielectrics in conduction and valence band offsets and permittivity.

Besides the κ -value and band alignment, attention must be paid to the interfacial quality between the high- κ dielectric and Si. The high leakage has been found due to the degradation of the interfacial oxide between the high- κ and the Si [17]. The defects near the interface could reduce the barrier height Φ_B , and induce carrier scattering, causing the degradation of the channel mobility.

Thermal stability of the high- κ stack is another filter. In fact, plenty of metal oxides have higher κ -values than Si dioxide, from Si₃N₄ with a $\kappa \sim 7$ to PbLaTiO_x with a κ -value as high as 1400 [19,20], most of them in a stack in contact with Si shows poor stability at high temperatures, and thus eliminated from the list. Other properties, such as breakdown properties, adhesion with the top metal layer and bottom Si substrate, the temperatures of deposition and annealing, and readiness to be patterned with available lithography, should also be taken into account. After the elimination, very limited candidates are left in the list. The finally crowned high- κ dielectric by industry is HfO₂ [21–24].

HfO₂ has a κ -value about 25, a bandgap around 5.7 eV, yielding large enough band offsets with Si. Its large formation heat (−271 kcal/mol, compared to that of SiO₂ ∼−218 kcal/mol) guarantees good thermal stability in contact with silicon. The gate leakage current of the MOSFETs using a HfO₂ dielectric show several orders of magnitude reduction compared to that of SiO₂ with the same gate capacity [25,26].

1.3. Metal Gate and Effective Work Function (EWF)

Another important issue relative to the dielectric thickness scaling is the depletion layer formed in the poly-Si gate near the interface of the gate and the dielectric, as shown schematically in Figure 6. The thinner is the dielectric, the stronger the field is generated by the channel inversion, and the more charges are involved in the depletion layer. The depletion layer forms an additional capacitor over the dielectric and impairs the impact of the gate voltage to channel. The thickness of the depletion layer is related to the carrier density of the poly-Si gate. The increase of doping level in the poly-Si can help to reduce the depletion thickness. The effort in employing more aggressive implantation for heavier doping poly-Si could induce grievous impurity penetration through the gate oxide [27]. Limited by this, the doping level of the n+ poly-Si is normally below 10²⁰ cm^{−3} and that of p+ poly-Si is less than the mid of 10¹⁹ cm^{−3}. This means that the depletion issue could not be released via increasing doping level. Beyond the 65 nm node, the poly-Si gate had to be phased out and replaced by metal gate electrodes.

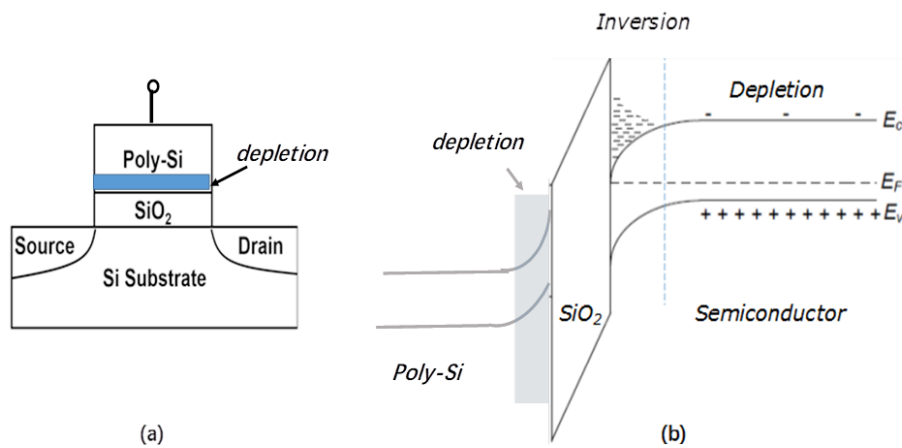


Figure 6. Depletion layer formed in poly-Si. (a) schematic of a MOSFET; (b) band structure of poly-Si/oxide/semiconductor.

The work function is the first requirement for the metal gate electrodes. At beginning, the selection of the metal gate candidates was based on their work function in vacuum. Figure 7 lists more than 20 metals and their vacuum work functions [28]. When a metal is in a MOS structure, its work function shifts from its vacuum value. This value is normally termed as “effective work function or EWF”. EWF could be extracted from the C-V curves obtained with the MOS capacitors (MOSCAP) [29]. Figure 8 displays the simplified energy band diagram of an ideal MOS structure using n-type substrate under the condition of flat band, where Φ_M stand for the work function of the metal, χ for the electron affinity, E_g for the band gap, Φ_B for the potential barrier between the dielectric and metal, and Ψ_B for the difference of potential between the Fermi level E_F and the intrinsic Fermi level at the midgap. Here, “ideal” means the fixed charge density in the dielectric is zero. As applied voltage is zero, the MOS structure has a flat band as shown in Figure 8, or the difference between the work functions the metal and the semiconductor, Φ_{MS} , is zero. For n-type substrate

$$\Phi_{MS} = \Phi_M - (\chi + \frac{E_g}{2q} - \psi_B) \tag{4}$$

C-V measurement will give the curve as shown in the right plots of Figure 8. For p-type substrate, the case is similar. The Φ_{MS} is

$$\Phi_{MS} = \Phi_M - (\chi + \frac{E_g}{2q} + \psi_B) \tag{5}$$

For real dielectric with a fixed charge density of ($\pm Q_f$), the C-V curve will shift as shown in the plots. To have a flat band, a voltage of V_{fb} needs to be applied to shift the curve back.

$$V_{fb} = \Phi_{MS} + \frac{Q_f}{\epsilon_0\kappa}EOT \tag{6}$$

Assuming the Q_f is independent of EOT , the measured V_{fb} as a function of EOT will intercept the y -axis at Φ_{MS} . Using this intercept value and the band structure of the dielectric, the effective work function of the metal Φ_M could be extracted.

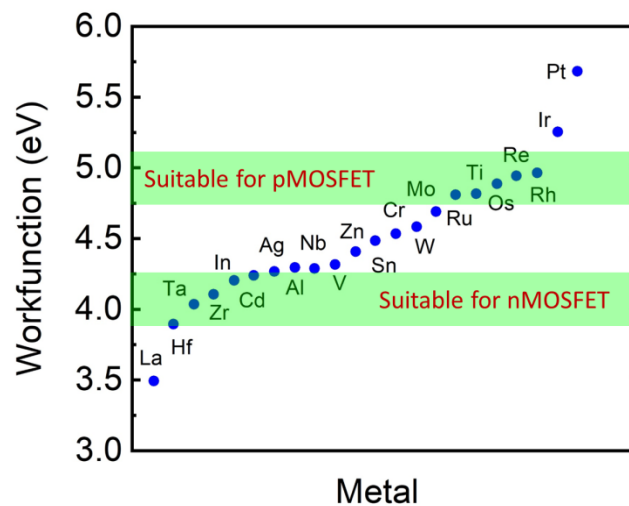


Figure 7. Work function of metals.

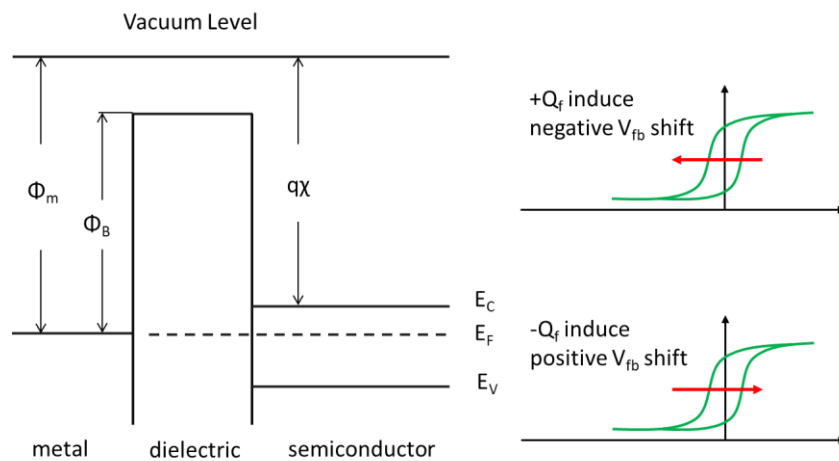


Figure 8. Flatband conditions of MOS structure for n-type substrate.

The metal gate for CMOSFETs can be a single metal with one *EF* near midgap or two different metals (dual metal gate), one with *EF* near the edge of the conduction band, and the other near that of the valance band, separately. Equation (7) gives the V_t as a function of V_{fb} .

$$V_t = V_{fb} + \frac{|Q_s|}{C_i} + 2\psi_B = V_{fb} + \frac{\sqrt{2\epsilon_s q N (2\psi_B)}}{C_i} + 2\psi_B \tag{7}$$

where the Q_s is substrate charge density corresponding to the substrate surface potential of inversion mode ($2\psi_B$), N the substrate doping concentration, C_i the gate oxide capacitance, ϵ_s the substrate permittivity. The single metal gate is the most straightforward solution, favorable to the CMOS processing. However, this approach is not favorable in device performance. The midgap work function induces high V_t and poor operation channel current. It has to be pointed out that the above conclusion on the single metal solution is true only for planar CMOS using bulk Si substrate. For the devices such as undoped FinFETs and FD-SOI FETs, it is more complex [30,31].

For the dual-metal gate CMOSFETs, the Φ_M of the gate electrode for nMOS is expected to be ~4 eV and that for pMOS ~5 eV [32]. Since the *EF* vacuum work function could not be used as the screening criteria, the study of metal gate properties needs to be done in a real gate stack with selected high- κ material and carefully designed stack structure. To reach threshold voltage (V_t) target, extreme care needs to be taken, because V_t is so sensitive to interfacial states that any slight difference in chemical composition, defects and polarization will induce V_t shift.

The thermal stability of the metal gate had been regarded as a fateful technical block for the industrial application of high- κ /metal gate stack. The harshest thermal process in CMOS production is the annealing for dopants activation in the area of source and drain. In most cases, a rapid thermal annealing (RTA) between 900–1100 °C is employed. The work function of most metals will shift back to midgap after this annealing. This is why the metal gates studied in the early explorations all have good refractory. They include elemental metals, their oxides, silicides, nitrides, carbides or alloys of more than two of them. Most of them, when being in contact with the selected high- κ , could not keep stable at high temperature. After the activation annealing, the EWf shifts.

To bypass the thermal instability problem, a new processing flow, the gate-last approach, has been developed [25]. In such a process, the high- κ is first deposited, followed by the conventional poly-Si gate process to form a poly-Si “dummy” gate. This conventional flow continues until the activation anneal is finished. Then, the poly-Si gate is removed before the deposition of the metal gate layer, capping layer and filling metal. In such a “replacement gate” regime, the source/drain activation anneal is carried out before the metal gate deposition and thus successfully avoids the V_t shift related to the activation anneal.

In the 45 nm node, the first generation of the high- κ /metal gate technology for mass production, dual metal/single high- κ stack was used. The metal gate for nMOS was TiAl, and that for pMOS was TiN, integrated with HfO₂ dielectric by a gate last process [25,33]. The TiAl and TiN were deposited in the trench on the bottom after the replacement gate removal. To fill the gap, a conductive metal such as Al or W was deposited.

TiN in the stack with HfO₂ has a EWf range between 4.4 and 4.9 eV, depending on processing technique used and the metal layer thickness [34,35] and meets the requirement for pMOS. TiN is a widely used material in conventional IC process, so induces no contamination risk. Its deposition, etching and cleaning techniques are well developed using industrial standard equipment. During 2003–2006, a lot of works presented at device conferences on the integration technology used high- κ /TiN metal gate stack, where TiN were deposited by PVD or CVD [36–42].

Aluminum metal has a work function around 4.28 eV and good conductivity, and thus is a candidate of n-type metal gate. Its melting point, however, is quite low (~660 °C), implying a poor thermal stability. Alloying Al into more refractory metal to form alloy was one of the research directions [43]. Doping Al into PVD TiN, for example, can shift the EWf from the value near the bottom of the Si conduction band to that near the top of the valence band [44] and get different flatband voltages in TiN(Al)/HfO₂/Si stack. In 2010, Kesapragada et al. reported a work function screening result for gate last process and proposed the combination of PVD TiAl for n-type metal with PVD TiN for p-type metal. The PVD TiAl and PVD TiN in gate stacks with HfO₂ show EWf around 4.1 eV and 4.85 eV. The C-V measurements show that the PMOS using HfO₂/PVD-TiN and the NMOS using HfO₂/PVD-TiAl have 1 volt separation in V_{fb} [45]. Intel seemed to use this combination for their planar CMOS integration, and got working high-performance devices with large gate leakage current reduction [25].

1.4. Metal Gate for FinFETs and GAA-FETs

Gate leakage is not the only issue relative to the dimension scaling. Compared to a long channel MOSFET, the shrinking of channel length will reduce the gate control ability [46–48]. First, the current at $V_g < V_t$ (subthreshold leakage) will increase along with the gate length shrinking, inducing so-called subthreshold swing, SS . Second, for short channel devices, V_t is also a function of the voltage between drain and source, V_{DS} , certain charges are depleted by the V_{DS} . As a result, the gate voltage required to form the channel is lowered by V_{DS} . This is called drain induced barrier lowering (DIBL). Third, for short channel devices, the potential of source and drain will also impact the channel, making the channel formation at lower V_t . The shorter is the channel, the smaller is the V_t . This is referred to as V_t roll-off.

All these short channel effects could be suppressed by changing the device structure from planar MOSFETs to FinFETs [49] and gate-all-around (GAA) FETs [50]. The FinFETs have become the mainstream logic devices for a few nodes [51]. The GAA nano-Si wire FETs and Si nano-sheets FETs have been reported by the research teams using industrial processing facility [52–57].

The relation between V_t and the work function of the gate electrode for FinFETs with undoped channel is different to that for the planar MOSFETs. For planar devices, there are plenty of charges to form inversion. For undoped FinFETs, much less charges are available. As a result, an additional surface potential needed to reach the V_t . W. Xiong summarized the relation of the V_t and work function of the gate electrode for low-power and high performance planar MOSFET and FinFETs in a schematically way as in Figure 9 [58]. The points in the top and bottom green rectangles give the V_t requirement of different low power devices and high performance devices, respectively. The points in the rectangle with yellow color give the work function requirement of bulk planer NMOSFETs and PMOSFETs. The points in the triangle give the work function requirement of FinFETs. For low power FinFETs, a metal with a work function of 4.6 eV in the midgap of Si can meet the requirement for both n-type and p-type devices. High performance devices desire low threshold, and thus two metals with work functions near the edges of the conduction band and valence band of Si are needed. Different from the metal gates for the planar CMOSFETs, which needs two metals with work functions 0.4 eV from the midgap, those for the FinFETs can use metals with work functions 0.2 eV from the midgap. The work function values of FinFET are about 4.4 eV and 4.8 eV for N metal and P metal respectively, while the values are about 4.2 eV and 5.0 eV for planar CMOSFETs.

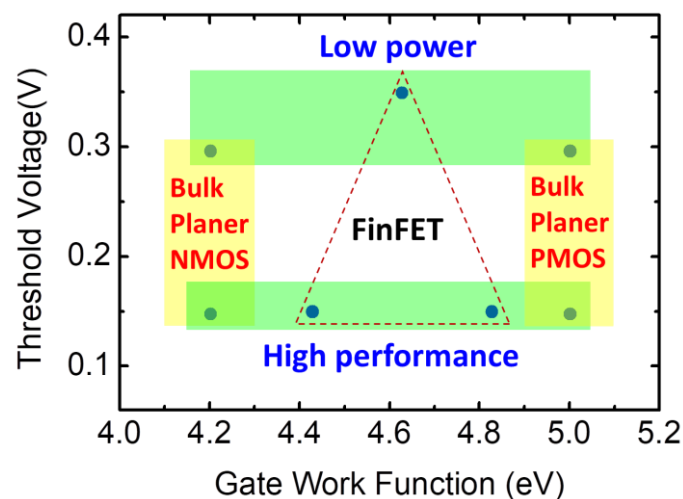


Figure 9. The relation between the threshold voltage and the work function of the metal gate for different devices.

Senzaki et al. [59] gave the other specifications include V_t stability ($\sim \pm 10$ mV of unstressed film), Mobility $\geq 95\%$ of that achieved with SiO_2 , density of interface traps (D_{it}) $\leq 5 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}$, high frequency (100 kHz) CV hysteresis ≤ 10 mV, Reliability comparable to Poly-Si/ SiO_2 , and thickness uniformity (3 sigma) $\leq 4\%$.

For FinFETs and GAA FETs, the conformality of the metal gate is a new challenge. In a planar device, the metal film could be deposited top-down by sputtering. For FinFETs, it is very difficult to form conformal film on sidewall of the Fins using these anisotropic deposition techniques. CVD technique has much better isotropy than PVD and is most likely able to meet the requirement of FinFETs. For GAA FETs, however, both PVD and CVD will be phased out from the deposition of gate layers, replaced by ALD. The advantages of using ALD to deposit metal gate can be summarized as: excellent thin film thickness uniformity, excellent composition control (doping by inserting dopant layers), little plasma damage to gate oxide (especially for thermal ALD) compared to PVD, lower

deposition temperature with low impurity compared to CVD, and conformality at nanoscale structures, especially for 3D devices [59].

2. ALD of the Metal Gates

Atomic layer deposition is a derivative of chemical vapor deposition (CVD), using the same reactants but different reactant introduction mode, to have a thickness control of mono-atomic layer level [60]. In CVD, the reactants, say AC and BD, are introduced together simultaneously and continuously into reaction chamber and the chemical reactions takes place in gas phase, or on the top surface of the substrate after absorption, to form a deposit AB. For ALD, the reactants are introduced separately and sequentially, in different pulse steps separated by purge step. A typical ALD cycle is composed of four sequential process steps: pulse of AC, purge, pulse of BD, purge. If the pulse steps are long enough, AC or BD could react with the pre-deposited B or A at all possible sites on the exposed surface of the substrate and finish a surface saturation reaction. After the saturation, no more sites are available, and the reaction will be self-limited. The introduction of the reactants will stop, and the residual gas purged by the inert gas. An ideal ALD cycle deposits only one monolayer of the atom. The merit of ALD is that its outstanding thickness uniformity and isotropic characteristic, since the surface reactions during the two pulse steps are self-limited.

Similar to CVD, most of ALD is thermal ALD, or it takes place at high temperature. This limits it from the applications which cannot stand the deposition temperature. To lower the deposition temperature, plasma is used to enhance the ALD reaction. The choice between the thermal ALD and the plasma-enhanced ALD (PEALD) should depend on the requirement of the application. For the deposition of high- κ and metal gate, PECVD is not a favorable technique, because the plasma might induce surface damage of the delicate gate area [61,62]. If a thermal ALD with acceptable deposition temperature is available, PEALD will be given up. In the following paragraphs, the ALD of p-metal gate and n-metal gate is discussed.

2.1. ALD of P-Type Metal Gate

The top-ranking candidates for p-type metal gate included refractory element metals such as Ru, Pt and W. It is interesting to note that all these three metals are also among the very limited number of metals which could be deposited by ALD.

Ru and RuO_x: the ALD of Ru was widely studied [63–66]. Because of its high work function (~4.7 eV) and conductive oxides, it is expected to be suitable to applications as p-type metal gate electrodes for SrTiO_x MIM capacitor for DRAM [67–69] and seed layer of Cu plating for back end of line process of CMOS [70–72]. A nice summary on the precursors available for the ALD of Ru and the deposition reactions can be found in the reference [72]. The precursors used for Ru are mainly cyclopentadienyl compounds such as RuCp₂ (Cp = cyclopentadienyl) and Ru(EtCp)₂ (Et = ethyl), and β -diketonate compounds like Ru(od)₂ (od = 2,4-octanedionato) and Ru(thd)₃ (thd = 2,2,6,6-tetramethyl-3,5-heptanedionato) [67,68]. The mechanisms of the processes are based either on oxidation of the ruthenium precursor by oxygen or on reduction by NH₃ plasma.

Although so much effort has been made, the quality of the ALD Ru layer does not seem qualified for work function metal application. Up to now, no matter which precursor used, the ALD of the Ru all have remarkable incubation cycles, inducing surface roughness [72]. They are probably matured for the application of the MIM capacitors and interconnections, but not for the work function layer of the metal gate.

Platinum: ALD of Pt has also been widely studied in the last 20 years because of its excellent chemical and thermal stability and conductivity for potential applications such as the electrodes for ultra-high κ in the cell of DRAM and those for ferroelectric dielectric in FERAM [67,73–76]. Its high work function (5.6 eV) and low resistivity (10.5 $\mu\Omega\cdot\text{cm}$) also attracted the attention for the application as p-type metal gates [77].

The ALD of platinum has been studied using two different kinds of compounds, MeCpPtMe₃ (Me = methyl) [67], and Pt(acac)₂ (acac = acetylacetonato), as precursors, and O₂, pure or in air, and H₂, as reactant [67,78]. For the ALD using MeCpPtMe₃, the precursor would dissociate when chemically absorbed on and reacted with the O in previously deposited layer. For that using Pt(acac)₂, both oxygen and hydrogen could react with the precursor, the ALD with hydrogen, however, could only grow a very poor film at low deposition rate. Mackus studied the mechanism of the ALD using MeCpPtMe₃ [79], and indicated that the ALD behavior is relative not only to the reaction between the precursor and O₂, but also to the catalytic nature of the Pt film, based on their observation of the gas products generated. The mechanism was described as a series of reactions in sequence; the combustion and dehydrogenation reactions in MeCpPtMe₃ pulse on the O covered surface, formation of a carbonaceous passivation of the surface, and the combustion of the carbonaceous layer in O pulse. It was believed that it was the carbonaceous passivation which attributes to the self-limitation and the temperature dependence of the deposition rate. Henkel's work studied the electrical performance of the Pt metal gate in the stacks with Al₂O₃, ZrO₂ and SiO₂ [76,77]. They found that the *EWf* of the ALD Pt strongly depended on the dielectric, 4.76 eV for ZrO₂, 5.22 eV for Al₂O₃ and 5.52 eV for SiO₂. The MOS capacitors using the ALD Pt on ZrO₂ and Al₂O₃ also showed good defect density control and leakage reduction.

A concern on the application of Ru and Pt as the work function metal might lie in the difficulty of wet clean. These noble metals are chemically inert and any contamination of them on the backside of the Si wafers needs a very harsh wet process to be removed. When being used as the metal gate, CMP process will inevitably induce backside contamination. This might explain why the two metals, after extensive investigations, have never been employed in front end of line of the CMOS production.

Tungsten: The ALD of W is the most successful case among elemental metal ALD processes. Thanks to sound study on the CVD of W, inorganic precursor WF₆, and reducing reactants, silane or borane compound and their reaction mechanisms have been well known. The first study on the ALD of W was reported by Klaus et al. in 2000 [80]. They studied the ALD on SiO₂ using WF₆ and Si₂H₆ and demonstrated a linear growth of W at temperatures below 350 °C, without any incubation. The mechanism of the deposition was explained as the self-limited reaction in that Si₂H₆ strips fluorine from WF_x species and the resulting SiH_yF species are subsequently removed by the next WF₆ exposure. Elam et al. [81] further studied the nucleation of the above deposition. Slightly different from the previous work, an incubation of five cycles is found, believed to attribute to the nucleation on the OH-group finalized SiO₂ surface. The ALD-W films deposited by using diborane, B₂H₆, as a reducing agent of WF₆ was reported in 2002 by Yang et al. [82] and further studied by Kim et al. [83,84]. The ALD-W process using silane, SiH₄, was also extensively investigated, based on the similar reaction mechanism consideration [85,86]. All the above works were mainly targeting the application as the seed layer of CVD for W contact plug. Wang et al. studied the ALD W on TiN using SiH₄ and B₂H₆ as the metal for filling the high aspect ratio gap of the replacement gate [87,88]. A good gap filling capability and electrical performance was demonstrated with MOSCAP and pMOSFETs. The comparison of the properties between the ALD W using SiH₄ and B₂H₆ for the replacement gate filling in the pMOSFETs revealed that the former, which is crystalline and has a much larger tensile stress (~2.4 GPa), could give superior electrical properties compared to the B₂H₆-generated layer.

ALD W is less favorable for being used as the work function layer of the metal gate, due to its near midgap work function (~4.6 eV) [89], the usage as filling metal for all-ALD gate stack is without doubt promising.

TiN: TiN was first introduced in the 1970s, deposited by reactive sputtering using Ti target and reactive gases such as NH₃ and N₂. Its excellent hardness, density, melting point and gold-like appearance attracted so much attention for the applications as abrasion-resistive or decorative coating. Quite unusual, such a nitride film has a high electrical conductivity. In semiconductor industry, it has been used as an inorganic antireflective coating for lithography [90], hardmask for low-κ patterning [91,92], and diffusion barrier for tungsten contact and Cu interconnection [93,94].

As mentioned before, TiN was successfully used as a p-metal gate in the first generation high- κ /metal gate technology. In fact, TiN is an ideal candidate for the metal gate because of its excellent thermal stability in contact with HfO₂, low resistivity and compatibility to conventional CMOS process [95–97]. Since conformality is difficult to achieve by PVD, extensive exploration of CVD techniques for TiN deposition has been carried out over the last 20 years, with variations such as PECVD [98,99], low-pressure CVD (LPCVD) [100,101], atmosphere pressure CVD (APCVD) [102,103], metalorganic CVD (MOCVD) [104,105] and low pressure metalorganic CVD [106,107].

ALD of TiN was first explored by Hiltunen et al. in 1988 [108] and by Ritala et al. in 1995 [109]. Using TiCl₄ as precursor and NH₃ as reactant, polycrystalline TiN was deposited on glass at 500 °C. It was found that the deposition rate is below 0.02 nm/cycle, corresponding to 0.1 monolayers of the (111) direction per cycle. These TiN layers have chlorine content less than the detection limit of the Rutherford Back scattering (RBS) and hydrogen impurity less than 0.4 at%. The oxygen content of the films is about 3 ± 2% in 1400 Å thick film and it is relatively higher in thinner film. The oxygen incorporation may be due to the oxidation of the film after the deposition. Thinner film is easier to oxidize. The oxidation will happen in all the other TiN films, including the films discussed in the following sections.

ALD with TiI₄ and NH₃ was also tried based on the consideration on the difference in dissociation energy between Ti-I (D₀ = 296 kJ/mol) and Ti-Cl (D₀ = 429 kJ/mol) [110]. Lower deposition temperature is expected for the ALD with TiI₄-NH₃ than TiCl₄-NH₃. The experiments showed that TiN layer could be deposited at 350 °C. At 500 °C, the deposition rates of the TiI₄-NH₃ is slightly higher than the TiCl₄-NH₃. The film deposited at 350 °C has 2 at% iodine content, and for those deposited at temperatures exceeding 400 °C, iodine content is below 0.5 at%. The oxygen content, however, was similar (10 at% at 400 °C) to the films by TiCl₄-NH₃ process. At 350 °C, 40 at% oxygen was incorporated in the film. As a result, the resistivity of the films decreased as a function of the deposition temperature.

The ALD of TiN on Si was studied by Jeon et al. [111]. Better quality of TiN was demonstrated at 350 °C with chlorine content of about 3 at%. The most important difference between these processes and that of Ritala et al. [109] is in NH₃ flow rate. Jeon et al. [111] deposited TiN films using the flow rate of 75 sccm, which is nearly 10 times higher than used by Ritala et al. [109] This might attribute to the difference in film quality at 350 °C.

The above works using Ti halides show a very low deposition rate at the temperature range compatible to CMOS process. To solve the problem, organic metal precursors were tested, based on the experience in MOCVD [112–114]. With CVD technique, TiN films could be grown at low temperatures with different titanium alkylamides [115]. Although the compounds include the Ti-N bond, external nitrogen source such as NH₃ is still needed since the simple decomposition of the alkylamides is not enough to achieve qualified films [116]. The ALD of TiN have been carried out with Ti[N(C₂H₅CH₃)₂]₄ (tetrakis(ethylmethylamido)titanium, TEMAT) and NH₃ as well [113,114]. It was found that the self-limited ALD reactions take place in the temperature range of about 150–220 °C. At higher temperatures, TEMAT decomposed and CVD type reactions became dominant. The growth rate of these films was 10 times higher than in the halide based processes, varying between 0.5–0.6 nm/cycle. This is even higher than the ideal monolayer per cycle (ML/cycle) and was explained by a model of re-chemisorption of the precursor and NH₃. The films showed low impurity level, with only 4 at% carbon and 6 at% hydrogen incorporation and excellent step coverage above 90%. J. Musschoot et al. studied the ALD of TiN from tetrakis(dimethylamino)titanium (TDMAT) [112]. Both thermal and plasma enhanced processes were studied, with N₂ and NH₃ as reactive gases. A growth rate of 0.06 nm/cycle was achieved with an optimized thermal ALD process, comparable to the ALD using TEMAT. The thermal ALD films had very high impurity level with about 37% oxygen and 9% carbon.

The above early ALD studies to deposit TiN were targeted at the application of tungsten and Cu diffusion barriers. The first study on the ALD of the TiN for the metal gate application was reported in 2002 by Lujan [117]. In their work, the thermal ALD of TiN was carried out with TiCl₄ and NH₃ at 350 °C and annealed in forming gas at 420 °C for 30 min to passivate interface states. The flatband voltage (V_{fb}) was extracted from the C-V curve and used to calculate the EWF. It was found that the V_{fb}

of the ALD TiN is comparable to that of the p-type poly-Si. The *EFW* extracted is about 5.3 eV. In the same work, they compared the C-V curve of the ALD TiN with PVD TiN and found that the PVD TiN had a mid-gap work function. The p-type *EFW* of the ALD TiN was explained as more N incorporated in the film. The processing details and growth mechanism were presented by Besling et al. and Satta et al. [118,119]. Park et al. published a work on the ALD of TiN in the same year using the same precursor and reactant [120]. They studied the W/TiN/SiO₂(3 nm)/p-Si MOS capacitors and demonstrated that the ALD-TiN has very low interfacial defect density on SiO₂. The comparison among the ALD, and CVD revealed that the ALD layer had lower level of Cl content. F. Fillot et al. studied the ALD of TiN on ALD HfO₂, using TDMAT and NH₃ [121]. The ALD of TiN was carried out at 180 °C, and gave out a layer with 27 at% Ti, 30 at% N, 37 at% oxygen and 6 at% carbon. Different from the *EFW* reported by Lujin [117], this MOALD TiN showed a *EFW* of n-types metal, ~4.2 eV. This *EFW* was attributed to the interfacial layer generated by incubation of the deposition. They detected an interfacial layer of ~2 nm in the TiN, with remarkable Ti-rich composition. To confirm this, a follow-up study was done using the same ALD to investigate the impact of the TiN thickness to the *EFW* [122]. It was found that the flatband voltage of the TiN layer below 2 nm showed strong thickness dependence. After 2 nm, the flatband voltage approach constant.

Thermal stability was the most important concern for the application of the TiN metal gate. In 2003, Westlinder et al. studied the thermal stability of the ALD TiN with capacitors of Poly-Si/TiN/SiO₂ [123]. The capacitors were annealed in the temperature range of 400 °C to 1000 °C in steps of 100 °C in an RTP furnace in N₂ ambient for 30 s. In addition, some samples were annealed in nitrogen diluted with 10 at% oxygen at 400 °C for 30 s. It was found that the work function of the TiN could remain p-type up to 700 °C and would shift to midgap after annealing at temperatures higher than 800 °C. This was concluded, based on the requirement of gate first process, as a disappointing result for the application, as the p-type metal gate cannot survive from the source/drain activation annealing at 1050 °C. In 2010, L. Wu [124] reported a study on the thermal stability of the TiN/HfO₂/Si stack, where HfO₂ was deposited by ALD using HfCl₄ and water, and TiN by ALD using TiCl₄ and NH₃. The work focused on the chemical stability of the stack after annealing at 1000 °C and revealed unsatisfactory thermal stability again.

It needs to be noted that the above thermal stability studies misfocused at a wrong temperature range, based on the assumption that a metal gate step must be processed before the activation anneal. Actually, if a gate last process employed, the thermal stability of the p-type V_t up to 700 °C is quite positive. In 2015, Brennan compared the electric properties of the TiN/SiO₂/Si MOS capacitor (MOSCAP) and CMOSFETs of FDSOI with the TiN deposited by PVD and PEALD to trace the plasma damage to the dielectric [125]. The PEALD was carried out using TDMAT and H₂/N₂ under well controlled plasma condition for much lower ion dose and energy compared to PVD. The MOSCAP with PVD TiN clearly showed larger trap density and higher interfacial defect density than the PEALD. The n- and p-MOSFETs with PVD and PEALD TiN had similar electrostatic performance, with very good short channel performance, say small subthreshold swing, DIBL and V_t roll-off. The gate dielectric quality of them, however, are remarkably different. The gate leakage of those with PVD TiN was much higher than PEALD, consistent with the high density of defects in the bulk SiO₂ leading to trap-assisted tunneling and significantly higher gate dielectric failure probability. Taken together, the electrical results suggested that during PVD of TiN, the gate dielectric was damaged by energetic ions and ultraviolet (UV) photons which break Si-O bands and leave defects states, inducing increased gate leakage and reliability issues.

In summary, most of the research works on TiN ALD were carried out using TiCl₄ and NH₃ or TDMAT and NH₃, with and without plasma enhancement. In most cases, the chloride based ALD has a p-type work function [117,123], while the TDMAT-based process gave a n-type work function [121,125], compared to the midgap one of the TiN by PVD [126]. It was attributed to the different chemical composition of the interfacial layer. The TiCl₄-based process could generate a Ti-rich interfacial layer, and thus had a Ti-like work function. The PVD TiN had a Ti:N ratio near 1:1, and as a result, had a

work function at midgap. The TDMAT process generated TiN with high oxygen and carbon content, inducing n-type metal behavior. Real mechanism of the difference might be more complex. Many works revealed that the *EFW* of the TiN in the gate stacks shifted with the thickness [97,127], post deposition anneal [97,128], microstructure of the TiN [129,130] and different doped ions such as Al [44], As [131], P/BF₂ [132]. Careful engineering of the ALD TiN is always needed for the application in real gate stacks.

2.2. ALD of N-Type Metal Gate

Compared to the p-type metal gate, the selection of n-type metal gate is more difficult. The first demonstration of a dual-metal gate CMOS using Ti as n-metal gate and Mo as p-metal gate, respectively, together with SiO_xN_y as dielectric, was reported in 2002. The device showed negligible gate depletion, remarkably reduced gate leakage and acceptable channel mobility [133]. The TiN/Ti double layer was deposited by sputtering, targeting at a theoretical work function of metal Ti on SiO_xN_y of 4.36 eV. The *EFW* extracted, however, from the C-V measurements is 4.56 eV, near the midgap value for TiN. The complete silicidation of the poly-silicon gate electrode, called FUSI, was also proposed for dual gate application [134]. In the FOSI process, poly-Si is first deposited on SiON and doped by B and As for pMOS and nMOS, respectively. Afterwards, a thick enough Ni layer was deposited on the poly-Si, followed by annealing for silicidation. Two different work functions, ~4.5 and ~4.9 eV for NMOS and PMOS, respectively, were obtained. This approach attracted much attention at beginning [135], due to its integration simplicity, but was finally abandoned due to the difficulty to achieve low enough *V_t* devices. Another dual metal gate integration work [136] used PVD Ru as p-type metal and PVD TaC as n-type metal, and HfO₂ as dielectric, demonstrated good device behavior. As mentioned before, the first industrial high- κ /metal gate technology for 45 nm node, reposted in 2007, used TiAl alloy as n-type MOSFETs [25]. The capacitor using AlTi n-type metal and HfO₂ showed an ideal C-V curve and n-type *EFW* [45]. In all the above works, the n-type metal gate were deposited by PVD.

The first work on ALD of n-type metal was reported in 2007 by Triyoso using TaC_y as the metal gate and HfO₂ as the dielectric [137]. The TaC_y films deposited by PEALD using organic precursor and a carbon containing gas was near-stoichiometric, nitrogen free, and had low oxygen impurities and amorphous carbon content. Excellent electrical properties using this TaC_y/HfO₂ stack were demonstrated, including work function between 4.77 and 4.54 eV and low fixed charge density ($\sim 2\text{--}4 \times 10^{-11} \text{ cm}^{-2}$). Jeon et al. studied the ALD of TiN-TiC mixture using a fine designed precursor and process [138]. The TDMAT was used as precursor for Ti, H₂ and NH₃ as reactants. The sequence of one ALD cycle was designed as 1s TDMAT pulse/3s Ar purge/3s H₂ plasma/1s (H₂-NH₃) preflow/3s (H₂-NH₃) plasma/3s Ar purge. The temperature range of pure ALD mode deposition was found between 150 °C and 200 °C, generating a layer of TiN. The deposition between 200 and 350 °C formed a mixture of TiC and TiN. The higher the temperature, the higher the TiC content will be. The *EFW* extracted from C-V measurement of MOSCAPs showed a decreasing trend from 5.02 eV for TiN to 4.8 eV for 18.5% TiC and 4.6 eV for 39% TiC. Such a tunable *EFW* was promising for dual gate CMOSFETs and multi-*V_t* applications. The CVD mode for TiC formation seemed a potential risk of causing processing variation.

Based on the encouraging results of PVD TiAl n-MOSFET [25] and the n-type *EFW* of ALD of TaC and TiC, the authors of this review started a series of systematic studies on the ALD of the TiAlC and TaAlC [139]. In 2015, we investigated the thermal ALD of TiAlC using TiCl₄ as Ti precursor and trimethylaluminum (TMA) as Al precursor on ALD HfO₂ surface [139–142]. One deposition cycle consisted of TiCl₄ pulse, N₂ purge, TMA pulse and N₂ purge. The deposition was studied in the temperature range of 300 °C to 400 °C. It was found that the major content of the film deposited at 400 °C is TiAlC, with 55 at% C, 35 at% Ti, 8 at% Al and small amount of Cl. The linear growth curve showed no incubation. The layer was amorphous and had low roughness ($\sim 0.33 \text{ nm}$ by AFM) and low resistivity. The C-V measurement of the MOSCAP with a structure of W/TiN/TiAlC/HfO₂/SiO₂/Si revealed no hysteresis, implying low defect density. The TiAlC layers processed with different thickness

showed a tunable *EFW* range from 4.49 eV to 4.79 eV. In a follow-up work [142], we found that the layer deposited at lower temperature such as 200 °C had metal Ti content and will be oxidized when exposed to air after the deposition. The growth mechanism was proposed as follows as there are a set of reactions during the ALD in parallel: first, the reductive behavior of TMA forms ethane. The reaction between TiCl_4 and TMA, generates Ti metal, which will react with the ethane, forming Ti-CH_2 , TiCH=CH_2 and TiC fragments. The Al generated by the decomposition of TMA alloyed in and formed a final TiAlC layer. A comparison study between TiAlC and TiAlN was carried out [140] using three combinations of TiCl_4 , TMA and NH_3 pulse separated by N_2 purge for TiAlN ALD and the ALD of TiAlC is the same to the previous works. Table 1 listed the processing sequence and the properties of the layers and Figure 10 displays the *EFW* of the four work function layers (WFL) in the $\text{W/TiN/WFL/HfO}_2/\text{SiO}_2/\text{Si}$. One can see that the n-type *EFW* does not only correlate to the Al content, but to the chemical bonds formed. The layers with only Al-N bonds did not show large *EFW* shift, while that with Ti-C did.

Table 1. The comparison of the ALD sequence and properties of and TiAlX .

	Mode A	Mode B	Mode C	Mode D
Sequence	$\text{TiCl}_4/\text{NH}_3/\text{TMA}/\text{NH}_3$	$\text{TiCl}_4/\text{TMA}/\text{NH}_3$	$\text{TiCl}_4/\text{NH}_3/\text{TMA}$	TiCl_4/TMA
Elements (at%)	Ti25,Al31,N43	Ti67,Al4,C3,N25	Ti76, Al2, C5,N12	Ti35,Al8,C55
Bonds	Ti-N, Al-N	Ti-N, Al-N, Ti-C	Ti-N, Al-N, Ti-C	Ti-C, Al-C
<i>EFW</i> (eV)	~4.79	~4.74	~4.68	~4.5

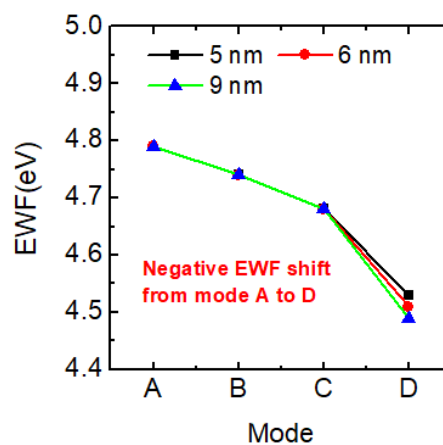


Figure 10. *EFW* comparison between the ALD TiAlN and TiAlC .

The only deficiency of the ALD TiAlC using TiCl_4 and TMA is its relatively small *EFW* shift. Compared to 0.44 eV for the high performance nMOSFETs, the *EFW* of the TiAlC from TMA still had room for improvement. In order to further tune the *EFW*, we studied the ALD using TiCl_4 and Triethylaluminum (TEA) [142]. TEA is a metal organic precursor with special β -hydrogen, which could lead to H_2 elimination, and generate Al intermediate [143]. Higher Al doping level was thus expected in the TiAlC deposited by ALD using TEA to replace TMA. The same ALD sequence is used to study the growth behavior at different temperatures between 250 and 350 °C. We found that the deposition in this temperature range saturated after the pulse time of TEA was over 10 sec, showing the typical self-limiting characteristic of ALD. The deposition rate was two times higher than that of the TMA process. A linear growth at 375 °C was found without incubation. The layer deposited at 375 °C has 24 at% Ti, 35 at% Al and 40 at% C. The chemical bonds detected by XPS are Ti-C, Al-C and Al-Al. The C-V curves of the MOSCAP with the same structure to the previous work were used to extract the *EFW*. The *EFW* of 10nm TiAlC layer tested in the stack of 75 nm W/2 nm $\text{TiN}/\text{TiAlC}/3\text{nm HfO}_2/\text{SiO}_2/\text{Si}$ varied with temperature. It decreased from 4.46 eV to 4.24 eV when the growth temperature increased from 250 °C to 375 °C. The *EFW* deposited at 375 °C decreased along with the TiAlC thickness and

after over 6 nm retained constant. The MOSCAP again had good electrical behavior, including low defect density and low leakage through the high- κ dielectric of $EOT \sim 0.7$ nm. The EFW tuning ability found here makes TiAlC deposited using $TiCl_4$ and TEA a very promising candidate as n-metal in all-ALD gate stack and multi- V_t applications.

The ALD of TaAlC was investigated using $TaCl_5$ with TMA and TEA as well with a similar method to that of TiAlC [144,145]. A very similar trend and comparable EFW tuning range had been found to those of the TiAlC from $TiCl_4$. The properties of the TiAlC and TaAlC with different Al precursors are summarized in Table 2. From Table 2, one can see that the properties of the TiAlC and TaAlC is so similar that it is easy to correlate the EFW shift with the Al in Al-C and Al-Al bonds. Considering the EFW requirements displayed in Figure 9, the lowest EFW shown in Table 2 can meet not only the need of FinFETs and GAA FETs, but also that of planar NMOSFETs.

Table 2. Comparison of the properties of the TiAlC and TaAlC layers.

Precursors	TiAlC		TaAlC	
	$TiCl_4$ + TMA	$TiCl_4$ + TEA	$TaCl_5$ + TMA	$TaCl_5$ + TEA
Composition at%	Ti35, Al18, C55	Ti24, Al34, C40	Ta 40, Al10, C44	Ta38, Al32, C38
Chem. bonds	Ti-C, Al-C	Ti-C, Al-C, Al-Al	Ta-C, Al-C	TaC, Al-C, Al-Al
Temp range ($^{\circ}C$)	300–400	250–375	300–400	250–375
EFW (thick.)	4.49 eV–4.79 eV	4.44 eV–4.28 eV	4.74 eV–4.49 eV	4.65 eV–4.26 eV
EFW (temp)	4.73 eV–4.53 eV	4.46 eV–4.24 eV	4.60 eV–4.54 eV	4.46 eV–4.26 eV

3. Conclusions

A review on the ALD of metal gate for both NMOSFETs and PMOSFETs based on the state-of-the-art of the ongoing research was presented. The discussion starts with the introduction to the necessities of technical transition from poly-Si/SiO₂ to high- κ /Metal gate and the demand for the ALD of metal gates due to the special challenge the 3D device such as FinFETs and GAA-FETs has to face. The concepts of EOT and EFW , and the methods to experimentally extract them are discussed by quotation of the theory on the energy band structure. The difference in the EFW target of the conventional planar CMOSFETs and the 3D devices such as FinFETs and GAA-FETs are discussed as the starting point of material selection. The research works on the ALD of the p-type and the n-type work function metals are cited to tease out the logic of the technical evaluation and to figure out the solution for future generations.

Following conclusions could be highlighted:

- (1) Based on the accumulation of the experimental data, the industry has found the high- κ /metal gate solution for the planar CMOSFETs, with ALD HfO_2 as the gate dielectric, PVD TiAl as the n-type metal gate and PVD TiN as the p-type metal gate, in a replacement gate process. The successful development of the dual metal gate technology seems to originate from the encouraging C-V measurement results by Kesapragada et al. [45], showing a 1 V separation between the MOSCAP using PVD TiAl and PVD TiN.
- (2) The ALD of the three element metal candidates, Ru, Pt and W, has attracted much attention. After great efforts, the deposition technique has not yet matured for the application of the p-type metals.
- (3) The ALD using $TiCl_4$ as precursor for Ti and NH_3 as reactant could deposited TiN with p-type EFW . While the TiN deposited by organic metal precursors with NH_3 has n-type EFW and that by PVD has a EFW near the midgap of Si.
- (4) The TiAlC and TaAlC deposited by TEA has a wide EFW tuning range from 4.65 eV to 4.26 eV, by varying the thickness. It is the Al-C and Al-Al bonds that induce these large EFW shifts. The Al-N bands does not have the EFW shift capability.
- (5) The ALD W deposited by WF_6 and SiH_4 is an ideal filling metal for pMOSFETs, which shows not only excellent fillability, but also strong tensile stress helpful to enhance the channel mobility.

- (6) For GAA-FETs in future generations, an ideal dual metal scheme could be all ALD stacks, with structure of W/TiN/TiAlC/HfO₂/SiO₂/Si for n-type FETs, and W/TiN/HfO₂/SiO₂/Si for p-type FETs, or replacing the TiAlC with TaAlC. The wide EWF tuning range of the Al-containing carbides might enable also the application for multi- V_t devices.

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