applied sciences

MDPI

Article

Comparison of Various Factors Affected TID Tolerance in FinFET and Nanowire FET

Hyeonjae Won †, Ilsik Ham †, Youngseok Jeong and Myounggon Kang *

Department of Electronic Engineering Korea National, University of Transportation, Chungju-si 27469, Korea
* Correspondence: mgkang@ut.ac.kr; Tel.: +82-43-841-5164
† Those authors contributed equally to this work.

Received: 29 June 2019; Accepted: 29 July 2019; Published: 3 August 2019

Abstract: Analysis of the radiation effects in a device is of great importance. The gate all around (GAA) structure that contributes to device scaling not only solves the short channel effects (SCE) problem but also makes the device more resistant in radiation environments. In this article, the total ionizing dose (TID) simulation of nanowire FET (NW) and FinFET was performed. Both these devices were compared and analyzed in terms of the shift of threshold voltage (V_T). The channel insulator was composed of two materials, SiO_2 and HfO_2. To improve the accuracy of the simulation, the interfacial trap parameter of SiO_2 and HfO_2 was applied. Based on the simulation result, the NW with a larger oxide area and larger gate controllability showed less V_T shift than that of the FinFET. It was therefore proved that NW had better TID resistance characteristics in a radiation environment. The gate controllability was found to affect the TID effect more than the oxide area. In addition, we analyzed the manner in which the TID effect changed depending on the V_{DD} and channel doping.

Keywords: total ionizing dose (TID); radiation; threshold voltage (V_T); nanowire FET; gate-all-around (GAA); FinFET; TID tolerance

1. Introduction

The effects of the total ionizing dose (TID) on electronic devices are critical issues in various fields such as space and nuclear applications. To reduce the radiation effects on the electronic components, three radiation hardening methods have been widely considered: radiation hardening by process (RHBP), radiation hardening by shielding (RHBS), and radiation hardening by design (RHBD) [1–4]. The international thermonuclear experimental reactor (ITER) studies the TID effect for the development of a precise remote control system [5]. Electronic equipment operating in a radiation environment is subject to radiations that lead to defects in transistors. The TID effects, single event effects (SEEs), and displacement damage (DD) can lead to disturbances in the reliable operation of semiconductor devices due to radiation [6–10]. In particular, in the TID effect, the trapped holes in the oxide of transistor in the electron hole pairs (EHP) are caused by radiation and change in the threshold voltage (V_T) [11]. The hole trapped in the oxide results in the inversion charge of the channel region and leads to change in V_T. In particular, nanoscale devices can affect other static and dynamic parameters [12]. Therefore, the reliability of the device is degraded. The devices with a 3D gate structure can solve the SCE problem and enable continuous scaling [13–15]. In particular, FinFET, which has a tri-gate structure, and NW, which has a gate all around (GAA) structure, are being studied as effective solutions for device miniaturization [16]. Therefore, both structures devices must be studied for mitigating the radiation effects. In this paper, the TID simulation of NW and FinFET was used to analyze that received more of the TID effect, depending on the structural part of the device. The experiments were performed considering the oxide area and gate controllability, which are the structural elements affected by the TID effect. For a more accurate comparison, the TID simulation was performed by calibrating the size

and current level of the NW and FinFET. Through these experiments, compared to the FinFET, we observed that the V_T of the NW changed insignificantly and that this device was more resistant in the radiation environment. This result shows that gate controllability is more effective for causing radiation tolerance than the oxide area. However, the oxide area of the hole trap is a key factor in the TID effect. As the oxide area increases, the number of trapped holes also increases and consequently, the reliability of the device is further degraded. However, by introducing the GAA structure, the gate controllability can be improved to suppressing the TID effect in the oxide area. In addition, the TID characteristics were confirmed by changing the V_{DD} and channel doping, which affect the resistance to the TID effect. Therefore, the importance of improving gate controllability, which is a method of suppressing the TID effect, is herein presented.

2. Simulation Methodology

2.1. Design Structure for TID Simulation

Prior to the simulation, the NW was stacked in five stages to match the current level and device size. Table 1 presents the basic physical device parameters used in this study. With the use of a 3D technology computer-aided design (TCAD) simulation tool, the FinFET and 5ch-NW were similarly constructed (Table 1). T_{fin} is the FinFET width, D_{nw} is the 5ch-NW diameter, L_g is the channel length, H_{fin} is the FinFET height, and H_{nw} is the 5ch-NW's total height. In addition, the FinFET was manufactured by referring to the International Technology Roadmap for Semi-conductors (ITRS) [17]. Figure 1 shows the TCAD structure of the FinFET and 5ch-NW.

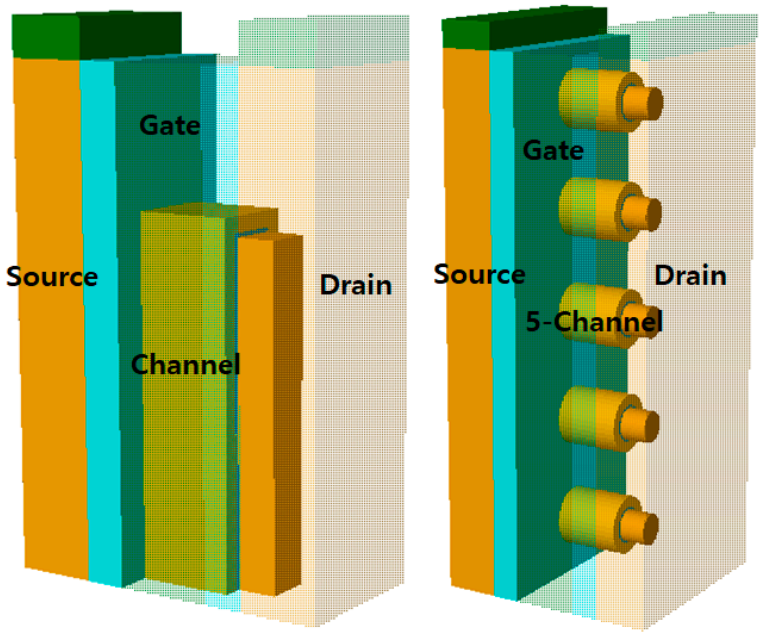

Figure 1. 3D technology computer-aided design (TCAD) structure of the FinFET and 5ch-nanowire FET (NW). (**Left**) FinFET, (**Right**) 5ch-NW. The 5ch-NW was stacked in five stages to match the FinFET's current level and device size.

The electrodes of the devices were made of tungsten, the body of silicon, the *p*-type doping was boron, and the *n*-type doping was phosphorus. The devices placed SiO_2 (0.5 nm, k = 3.9) and HfO_2 (2 nm, k = 25) on the FinFET and 5ch-NW channel insulator material. The equivalent oxide thickness (EOT) can be calculated using Equation (1).

$$\mathrm{EOT} = \frac{(\mathrm{SiO_2}\ k)}{(\mathrm{High}\ k)}(T_{Hi-k}) \quad (1)$$

Table 1. Design specifications of the FinFET and 5ch-NW.

Condition Factor	FinFET	5ch-NW
S/D Doping	1×10^{21} (cm^{-3})	1×10^{21} (cm^{-3})
Channel Doping	1×10^{16} (cm^{-3})	1×10^{16} (cm^{-3})
EOT	0.812 (nm)	0.812 (nm)
T_{fin}, D_{nw}/L_g	6/12 (nm)	6/12 (nm)
H_{fin}, H_{nw}	42 (nm)	30 (nm)
Total area (HfO_2 + SiO_2 + Silicon)	489.5 (nm^2)	474.9 (nm^2)
Oxide area (HfO_2 + SiO_2)	237.5 (nm^2)	333.6 (nm^2)
Parameter explanation		
T_{fin}: FinFET's width	D_{nw}: 5ch-NW's diameter	
L_g: channel length	H_{fin}: FinFET's height	
H_{nw}: 5ch-NW's total height		

The electrical properties were also calibrated for a fair comparison of the TID effects. Figure 2 shows the I_D-V_G characteristics with the FinFET and 5ch-NW and demonstrates that the electrical characteristics of FinFET and 5ch-NW were calibrated.

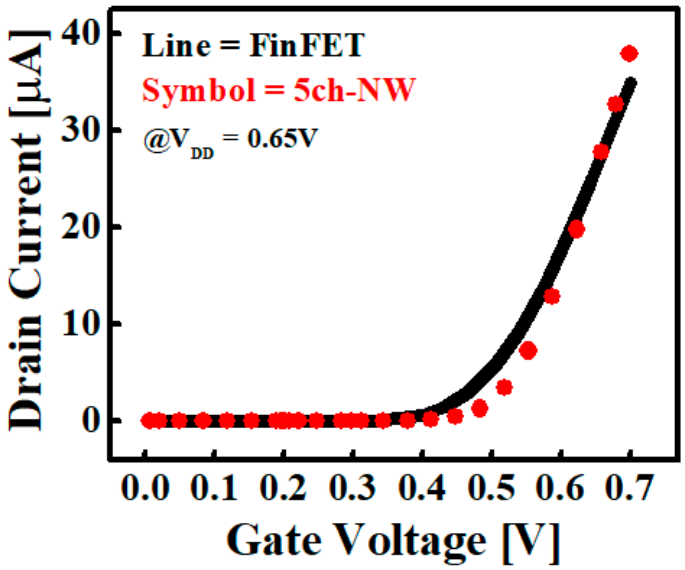

Figure 2. Black line is the I_D-V_G curve of the FinFET and the red symbol is the I_D-V_G curve of the 5ch-NW and shows the calibrated FinFET and 5ch-NW's I_D-V_G curve characteristics for similar conditions. Both were extracted by sweeping V_G from 0 to 0.7 V when V_{DD} = 0.65 V.

2.2. TID Simulation of Various Factors

The TID simulation used the Silvaco victory device software [18]. The Klaassen model used in the simulation reflects various parameters such as electron and hole mobility, trap parameters, and recombination parameters [19–23]. The trap-detrap model parameters in the oxide region by radiation were used in the same way as in [24]. For a more precise simulation, the interfacial trap coefficient between SiO_2 and HfO_2 was calculated by introducing an interfacial trap parameter between the insulators. We generated the corresponding I_D-V_G curves by applying the TID effect. The radiation source was a γ-ray irradiation performed using a Co^{60} source [25]. Radiation was irradiated 1 rad/s for the devices. The input V_{DD} was equal to 0.65 V and the sweep V_G was in the range 0–0.7 V for the electrical characteristics of 100 Krad, 1 Mrad, 10 Mrad, and 100 Mrad. The simulation confirmed the TID effect on the structural aspects of the FinFET and 5ch-NW. All comparative calculations were performed with the same efficiency as the charge capture [9].

To observe V_{DD} influence, the V_{DD} was simulated by varying it from 0.65 V to 0.1 V. The V_T shift amount was compared based on the V_{DD} in the TID simulation. We applied the V_{DD} conditions mentioned above to FinFET and 5ch-NW, and the V_G sweep was done in the same way from 0 V to 0.7 V.

The TID characteristics of the two aforementioned devices according to the changed channel doping concentration were confirmed as the channel doping concentration changed. The TID effect change was confirmed by the V_T shift. The channel doping concentration was changed from 1×10^{16} cm^{-3} to 1×10^{18} cm^{-3}. After changing the channel doping of both the devices, the initial simulation without radiation was compared to the simulation with TID of 10 Mrad.

3. Results and Discussion

Figure 3 shows the basic structure of the FinFET and 5ch-NW as well as the interface hole trap after TID simulation. Figure 3a,b show that the physical thickness and EOT of the insulator were the same. Figure 3c,d show the interface hole traps of the FinFET and 5ch-NW, respectively. The hole traps at the interface between SiO_2 and HfO_2 was confirmed to improve simulation accuracy. Figure 3c,d also show that the hole-trapped interface between Si and SiO_2.

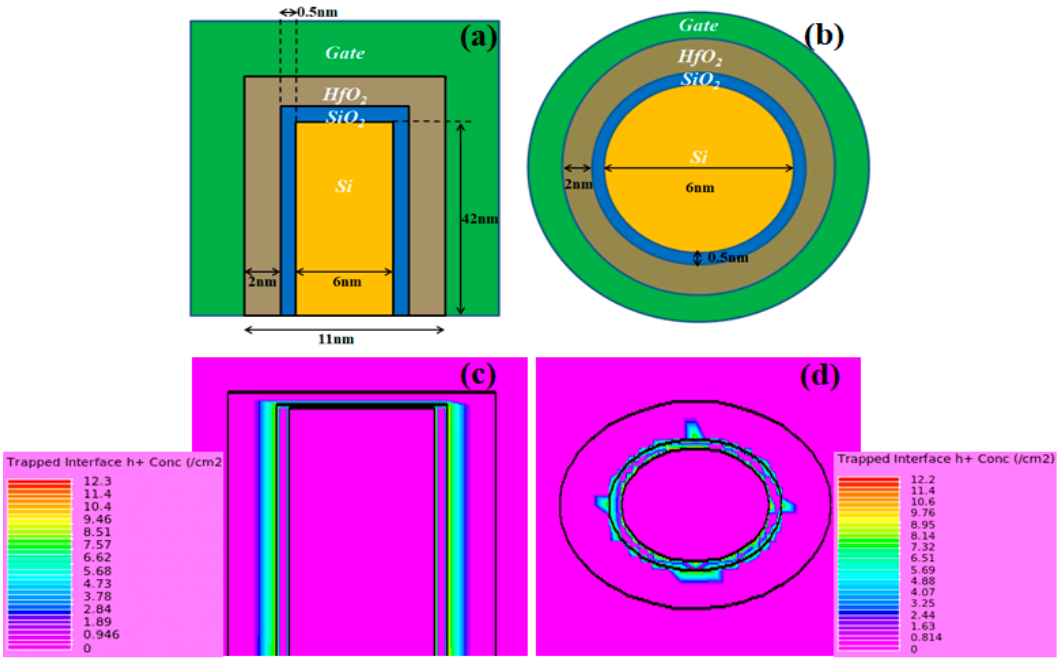

Figure 3. Structure of each device and the interface hole traps after the total ionizing dose (TID) simulation. (**a**) The structure of the FinFET; (**b**) the single-stage structure of 5ch-NW; (**c**) the interface trap of the FinFET; (**d**) the interface trap of the 5ch-NW.

TID is a phenomenon generated because of the accumulation of radiation irradiated to the device. When the radiation penetrates through the insulator region of a device, EHP is generated through the ionization process. Due to their difference in mobility, the generated electrons rapidly diffuse out from the dielectric region. However, some holes are captured in the insulator region trap sites, thereby increasing the leakage current and causing a negative V_T shift [26,27].

Figure 4 illustrates the TID simulation method. In Figure 4a, V_G according to the transient time takes the shape of a pulse. The I_D-V_G curve changes depending on if the pulse is rise or down. In this figure, we can see the upsweep when the purse is rising. Additionally, we can see the downsweep when the purse is going down. The width of the pulse is related to the amount of dose. We can see the simulation results when the pulse is end. The results show the V_T shift and that means the hole is trapped in the interface.

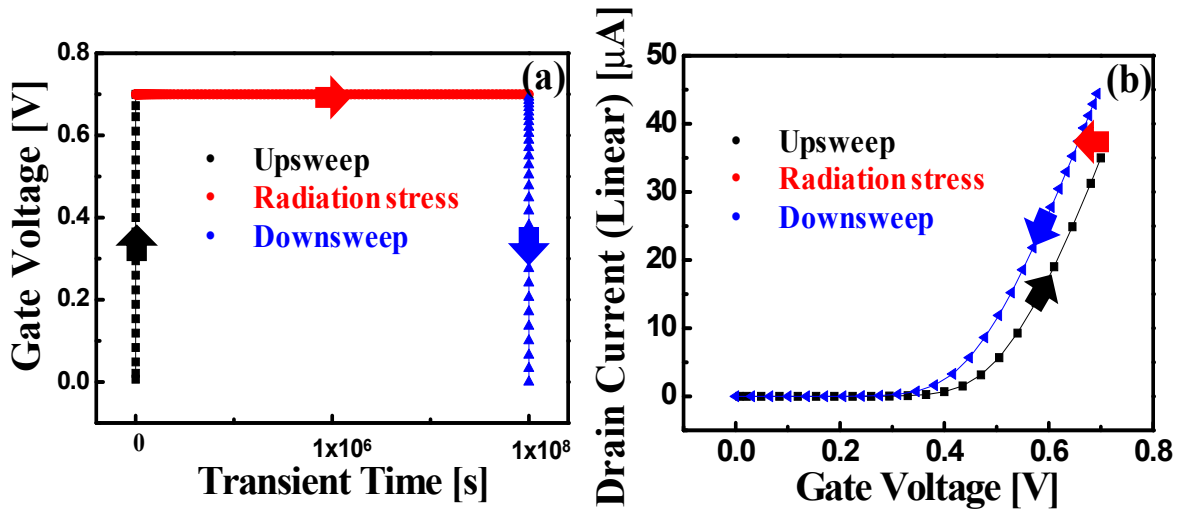

Figure 4. TID simulation method of the FinFET. (**a**) The V_G-transient time; (**b**) the V_T shift due to the interface trap.

Figure 5 shows the electrical characteristics of the device with the TID effects for each radiation level. We extracted the V_T when the drain current was 1×10^{-7} [A] using the current constant method in Figure 5. It shows that the V_T shifted because the holes generated by the radiation were trapped in the insulator. Therefore, the shift tendency increases with the increase in the TID. In Figure 5, relatively low levels of radiation did not affect the transfer characteristics. Due to the nanoscale oxide area, the hole trap caused by the radiation was reduced. Additionally, the GAA structure increased the gate holding power and reduced the effect of the trapped charge.

Figure 5c,d show the log scale of I_D-V_G where the off current increase phenomenon, caused by the TID effects, was confirmed. In the figure, we can see that the off current change of 5ch-NW was less than that of FinFET. This shows that the effect of suppressing the SCE also suppressed the TID effects. Table 2 presents the V_T value for each TID amount of both the FinFET and 5ch-NW.

Table 2. V_T data of each device according to the amount of TID.

V_{DD} = 0.65 V	FinFET (V_T)	5ch-NW (V_T)
Initial	329 mV	402 mV
100 k (rad)	325 mV	402 mV
1 M (rad)	323 mV	400 mV
10 M (rad)	312 mV	388 mV
100 M (rad)	281 mV	360 mV

Figure 5e,f show the transconductance of the FinFET and 5ch-NW. It can be noticed that the transconductance increases with radiation, as shown in Figure 5e,f, because of the decrease of V_T and the flow of more drain current at the same gate voltage.

Figure 6 shows the details the V_T shift for each device. In the case of FinFET, a 48 mV shift from 100 Mrad than the initial was observed. In the case of the 5ch-NW, roughly 42 mV shift from 100 Mrad than the initial was observed. The 5ch-NW therefore showed less V_T shifts than the FinFET, as per the simulation results.

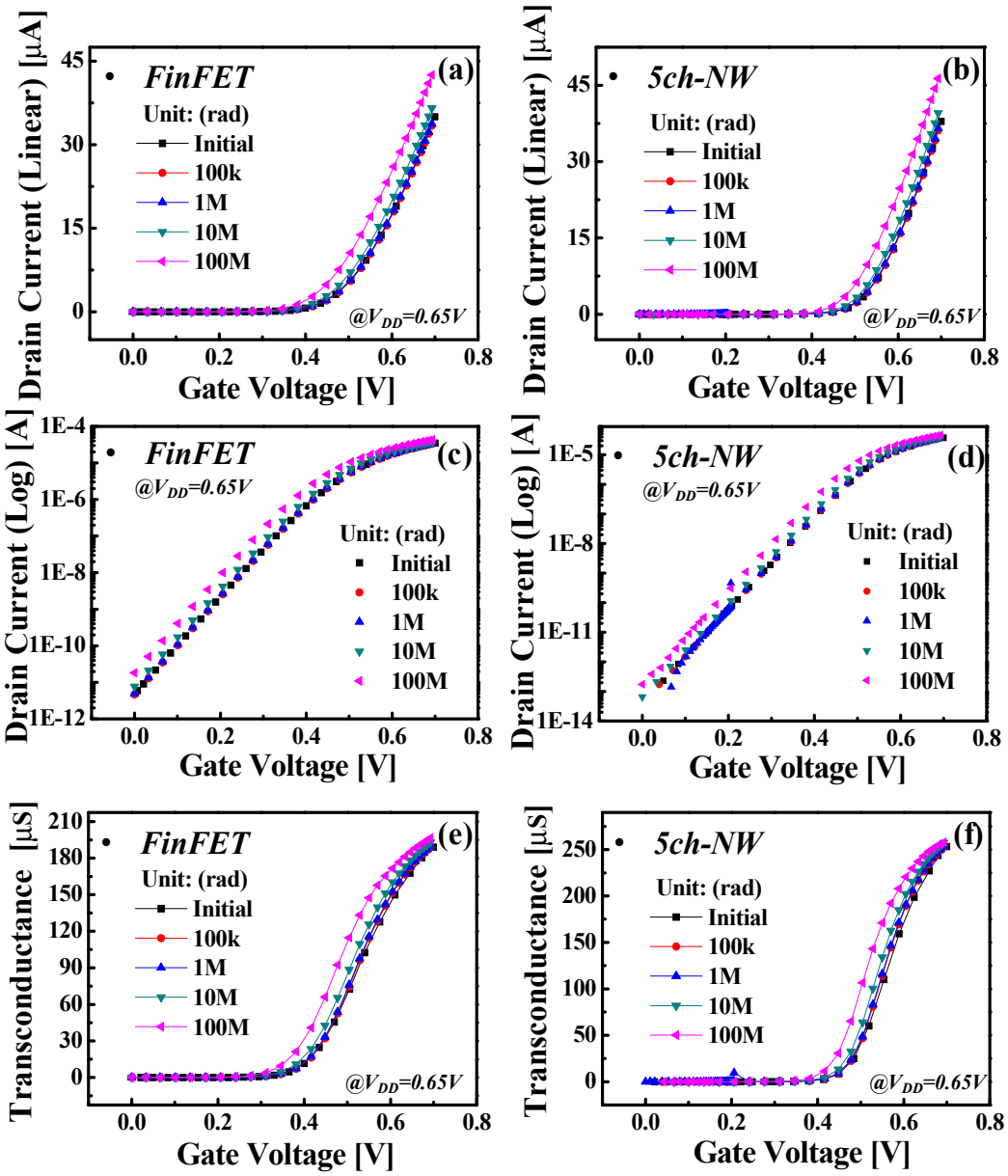

Figure 5. I_D-V_G curve shifts with an increasing radiation dose up to 100 Mrad for (**a**) FinFET, and (**b**) 5ch-NW. The I_D-V_G curves were extracted at 100 krad, 1 Mrad, 10 Mrad, and 100 Mrad. These graphs were obtained by sweeping V_{DD} = 0.65 V and V_G from 0 V to 0.7 V when the total dose was reached. (**c**,**d**) are the I_D-V_G curve graph of the log scale of each device according to the TID effect. (**c**) is the FinFET's log scale curve, (**d**) is the 5ch-NW's log scale curve, (**e**) is the FinFET's transconductance graph, and (**f**) is the 5ch-NW's transconductance graph.

The 5ch-NW had a larger oxide area than the FinFET. Therefore, it was reflected to have a greater TID effect and a larger V_T shift. However, these were less in the case of the 5ch-NW because of superior gate controllability. The GAA structure improved the gate controllability because all the sides are covered with the gate. This does not only address SCE, but also improves tolerance to the TID effect [28]. Structurally, the oxide area of 5ch-NW was approximately 96.1 nm^2, which is larger than that in FinFET. However, the TID effect in 5ch-NW was less than that in FinFET in the above-mentioned experiment. Therefore, it shows that the gate controllability factor is more crucial than the oxide area in TID effect suppression.

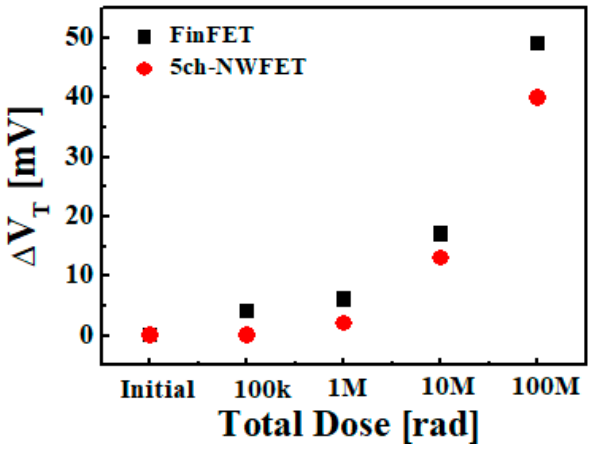

Figure 6. FinFET and 5ch-NW extracted the V_T shift amount according to the increasing TID.

Figure 7 depicts a graph of the TID simulation result with V_{DD} set at 0.1 V and 0.65 V. In Figure 7c, at higher radiation, the V_T shifts significantly than in the case of lower radiation because of the hole traps in the FinFET and 5ch-NW. Additionally, because of the strong TID effect, the FinFET and 5ch-NW are less affected by V_{DD} at the higher radiation. However, the FinFET is affected by V_{DD} when low radiation is applied, because the gate controllability of the FinFET is weaker than that of the 5ch-NW. Therefore, the 5ch-NW is not significantly affected by V_{DD}.

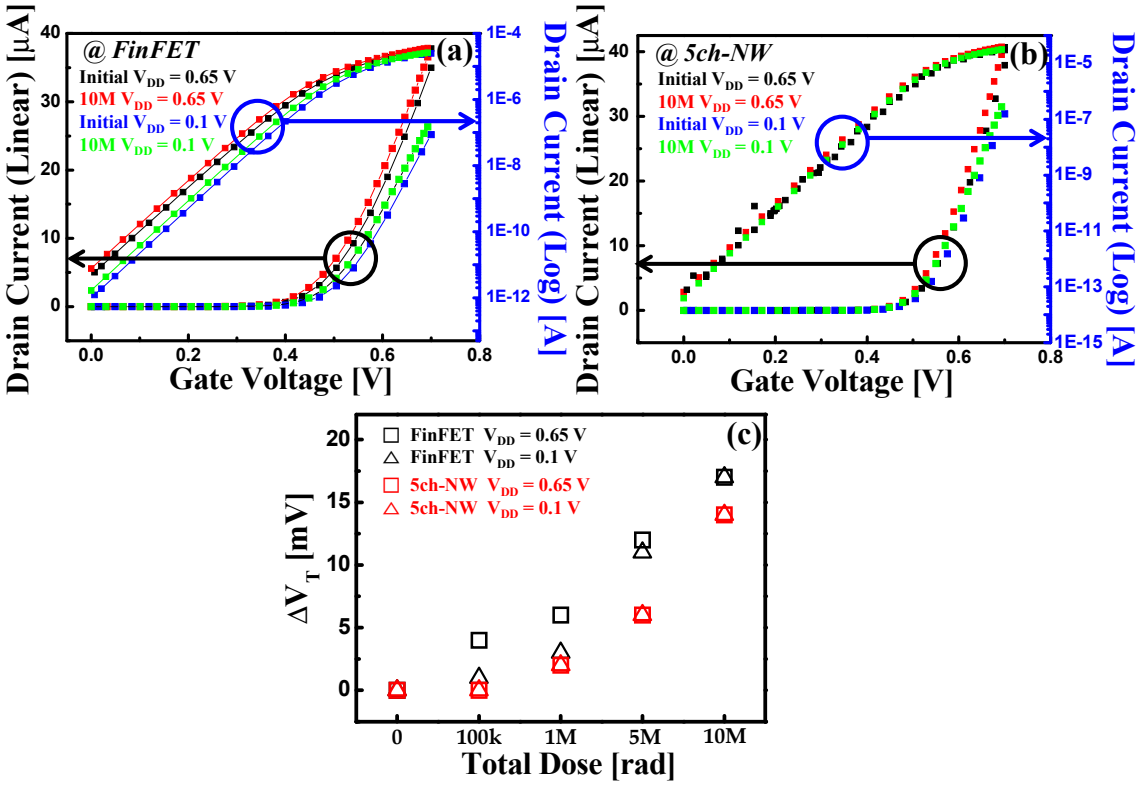

Figure 7. Simulation results according to V_{DD} variation (**a**) FinFET curves, (**b**) 5ch-NW curves. (**c**) Comparison of the V_T shifts of FinFET and 5ch-NW.

Table 3 lists the V_T shift according to the variation of V_{DD}. In the case of 5ch-NW, there was almost no change owing to its better gate controllability, which reduced the V_{DD} influence.

Table 3. V_T shift according to the V_{DD} variation.

	FinFET (ΔV_T)		5ch-NW (ΔV_T)	
	V_{DD} = 0.1 V	V_{DD} = 0.65 V	V_{DD} = 0.1 V	V_{DD} = 0.65 V
100 k (rad)	1 mV	4 mV	0 mV	0 mV
1 M (rad)	3 mV	6 mV	2 mV	2 mV
5 M (rad)	11 mV	12 mV	6 mV	6 mV
10 M (rad)	17 mV	17 mV	14 mV	14 mV

Figure 8 shows that the I_D-V_G changed due to the TID effect. Figure 8a shows the I_D-V_G of the FinFET, and Figure 8b shows the I_D-V_G of the 5ch-NW. We can see that the V_T changed and how it was different if the channel doping was changed. First, the V_T decreased due to the TID effect, and the V_T decreased on the same way when the channel doping was changed. In the case of channel doping at 1×10^{16} cm^{-3}, it was confirmed that the V_T variation due to the TID effect was similar to the V_T variation at 1×10^{18} cm^{-3}. Therefore, the V_T increased when the channel doping increased in both the FinFET and 5ch-NW, and the V_T decreased due to the TID effect at both 1×10^{16} cm^{-3} and 1×10^{18} cm^{-3}.

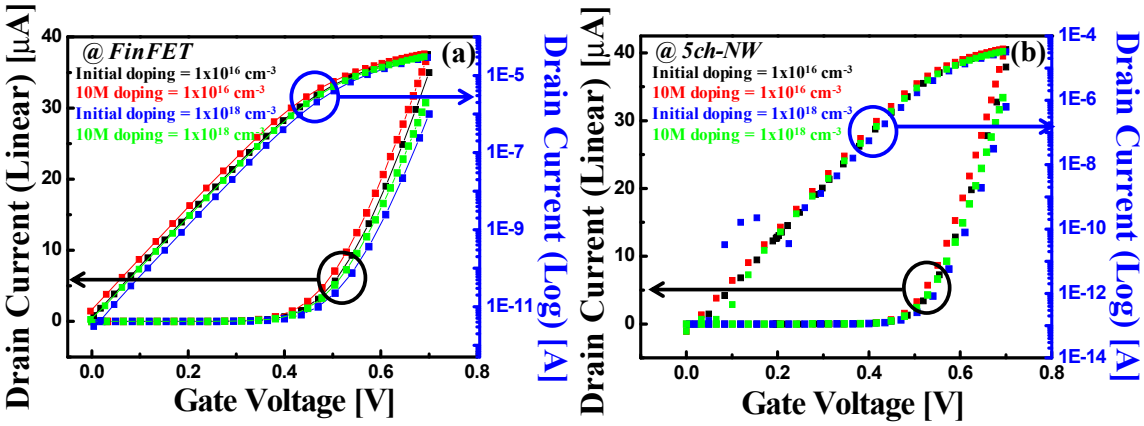

Figure 8. The simulation results according to channel doping. (**a**) FinFET, (**b**) 5ch-NW.

Table 4 lists the V_T variation based on channel doping. The doping of the FinFET changed from 1×10^{16} cm^{-3} to 1×10^{18} cm^{-3}, and that of the 5ch-NW was also changed in a similar way. Increasing channel doping in FinFET and 5ch-NW caused an increase in the initial V_T. In addition, when radiation was applied, the V_T and the TID effect decreased for all cases, regardless of doping. When the doping was changed to 1×10^{18} cm^{-3}, the change in V_T was less in the 5ch-NW than that in the FinFET as less of the interface and oxide traps were generated in the case of the former [29]. As channel doping increased, 10 M radiation appears to have significantly reduce V_T, however, this can only attributed to the increase in the absolute value of the initial amount. In fact, very silght difference was observed when calculating the percentage variation of the aforementioned amount. As presented in Table 4, the V_T variation percentage was found to be similar between the channel doping of 1×10^{16} cm^{-3} and 1×10^{18} cm^{-3} for both the FinFET and 5ch-NW. Thus, channel doping had little or no influence on the TID effect in the FinFET and 5ch-NW.

Table 4. V_T variation according to the channel doping.

	FinFET (ΔV_T)		5ch-NW (ΔV_T)	
Channel doping	1×10^{16} cm^{-3}	1×10^{18} cm^{-3}	1×10^{16} cm^{-3}	1×10^{18} cm^{-3}
Initial	329 mV	345 mV	402 mV	411 mV
10 Mrad	312 mV	329 mV	388 mV	398 mV
ΔV_T (%)	5.16%	4.63%	3.48%	3.16%

4. Conclusions

In this paper, we found that the 5ch-NW GAA devices exhibited less ionizing radiation sensitivity when compared to the FinFET device. Structurally, the 5ch-NW device had an oxide area of approximately 96.1 nm^2, which is larger than that of the FinFET. However, in our experiment, the TID effect of 5ch-NW was observed to be less than that of the FinFET. It was shown that the gate controllability factor is more crucial to the suppression of the TID effect than the oxide area. The GAA structure, which has larger gate controllability, confirmed that the TID effect problem can be effectively resolved. The GAA structure and high-k dielectric materials have to be introduced to improve gate controllability. Furthermore, the 5ch-NW was not found to be affected by V_{DD}. However, the FinFET was affected by V_{DD} when low radiation was applied. Therefore, devices with strong gate controllability were not affected by TID and channel doping had little or no influence on the TID effect.

Author Contributions: H.W. simulation and analysis of data and Methodology; I.H. correcting article and design figures; Y.J. writing review and editing; M.K. project administration and supervision and proofreading the manuscript and funding.

Funding: This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2018R1A6A1A03023788), the Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) (N000P00008500, The Competency Development Program for Industry Specialist), the National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT, and Future Planning (2017M1A7A1A01016265). This research was also supported by the MOTIE (Ministry of Trade, Industry & Energy (10085645) and KSRC (Korea Semiconductor Research Consortium) support program for the development of future semiconductor devices.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Leroux, P.; Van Koeckhoven, W.; Verbeeck, J.; Van Uffelen, M.; Esqué, S.; Ranz, R.; Damiani, C.; Hamilton, D. Design of a MGy radiation tolerant resolver-to-digital convertor IC for remotely operated maintenance in harsh environments. *Fusion Eng. Des.* **2014**, *89*, 2314–2319. [CrossRef]
2. Haddad, N.F.; Kelly, A.T.; Lawrence, R.K.; Li, B.; Rodgers, J.C.; Ross, J.F.; Warren, K.M.; Weller, R.A.; Mendenhall, M.H.; Reed, R.A. Incremental enhancement of SEU hardened 90 nm CMOS memory cell. *IEEE Trans. Nucl. Sci.* **2011**, *58*, 975–980. [CrossRef]
3. Clark, L.T.; Mohr, K.C.; Holbert, K.E.; Yao, X.; Knudsen, J.; Shah, H. Optimizing radiation hard by design SRAM cells. *IEEE Trans. Nucl. Sci.* **2007**, *54*, 2028–2036. [CrossRef]
4. Gatti, U.; Calligaro, C.; Pikhay, E.; Roizin, Y. Radiation-hardened techniques for CMOS flash ADC. In Proceedings of the IEEE International Conference on Electronics Circuits and Systems (ICECS), Marseille, France, 7–10 December 2014; pp. 1–4.
5. Verbeeck, J.; Cao, Y.; Van Uffelen, M.; Casellas, L.M.; Damiani, C.; Morales, E.R.; Santana, R.R.; Meek, R.; Hais, B.; Hamilton, D.; et al. Qualification method for a 1 MGy-tolerant front-end chip designed in 65 nm CMOS for the read-out of remotely operated sensors and actuators during maintenance in ITER. *Fusion Eng. Des.* **2015**, *96–97*, 1002–1005. [CrossRef]
6. Verbeeck, J.; Van Uffelen, M.; Steyaert, M.; Leroux, P. 17 bit 4.35 mW 1 kHz delta sigma ADC and 256-to-1 multiplexer for remote handling instrumentation equipment. *Fusion Eng. Des.* **2013**, *88*, 1942–1946. [CrossRef]
7. Cao, Y.; Cock, W.D.; Steyaert, M.; Leroux, P. A 4.5 MGy TID-tolerant CMOS bandgap reference circuit using a dynamic base leakage compensation technique. *IEEE Trans. Nucl. Sci.* **2013**, *60*, 2819–2824. [CrossRef]
8. Virmontois, C.; Goiffon, V.; Magnan, P.; Girard, S.; Inguimbert, C.; Petit, S.; Rolland, G.; Saint-Pé, O. Displacement damage effects due to neutron and proton irradiations on CMOS image sensors manufactured in deep submicron technology. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 3101–3108. [CrossRef]
9. Barnaby, H.J. Total-ionizing-dose effects in modern CMOS technologies. *IEEE Trans. Nucl. Sci.* **2006**, *53*, 3103–3121. [CrossRef]
10. Martin, H.; Martin-Holgado, P.; Morilla, Y.; Entrena, L.; San-Millan, E. Total ionizing dose effects on a delay-based physical unclonable function implemented in FPGAs. *Electronics* **2018**, *7*, 163. [CrossRef]

11. Seo, D.; Trang, L.D.; Han, J.W.; Kim, J.; Lee, S.; Chang, I.J. Total Ionizing Dose Effect on Ring Oscillator Frequency in 28nm FD-SOI Technology. *IEEE Electron. Device Lett.* **2018**, *39*, 1728–1731. [CrossRef]
12. Zebrev, G. Static and Dynamic Oxide-Trapped-Charge-Induced Variability in Nanoscale CMOS Circuits. *IEEE Trans. Electron Devices* **2019**, *66*, 2483–2488. [CrossRef]
13. Zhai, Y.; Mathew, L.; Rao, R.; Palard, M.; Chopra, J.S.; Ekerdt, G.; Register, L.F.; Banerjee, S.K. High-Performance Vertical Gate-All-Around Silicon Nanowire FET with High-k/Metal Gate. *IEEE Trans. Electron Devices* **2014**, *61*, 3896–3900. [CrossRef]
14. Song, J.Y.; Choi, W.Y.; Park, J.H.; Lee, J.D.; Park, B.G. Design optimization of gate-all-around (GAA) MOSFETs. *IEEE Trans. Nanotechnol.* **2006**, *5*, 186–191. [CrossRef]
15. Bangsaruntip, S.; Cohen, G.M.; Majumdar, A.; Sleight, J.W. Universality of Short-Channel Effects in Undoped-Body Silicon Nanowire MOSFETs. *IEEE Electron Device Lett.* **2010**, *31*, 903–905. [CrossRef]
16. Ko, K.; Kang, M.; Jeon, J.; Shin, H. Compact Model Strategy of Metal-Gate Work-Function Variation for Ultrascaled FinFET and Vertical GAA FETs. *IEEE Trans. Electron Devices* **2019**, *66*, 1613–1615. [CrossRef]
17. *The International Technology Roadmap for Semiconductors (ITRS)*; Semiconductor Industry Association: Washington, DC, USA, 2015.
18. Victory Device User's Manual, Silvaco Version. Available online: https://www.silvaco.com/products/tcad/device_simulation/victory_device/victory_device.html (accessed on 26 January 2015).
19. Klaassen, D.B.M. Physical modeling bipolar device simulation. In *Simulation of Semiconductor Devices and Processes*; Fichtner, W., Aemmer, D., Eds.; Springer Science and Business Media: New York, NY, USA, 1991; Volume 4, pp. 23–43.
20. Klaassen, D.B.M. A unified mobility model for device simulation—I. Model equations and concentration dependence. *Solid State Electron.* **1992**, *35*, 953–959. [CrossRef]
21. Klaassen, D.B.M. A unified mobility model for device simulation—II. Temperature dependence of carrier mobility and lifetime. *Solid State Electron.* **1992**, *35*, 961–967. [CrossRef]
22. Klaassen, D.B.M.; Slotboom, J.W.; De Graaff, H.C. Unified apparent bandgap narrowing in n- and p- type silicon. *Solid State Electron.* **1992**, *35*, 125–129. [CrossRef]
23. Hurkx, G.A.M.; Klaassen, D.B.M.; Knuvers, M.P.G. A new recombination model for device simulation including tunneling. *IEEE Trans. Electron Devices* **1992**, *39*, 331–338. [CrossRef]
24. Kimpton, D.; Kerr, J. A Simple Trap-Detrap Model for Accurate Prediction of Radiation Induced Threshold Voltage Shifts in Radiation Tolerant Oxides for All Static or Time Variant Oxide Fields. *Solid State Electron.* **1994**, *37*, 153–158. [CrossRef]
25. Cho, J.W. *Sensor and Communication Network Technology for Harsh Environments in the Nuclear Power Plant*; KAERI/AR-795/2008; IAEA International Nuclear Information System: Vienna, Austria, 2008; Volume 39, pp. 1–133.
26. Oldham, T.R.; McLean, F.B. Total ionizing dose effects in MOS oxides and devices. *IEEE Trans. Nucl. Sci.* **2003**, *50*, 483–499. [CrossRef]
27. Adell, P. *Hydrogen Contamination and Its Correlation with Enhanced Low-Dose-Rate Sensitivity Nasa Electronic Parts and Packaging (Nepp) Program Office of Safety and Mission Assurance*; National Aeronautics and Space Administration: Washington, DC, USA, 2012; pp. 1–62.
28. Nam, J.; Kang, C.Y.; Kim, K.P.; Yeo, H.; Lee, B.J.; Seo, S.; Yang, J.W. Influence of Ionizing Radiation on Short-Channel Effects in Low-Doped Multi-Gate MOSFETs. *IEEE Trans. Nucl. Sci.* **2012**, *59*, 3021–3026.
29. Kilchytska, V.; Alvarado, J.; Collaert, N.; Rooyakers, R.; Militaru, O.; Berger, G.; Flandre, D. Total-dose effects caused by high-energy neutrons and γ -rays in multiple-gate FETs. *IEEE Trans. Nucl. Sci.* **2010**, *57*, 7–13. [CrossRef]