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A Virtual Impedance Control Strategy for Improving the Stability and Dynamic Performance of VSC–HVDC Operation in Bidirectional Power Flow Mode

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Abstract: It is a common practice that one converter controls DC voltage and the other controls power in two-terminal voltage source converter (VSC)–based high voltage DC (HVDC) systems for AC gird interconnection. The maximum transmission power from a DC-voltage-controlled converter to a power-controlled converter is less than that of the opposite transmission direction. In order to increase the transmission power from a DC-voltage-controlled converter to a power-controlled converter, an improved virtual impedance control strategy is proposed in this paper. Based on the proposed control strategy, the DC impedance model of the VSC–HVDC system is built, including the output impedance of two converters and DC cable impedance. The stability of the system with an improved virtual impedance control is analyzed in Nyquist stability criterion. The proposed control strategy can improve the transmission capacity of the system by changing the DC output impedance of the DC voltage-controlled converter. The effectiveness of the proposed control strategy is verified by simulation. The simulation results show that the proposed control strategy has better dynamic performance than traditional control strategies.

Keywords: VSC–HVDC; DC-side oscillation; virtual impedance; impedance-based Nyquist stability criterion

1. Introduction

With the development of power electronic devices, VSC–HVDC systems have been widely applied to AC grid interconnection because of their independent decoupling control of active and reactive power [1–3]. Recently, a large number of studies on modeling, control, and stability analysis of VSC–HVDC system have been published [4–10]. Previous studies have shown that the interaction between converters or between the converter and the grid influences the stability of a system. DC- side oscillation is a problem in VSC–HVDC and has been reported in a real project [11]. When DC side oscillation occurs, a DC system will not work and will impact on the power system. Therefore, the DC-side stability of VSC–HVDC should be evaluated before connecting it to the main grid.

In VSC–HVDC systems applied to AC grid interconnection, active power often needs bidirectional transmission [12]. However, studies show that the maximum transmission power of the DC-voltage-controlled converter to power-controlled converter is less than that in the opposite power flow direction [13]. An Impedance-based approach can be adopted to analyze the influence of VSC–HVDC systems with different directions of transmission power on stability [13].

The impedance stability criterion was proposed in [14] and used in grid-connected inverters [15]. It was applied as a stability criterion in a VSC–HVDC system [12,16–19]. The impedance model of two-terminal VSC–HVDCs was built in [12], and the cause of DC current resonance was analyzed with Nyquist stability criteria. Different subsystems were selected to analyze the DC-side stability of the

VSC–HVDC system with a transfer function method in [16]. The influence of overhead transmission lines, DC cables, and the DC-side filter on system stability was investigated in [17]. The different performances of the lumped parameter and distributed parameter circuit models in stability analysis were discussed in [18]. It was found that the distributed parameter circuit model is more accurate in stability analysis.

In the condition of VSC–HVDC for AC Grid interconnection, the maximum transmission capacities of the different power flow directions are different. Thus, a control strategy is required to improve the transmission capacity from the DC-voltage-controlled converter to the power-controlled converter to improve resource utilization efficiency. To increase the maximum transmission power, the DC side oscillation must be suppressed. The suppression methods of DC side oscillation can be classified into passive methods [20,21] and active methods [22–29]. Passive methods suppress resonance by introducing a passive damper branch into the circuit to remodel the impedance of the source converter or load converter in a cascaded system. Active methods suppress resonance by introducing voltage and current feedback control in a controller to improve the impedance of the source converter or load converter. Virtual impedance is widely used in control systems as an active damping control method [24–29]. It can be introduced to suppress DC-side oscillation [24,25], to limit output current for voltage controlled inverters during overloads or faults [26,27], to improve the stability of a grid-connected inverter by change its input admittance [28], and to enhance the small-signal stability of a modular multilevel converter (MMC) based DC grid [29].

Virtual impedance in the DC voltage control loop can suppress the DC-side oscillation of a VSC–HVDC transmission system and improve its stability margin and the transmission capacity of the system [24,25]. However, virtual impedance control leads to steady-state errors in the DC output voltage of DC-voltage-controlled converters, due to different operating points [25]. An improved virtual impedance control strategy is proposed in this paper. To design an appropriate control strategy, a stability analysis is required. Thus, a DC impedance-based model of VSC–HVDC is built, and the stability of the system is analyzed based on impedance stability criteria.

The rest of the paper is organized as follows: Section 2 describes the system's structure and the simulation of a VSC–HVDC system, as well as the design of an improved virtual impedance control. Section 3 presents the impedance model of an HVDC system. Section 4 conducts a stability analysis on the basis of impedance stability criteria, and Section 5 shows the simulation verification. Section 6 summarizes the proposed method.

2. Improved Virtual Impedance Control Principle

This paper mainly studies a two-level topology structure. The analysis in this paper can be also applicable to an MMC system if the dc bus voltage ripples are insignificant [12]. A two-level VSC–HVDC system used in AC grid interconnection is depicted in Figure 1. Figure 1 shows a DC voltage-controlled converter and a power-controlled converter on the left and right sides, respectively. The two converters have an identical structure. $R_{n1} + jX_{n1}$ and $R_{n2} + jX_{n2}$ are the equivalent impedance of the AC system, $R_{c1} + j\omega_1 L_1$ and $R_{c2} + j\omega_2 L_{c2}$ are the impedance of the filter reactor, C_{f1} and C_{f2} are the filter capacitors, $\dot{m}_1$ and $\dot{m}_2$ are the modulations of the converter station, $\dot{u}_{s1}$ and $\dot{u}_{s2}$ are the AC voltage at point of common coupling, $\dot{u}_{g1}$ and $\dot{u}_{g2}$ are the AC voltage of the AC system, $\dot{i}_{s1}$ and $\dot{i}_{s2}$ are the AC current flowing through the filter reactor, and $\dot{i}_{g1}$ and $\dot{i}_{g2}$ are the AC current flowing through the AC system. The DC cable is a π type, with an equivalent resistance of R_d, an equivalent inductance of L_d, and an equivalent capacitance of C_d.

The modeling and control of the VSC–HVDC system are presented in a synchronous rotating frame (SRF). The transformation of the three-phase quantity from stationary reference frame to the SRF is based on the amplitude-invariant Park transformation, with the d-axis aligned with the voltage vector u_s and q-axis leading the d-axis by 90°. The grid voltage defines the system's dq reference. A phase-locked loop (PLL) defines the controller dq reference. The system reference is aligned with the

PLL reference in a steady state. When a small disturbance occurs, the system reference is no longer aligned with the PLL reference. The relationship between the system reference and the PLL reference under a small disturbance is shown in Figure 2.

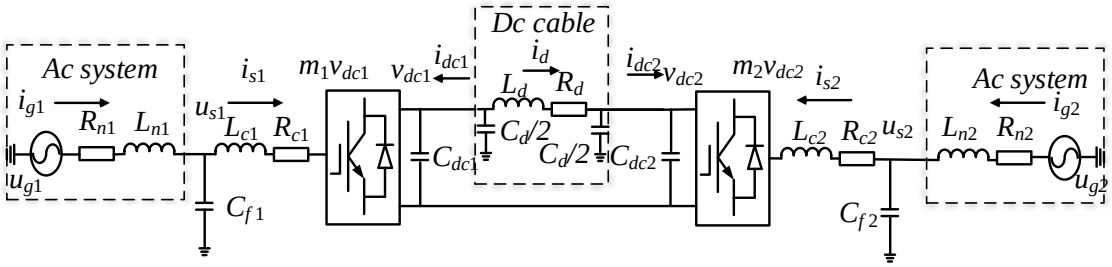


Figure 1. VSC–HVDC used in AC grid interconnection.

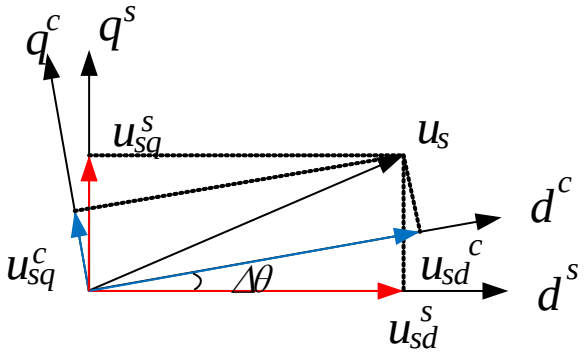


Figure 2. System and phase-locked loop (PLL) references.

Here, subscript *dq* represent the components of the physical quantity in the SRF. Subscript 0 represents the value of the physical quantity at the static working point, subscript *ref* represents the given value of physical quantity, and subscript Δ represents the small disturbance components of the physical quantity. Superscript *c* represents the components of physical quantity in the PLL reference, and superscript *s* represents the components in the system reference.

The simulation model of VSC–HVDC in Figure 1 is built on a MATLAB/Simulink. The system parameters are shown in the following table. The vector current control [13] is adopted in the two converters, and the control is shown in Figure 3. For symmetry of the VSC–HVDC system, subscripts 1,2 of the system parameters in Table 1 and the control diagram in Figure 3 are omitted. In the model, controller parameters are per unit. The base angular grid frequency is 50 Hz, the base grid voltage is 110 kV, the base system capacity is 500 MW, and the base DC voltage is 250 kV. According to the parameters in Table 1, the system's closed-loop bandwidth with a DC voltage controller is 65 Hz, and the system's open-loop phase margin is 58 degrees. The system's closed-loop bandwidth with an active power controller is 8 Hz, and the system's open-loop phase margin is 150 degrees. The system's closed-loop bandwidth with the current controller is 180 Hz, and the system's open-loop phase margin is 85 degrees.

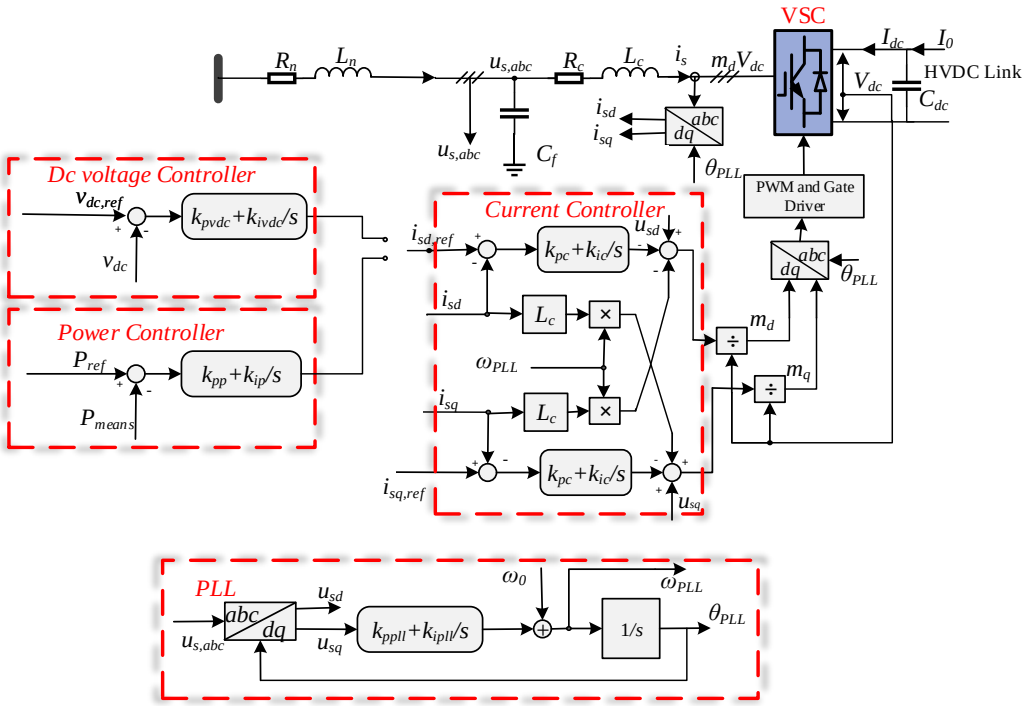


Figure 3. Control structure of the converters.

Table 1. Simulation parameters.

Parameters		Values
Converter and AC system	System capacity Sn/MW	500
	Line voltage of grid u_g/kV	110
	DC voltage V_{dc}/kV	250
	Grid internal resistance R_n/Ω	0.2
	Grid frequency ω_0/Hz	50
	Grid internal inductance L_n/H	1×10^{-3}
	Filter reactor inductance L_c/H	4.5×10^{-2}
	Filter reactor resistance R_c/Ω	0.2
	DC side capacitance $C_{dc}/\mu f$	300
DC cable	DC cable resistance R_d/Ω/km	1.39×10^{-2}
	DC cable inductance L_d/H/km	1.59×10^{-4}
	DC cable capacitance C_d/F/km	2.31×10^{-7}
Controller	DC voltage outer loop k_{pvdc}/k_{ivdc}	15/100
	Current inner loop k_{pc}/k_{ic}	0.5/0.1
	Active power outer loop k_{pp}/k_{ip}	1/10
	Phase locked loop k_{pPLL}/k_{iPLL}	10/100

The power flow direction from the power-controlled converter to the DC voltage-controlled converter is set to positive. Figure 4 shows the resulting time-domain responses of the DC voltage of the VSC–HVDC system. At 2 s, the active power instruction value steps from 500 MW to −500 MW, and the length of the DC cable is 50 km. It can be observed that the DC voltage starts to oscillate, the active power starts to fluctuate, and the system loses stability.

The power-controlled converter exhibits a constant power load (CPL) when the active power is transmitted from the DC-voltage controlled converter to the power-controlled converter. The incremental input resistance characteristic caused by CPL affects the stability of the VSC–HVDC system [24].

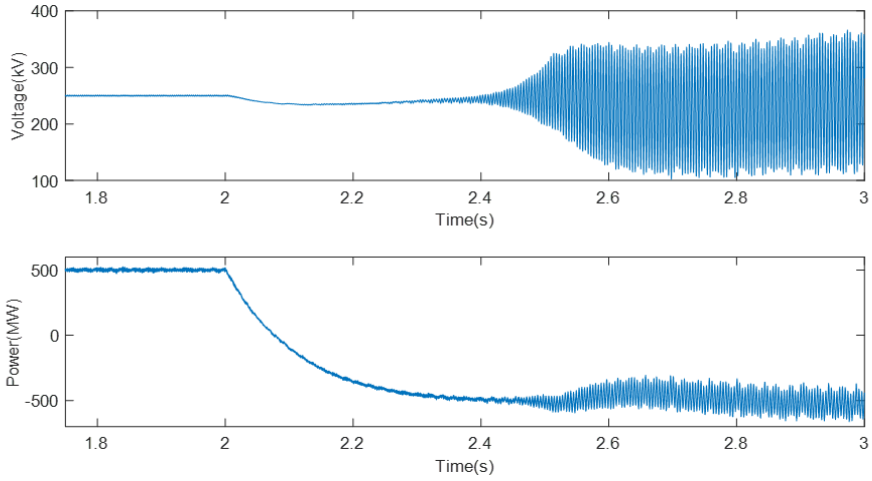


Figure 4. DC-link voltage and the active power of the VSC–HVDC system.

A virtual impedance control strategy is introduced in the DC-voltage-controlled converter to mitigate the DC-side oscillation caused by the negative incremental input resistance characteristic of the power-controlled converter. The expression of the virtual impedance control is

$$v_{dcref} = v_{dcn} - (R_{eq} + sL_{eq})i_{dc} \tag{1}$$

where v_{dcref} is the DC voltage reference value, v_{dcn} is the no-load DC voltage of the converter, and R_{eq} and L_{eq} are the set values for the virtual impedance. Due to the addition of current feedback, under loaded conditions, there will be a fixed steady-state error between the DC voltage reference value and the measured value, which almost equals $R_{eq} * i_{dc}$. Thus, the steady-state error increases with an increase in the transmission power (in both power flow directions).

In order to eliminate the steady-state error caused by virtual impedance, this paper modifies the voltage control loop, as shown by the blue dotted line frame in Figure 5.

$$i_{dcn} = \frac{k_i}{s}(v_{dcn} - v_{dc}) \tag{2}$$

$$v_{dcref} = v_{dcn} - (R_{eq} + sL_{eq})(i_{dc} - i_{dcn}) \tag{3}$$

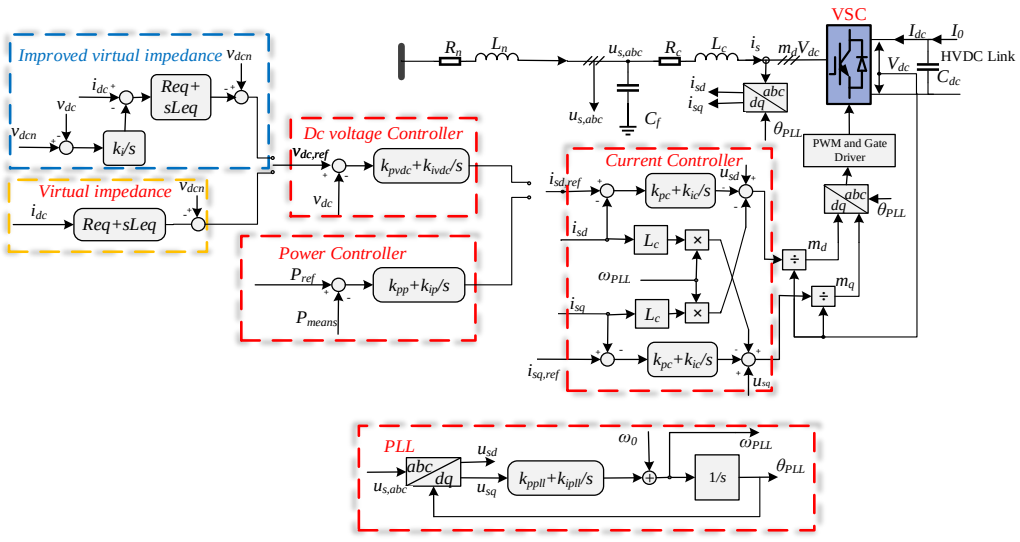


Figure 5. Proposed control structure of the converters.

3. Impedance Model of Converters with Improved Virtual Impedance Control Strategy

3.1. DC-Side Impedance Modeling of DC-Voltage-Controlled Converter

The linearized dynamic equations of the DC voltage-controlled converter are expressed as

$$\begin{bmatrix} m_{d0} \\ m_{q0} \end{bmatrix}\Delta v_{dc} + v_{dc0}\begin{bmatrix} \Delta m_d^s \\ \Delta m_q^s \end{bmatrix} + Z_0(s)\begin{bmatrix} \Delta i_{sd}^s \\ \Delta i_{sq}^s \end{bmatrix} = \begin{bmatrix} \Delta u_{sd}^s \\ \Delta u_{sq}^s \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} \Delta u_{sd}^s \\ \Delta u_{sq}^s \end{bmatrix} = -Z_g(s)\begin{bmatrix} \Delta i_{gd}^s \\ \Delta i_{gq}^s \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} \Delta i_{gd}^s \\ \Delta i_{gq}^s \end{bmatrix} = \begin{bmatrix} \Delta i_{sd}^s \\ \Delta i_{sq}^s \end{bmatrix} + Y_{cf}(s)\begin{bmatrix} \Delta u_{sd}^s \\ \Delta u_{sq}^s \end{bmatrix} \tag{6}$$

where

$$Z_0 = \begin{bmatrix} R_c + sL_c & -\omega_0 L_c \\ \omega_0 L_c & R_c + sL_c \end{bmatrix} \tag{7}$$

$$Z_g = \begin{bmatrix} R_n + sL_n & -\omega_0 L_n \\ \omega_0 L_n & R_n + sL_n \end{bmatrix} \tag{8}$$

$$Y_{cf}(s) = \begin{bmatrix} sC_f & -\omega_0 C_f \\ \omega_0 C_f & sC_f \end{bmatrix} \tag{9}$$

Its controller and modulator linearized equations are expressed as

$$\begin{bmatrix} \Delta i_{sd,ref} \\ \Delta i_{sq,ref} \end{bmatrix} = \begin{bmatrix} k_{pvdc} + \frac{k_{ivdc}}{s} \\ 0 \end{bmatrix}(\Delta v_{dcref} - \Delta v_{dc}) \tag{10}$$

$$v_{dc0}\begin{bmatrix} \Delta m_d^c \\ \Delta m_q^c \end{bmatrix} = -G_{pwm}G_{cc}\begin{bmatrix} \Delta i_{sd,ref} \\ \Delta i_{sq,ref} \end{bmatrix} + G_{pwm}\begin{bmatrix} \Delta u_{sd}^c \\ \Delta u_{sq}^c \end{bmatrix} + G_{pwm}(G_{cc} + Z_{del})\begin{bmatrix} \Delta i_{sd}^c \\ \Delta i_{sq}^c \end{bmatrix} \tag{11}$$

where k_{pvdc} and k_{ivdc} are the proportional and integral gains of the DC voltage controller, respectively, G_{pwm} is the PWM delay, and G_{cc} is the current compensator transfer function, where k_{pc} and k_{ic} are the proportional and integral gains of the current compensator, respectively.

$$G_{pwm} = \begin{bmatrix} H_{pwm} & 0 \\ 0 & H_{pwm} \end{bmatrix} \tag{12}$$

$$H_{pwm} = e^{-sT_s}\frac{1 - e^{-sT_s}}{sT_s} \tag{13}$$

$$G_{cc} = \begin{bmatrix} k_{pc} + \frac{k_{ic}}{s} & 0 \\ 0 & k_{pc} + \frac{k_{ic}}{s} \end{bmatrix} \tag{14}$$

$$Z_{del} = \begin{bmatrix} 0 & \omega_{pLL}L_c \\ -\omega_{pLL}L_c & 0 \end{bmatrix} \tag{15}$$

The variables of the controller are based on the output of the PLL reference, whereas the variables of the circuit are based on the system reference. The relationship of physical quantity between the PLL and the system references is expressed as [13]

$$\begin{bmatrix} \Delta i_{sd}^c \\ \Delta i_{sq}^c \end{bmatrix} = \begin{bmatrix} \Delta i_{sd}^s \\ \Delta i_{sq}^s \end{bmatrix} + \overbrace{\begin{bmatrix} 0 & G_{PLL}(s)i_{sq0} \\ 0 & -G_{PLL}(s)i_{sd0} \end{bmatrix}}^{G_{PLL}^i}\begin{bmatrix} \Delta u_{sd}^s \\ \Delta u_{sq}^s \end{bmatrix} \tag{16}$$

$$\begin{bmatrix} \Delta u^{c}_{sd} \\ \Delta u^{c}_{sq} \end{bmatrix} = \overbrace{\begin{bmatrix} 1 & G_{PLL}(s)u_{sq0} \\ 0 & 1 - G_{PLL}(s)u_{sd0} \end{bmatrix}}^{G^{v}_{PLL}} \begin{bmatrix} \Delta u^{s}_{sd} \\ \Delta u^{s}_{sq} \end{bmatrix} \tag{17}$$

$$\begin{bmatrix} \Delta m^{c}_{d} \\ \Delta m^{c}_{q} \end{bmatrix} = \begin{bmatrix} \Delta m^{s}_{d} \\ \Delta m^{s}_{q} \end{bmatrix} - \overbrace{\begin{bmatrix} 0 & -G_{PLL}(s)m_{q0} \\ 0 & G_{PLL}(s)m_{d0} \end{bmatrix}}^{G^{d}_{PLL}} \begin{bmatrix} \Delta u^{s}_{sd} \\ \Delta u^{s}_{sq} \end{bmatrix} \tag{18}$$

where

$$tf_{PLL} = k_{pPLL} + \frac{k_{iPLL}}{s} \tag{19}$$

$$G_{PLL} = \frac{tf_{pLL}}{s + u_{sd0} f_{PLL}} \tag{20}$$

Here, tf_{PLL} is the PLL transfer function and k_{pPLL} and k_{iPLL} are the proportional and integral gains of the PLL compensator, respectively.

The linearized equation of the power balance between the AC and DC sides of the converter is expressed as

$$\Delta i_{dc} = 1.5\left(\begin{bmatrix} m_{d0} & m_{q10} \end{bmatrix} \begin{bmatrix} \Delta i^{s}_{sd} \\ \Delta i^{s}_{sq} \end{bmatrix} + \begin{bmatrix} i_{sd0} & i_{sq0} \end{bmatrix} \begin{bmatrix} \Delta m^{s}_{d} \\ \Delta m^{s}_{q} \end{bmatrix}\right) \tag{21}$$

The small signal expression of the improved virtual impedance compensator is expressed as

$$\Delta i_{dcn} = -\frac{k_i}{s} \Delta v_{dc} \tag{22}$$

$$\Delta v_{dcref} = -(R_{eq} + sL_{eq})\left(\frac{k_i}{s} \Delta v_{dc} + \Delta i_{dc}\right). \tag{23}$$

Inserting (22) and (23) into (10), the relation between the AC current reference values $\Delta i_{sd,ref}$, $\Delta i_{sq,ref}$, DC voltage Δv_{dc}, and DC current Δi_{dc} is expressed as

$$\begin{bmatrix} \Delta i_{sd,ref} \\ \Delta i_{sq,ref} \end{bmatrix} = \begin{bmatrix} H_{vdc} & H_{idc} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} \tag{24}$$

where

$$H_{vdc} = -\left(k_{pvdc} + \frac{k_{ivdc}}{s}\right)\left(\frac{k_i R_{eq}}{s} + k_i L_{eq} + 1\right) \tag{25}$$

$$H_{idc} = -\left(k_{pvdc} + \frac{k_{ivdc}}{s}\right)(R_{eq} + sL_{eq}) \tag{26}$$

Formula (5) can be written as

$$\begin{bmatrix} \Delta i^{s}_{gd} \\ \Delta i^{s}_{gq} \end{bmatrix} = -Y_g(s) \begin{bmatrix} \Delta u^{s}_{sd} \\ \Delta u^{s}_{sq} \end{bmatrix}. \tag{27}$$

Inserting (27) into (6), the relation between the AC voltage and AC current can be given as

$$\begin{bmatrix} \Delta u^{s}_{sd} \\ \Delta u^{s}_{sq} \end{bmatrix} = \overbrace{\left(Y_{cf}(s) - Y_g(s)\right)^{-1}}^{Z_s} \begin{bmatrix} \Delta i^{s}_{sd} \\ \Delta i^{s}_{sq} \end{bmatrix}. \tag{28}$$

Considering PLL, inserting (16)–(18) and (28) into (11), the modulation index can be written as

$$\begin{bmatrix} \Delta m_d^s \\ \Delta m_q^s \end{bmatrix} v_{dc0} = -G_{pwm}G_{cc}\begin{bmatrix} H_{vdc} & H_{idc} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} + G_z^{vdc}(s)\begin{bmatrix} \Delta i_{sd}^s \\ \Delta i_{sq}^s \end{bmatrix} \tag{29}$$

where

$$G_z^{vdc}(s) = G_{pwm}(G_{cc} + Z_{del}) + Z_s(s)G_c^i. \tag{30}$$

$$G_c^i = (G_{pwm}G_{PLL}^v + G_{pwm}(G_{cc} + Z_{del})G_{PLL}^i + v_{dc0}G_{PLL}^d) \tag{31}$$

The relation between the DC voltage, DC current, and AC currents can be obtained from (4) by inserting (28) and (29):

$$Y_{AC}^{Vdc}(s)\begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} = \begin{bmatrix} \Delta i_{sd}^s \\ \Delta i_{sq}^s \end{bmatrix} \tag{32}$$

where

$$Y_{AC}^{Vdc}(s) = (Z_s(s) - Z_0(s) - G_z^{vdc}(s))^{-1}(\begin{bmatrix} m_{d0} & 0 \\ m_{q0} & 0 \end{bmatrix} + G_{pwm}G_{cc1}\begin{bmatrix} H_{vdc} & H_{idc} \\ 0 & 0 \end{bmatrix}) \tag{33}$$

and Y_{AC}^{Vdc} can be expressed as a 2*2 order matrix:

$$Y_{AC}^{Vdc} = \begin{bmatrix} Y_1 & Y_2 \\ Y_3 & Y_4 \end{bmatrix} \tag{34}$$

Inserting (32) into (4), yields

$$\begin{bmatrix} \Delta m_d^s \\ \Delta m_q^s \end{bmatrix} = \frac{1}{v_{dc0}}((Z_s(s) - Z_0(s))Y_{AC}^{Vdc}(s) - \begin{bmatrix} m_{d0} & 0 \\ m_{q0} & 0 \end{bmatrix})\begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix}. \tag{35}$$

In the power balance relation, by inserting (34) and (35) into (21), (21) can be replaced by

$$\begin{aligned} \Delta i_{dc} = 1.5\begin{bmatrix} m_{d0} & m_{q0} \end{bmatrix}\begin{bmatrix} \Delta i_{sd}^s \\ \Delta i_{sq}^s \end{bmatrix} + 1.5\begin{bmatrix} i_{sd0} & i_{sq0} \end{bmatrix}\begin{bmatrix} \Delta m_d^s \\ \Delta m_q^s \end{bmatrix} = 1.5\begin{bmatrix} m_{d0} & m_{q0} \end{bmatrix}Y_{AC}^{Vdc}(s)\begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} + \\ 1.5\begin{bmatrix} i_{sd0} & i_{sq0} \end{bmatrix}\frac{1}{v_{dc0}}((Z_s(s) - Z_0(s))Y_{AC}^{Vdc}(s) - \begin{bmatrix} m_{d10} & 0 \\ m_{q10} & 0 \end{bmatrix})\begin{bmatrix} \Delta v_{dc} \\ \Delta i_{dc} \end{bmatrix} = M_1\Delta v_{dc} + M_2\Delta i_{dc} \end{aligned} \tag{36}$$

where

$$\begin{aligned} M_1 = 1.5m_{d0}Y_1 + 1.5m_{q0}Y_3 + \frac{1.5}{v_{dc0}}i_{sd0}(RY_1 + sLY_1 - \omega_0 LY_3 - m_{d0}) + \\ i_{sq0}(RY_3 + sLY_3 - \omega_0 LY_1 - m_{q0}) \end{aligned} \tag{37}$$

$$M_2 = 1.5m_{q0}Y_2 + \frac{1.5}{v_{dc0}}i_{sd0}(RY_2 + sLY_2 - i_{sq0}\omega_0 LY_4) + i_{sq0}(RY_2 + sLY_2 - \omega_0 LY_4) \tag{38}$$

$$R = R_n - R_c \tag{39}$$

$$L = L_n - L_c \tag{40}$$

The DC impedance of the converters can be calculated by solving (36) and can be expressed as

$$Z_{dc\mathrm{r}} = \frac{1 - M_2}{M_1}. \tag{41}$$

Consider the DC-side capacitor,

$$Z_{dc1} = \frac{Z_{dcr}}{1 + sC_{dc}Z_{dcr}}. \tag{42}$$

3.2. DC Side Impedance Modeling of the Power-Controlled Converter

The linearized dynamic equations of the power-controlled converter are the same as those of the DC-voltage-controlled converter, which are expressed as (4)–(6), and its outer loop controller linearized equation is expressed as

$$\begin{bmatrix} \Delta i_{sd,ref} \\ \Delta i_{sq,ref} \end{bmatrix} = -H_p(\overbrace{\begin{bmatrix} 1.5u_{sd0} & 1.5u_{sq0} \\ 0 & 0 \end{bmatrix}}^{G_{vp}}\begin{bmatrix} \Delta i^c_{sd} \\ \Delta i^c_{sq} \end{bmatrix}+\overbrace{\begin{bmatrix} 1.5i_{sd0} & 1.5i_{sq0} \\ 0 & 0 \end{bmatrix}}^{G_{ip}}\begin{bmatrix} \Delta u^c_{sd} \\ \Delta u^c_{sq} \end{bmatrix}) \tag{43}$$

where $H_p = k_{pp} + k_{ip}/s$ is the active power compensator and k_{pp} and k_{ip} are the proportional and integral gains of the compensator. Its current compensator and modulator is same as (11). Inserting (16)–(18) into (42) gives

$$\begin{bmatrix} \Delta i_{sd,ref} \\ \Delta i_{sq,ref} \end{bmatrix} = -H_pG_{vp}\begin{bmatrix} \Delta i^s_{sd} \\ \Delta i^s_{sq} \end{bmatrix}-(H_pG_{vp}G^i_{PLL}+H_pG_{ip}G^i_{PLL})\begin{bmatrix} \Delta u^s_{sd} \\ \Delta u^s_{sq} \end{bmatrix}. \tag{44}$$

Inserting (16)–(18) and (28) into (11), the relation between the modulation index and AC current can be expressed as

$$\begin{bmatrix} \Delta m^s_d \\ \Delta m^s_q \end{bmatrix}v_{dc0} = (G_{pwm}G_{cc}H_pG_{vp}+G_{pwm}(G_{cc}+Z_{del}))\begin{bmatrix} \Delta i^s_{sd} \\ \Delta i^s_{sq} \end{bmatrix}+ (G_{pwm}G_{cc}H_p(G_{vp}G^i_{PLL}+G_{ip}G^v_{PLL})+G^i_C)\begin{bmatrix} \Delta u^s_{sd} \\ \Delta u^s_{sq} \end{bmatrix} \tag{45}$$

where

$$G^i_C = G^d_{PLL}+G_{pwm}G^v_{PLL}+G_{pwm}(G_{cc}+Z_{del})G^i_{PLL}. \tag{46}$$

Equation (45) can be rewritten as

$$\begin{bmatrix} \Delta m^s_d \\ \Delta m^s_q \end{bmatrix}v_{dc0} = G^P_Z\begin{bmatrix} \Delta i^s_{sd} \\ \Delta i^s_{sq} \end{bmatrix}. \tag{47}$$

Inserting (47) and (28) into (4) yields

$$\overbrace{(Z_s(s)-Z_0(s)-G^P_Z(s))^{-1}\begin{bmatrix} m_{d0} \\ m_{q0} \end{bmatrix}}^{Y^P_{AC}}\Delta v_{dc} = \begin{bmatrix} \Delta i^s_{sd} \\ \Delta i^s_{sq} \end{bmatrix}. \tag{48}$$

The DC-side impedance of the converter can be obtained by inserting (47) and (48) into (21):

$$Z_{dcA} = \frac{1}{1.5(\begin{bmatrix} m_{d0} & m_{q0} \end{bmatrix}+\begin{bmatrix} i_{sd0} & i_{sq0} \end{bmatrix}G^P_Z)Y^P_{AC}}. \tag{49}$$

Consider the DC-side capacitor,

$$Z_{dcB} = \frac{Z_{dcA}}{1+sC_{dc}Z_{dcA}} \tag{50}$$

Adding the DC cable impedance to the DC-side impedance of the power-controlled converter yields

$$Z_{dc2}(s) = (Z_{dcB}(s)\left\|\frac{2}{sC_d}+sL_d+R_d\right)\left\|\frac{2}{sC_d}\right. . \tag{51}$$

3.3. Verifying Impedance Modeling Through Perturbation Signal Testing

Perturbation signal testing is used to verify the accuracy of the proposed small-signal model. An AC current source should be placed parallel to the DC side of the system as an input signal, as Figure 6a shows. It is necessary to inject AC current at different frequencies to measure the DC side impedance at different frequencies. At each injection frequency, a simulation experiment is conducted. The DC voltage and DC current data of each experiment are analyzed by fast Fourier transformation. The components under the disturbance frequency are taken out, and the ratio of DC voltage and DC current is calculated as the calculated impedance [13]. Figure 6b,c shows the DC-side impedance verification of the DC system rectifier and inverter sides, respectively. The solid line in Figure 6b represents the analytical impedance of the rectifier converter as in (42), and the points represent the simulation results. Figure 6b represents the analytical impedance of the inverter station and the DC cable as (51), and the points represent the simulation results.

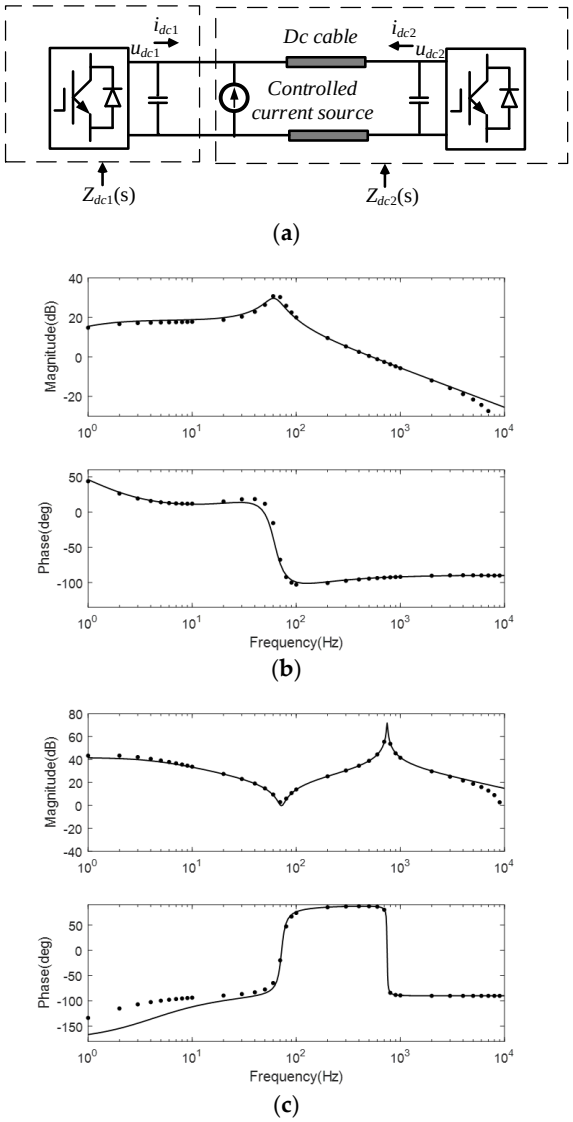


Figure 6. Frequency response of the impedance and verification. The solid line represents the model prediction, and the black points denote the simulation. (**a**) Disturbance signal testing. (**b**) Impedance of the DC voltage-controlled converter (**c**). Impedance of the power-controlled converter.

4. Stability Analysis of VSC–HVDC with Improved Virtual Impedance Control Strategy

According to the results of small signal modeling, the DC side of the voltage-controlled converter is modeled by a DC voltage source (V_s), in series with an output impedance (Z_s), which equals to Z_{dc1}. The DC side of the power-controlled converter and DC cable is modeled by a DC current source shunted with an input impedance (Z_l), which equals to Z_{dc2}. Figure 7 shows the equivalent impedance model of the system.

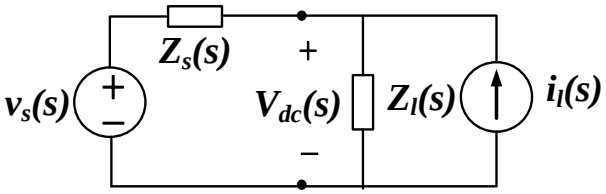


Figure 7. Equivalent model of the VSC–HVDC system.

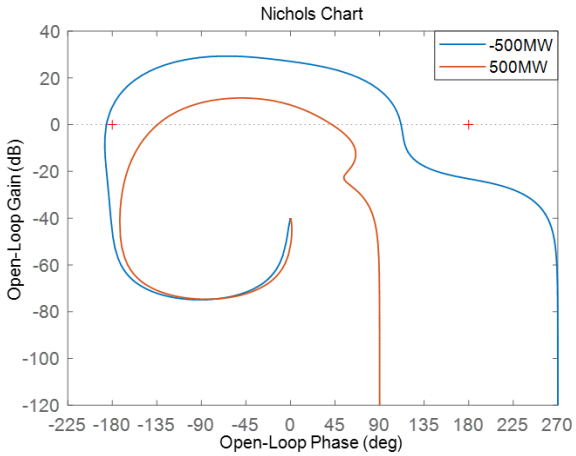
According to Kirchhoff's law, the output voltage of the DC side V_{dc} (s) can be expressed by Formula (52). The stability of the DC system depends on the ratio of Z_s to Z_l, which is the open-loop transfer function of system T_m. DC voltage is predicted to be stable when T_m satisfies the Nyquist stability criterion [12–14]:

$$V_{dc}(s) = (v_s(s) + i_l(s)Z_s(s))(\frac{1}{1+T_m}) \quad (52)$$

$$T_m = \frac{Z_s(s)}{Z_l(s)}. \quad (53)$$

4.1. Impact of the Power Flow Direction

Figure 8a shows the Nichols plots of an open-loop transfer function T_m when the transmission power is ±500 MW and the length of the DC cable is 50 km. The traditional control strategy [13] shown in Figure 3 is adopted to a DC-voltage-controlled converter, and controller parameters are set as k_{pvdc} = 15, k_{ivdc} = 100.



(a)

Figure 8. *Cont.*

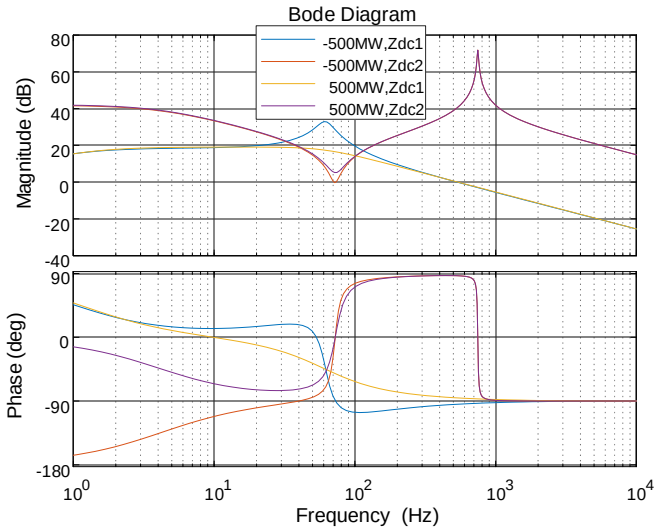


Figure 8. (**a**) Nichols plots of T_m when transmission power is ±500 MW. (**b**) Impedance frequency responses of Z_{dc1} and Z_{dc2} when transmission power is ±500 MW.

As shown in Figure 8a, the red line does not encircle (−180°, 0), and the VSC–HVDC system is predicted to be stable. The blue encircles (−180°, 0), and the VSC–HVDC system is predicted to be unstable.

Figure 8b shows the impedance frequency responses of Z_{dc1} and Z_{dc2} when the active power is set as ±500 MW. Compared with the yellow line and the blue line, in the mid-frequency band, the blue line shows negative damping while the yellow line does not. Z_{dc1} and Z_{dc2} intersect at the mid-frequency band due to the influence of DC cable impedance. The phase difference at the red line and blue line in the mid-frequency band is approximately 180°, so the DC voltage is predicted to oscillate. The stability analysis results are consistent with the simulation results in Figure 4.

4.2. Impact of Virtual Impedance by Frequency Responses

Figure 9 shows the impedance frequency responses of Z_{dc1} and Z_{dc2} when the active power is set as −500 MW and the length of DC cable is 50 km. The proposed strategy in this paper is adopted for a DC-voltage-controlled converter, and the controller parameters are set as $k_{pvdc} = 15$, $k_{ivdc} = 100$, and $k_i = 10$. Figure 9a shows the impedance frequency responses of Z_{dc1} under a different R_{eq}s. The pink line represents Z_{dc2} and the blue, red, and yellow lines represents Z_{dc1} when $R_{eq} = 0.5$, 2 and 5, respectively. The blue line shows that when the phase of Z_{dc1} impedance in the mid-frequency band is below −90°, the system exhibits negative damping. The phase difference at the intersection of the pink and blue lines in the mid-frequency band is approximately 180°, and the DC voltage is predicted to oscillate. The red and yellow lines show that when the phase of Z_{dc1} impedance in the mid-frequency band is above -90°, and the phase difference is less than 160 degrees, the DC voltage is predicted to stable. However, with the increase of R_{eq}, the phase difference at the intersection of the pink and blue lines in low-frequency bands increases, and the system tends to lose stability.

Figure 9b shows impedance frequency responses of Z_{dc1} under a different L_{eq}s. The pink line represents Z_{dc2} and the blue, red, and yellow lines represent Z_{dc1} when $L_{eq} = 0.002$, 0.02, and 0.05, respectively. Blue line shows that phase of Z_{dc1} impedance in mid-frequency band is below −90°, the system exhibits negative damping. The phase difference at the intersection of the pink and blue lines in the mid-frequency band is approximately 180°, and the DC voltage is predicted to oscillate. Red and yellow lines show that when the phase of Z_{dc1} impedance in the mid-frequency band is above −90°, and the phase difference is less than 160 degrees, the DC voltage is predicted to be stable.

However, with the increase of L_{eq}, the phase difference at the intersection of the pink and blue lines in the low-frequency band increases, and the system tends to lose stability.

The conclusion is that if the virtual impedance is too small, it will not be enough to suppress the oscillation. If the virtual impedance is too large, a new oscillation may occur in the low frequency band.

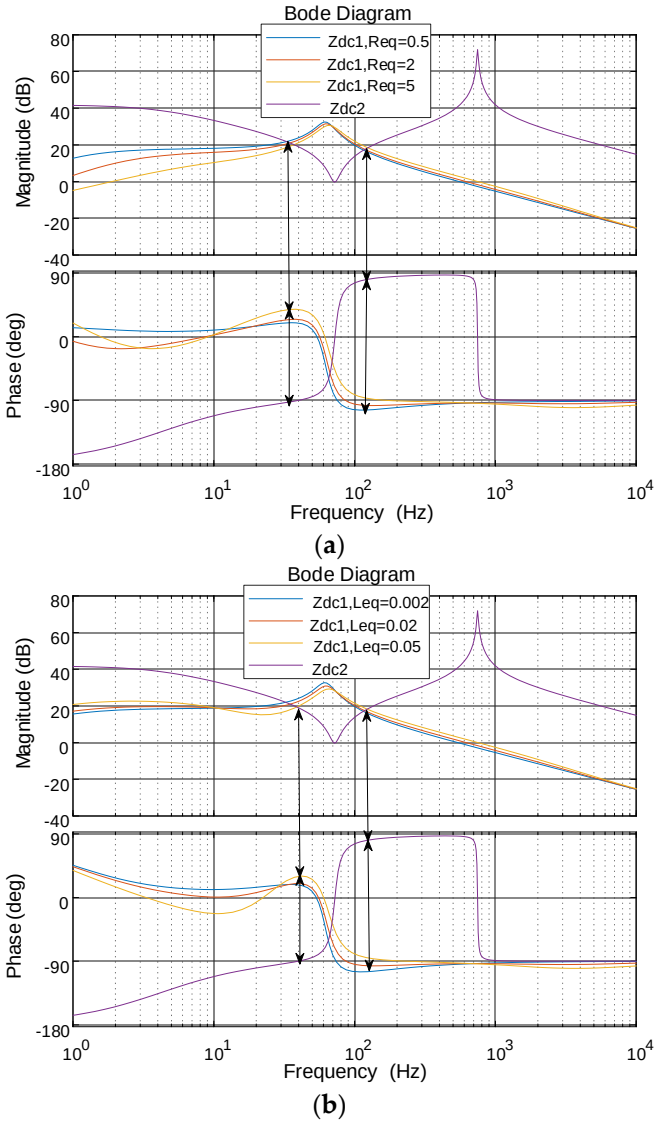
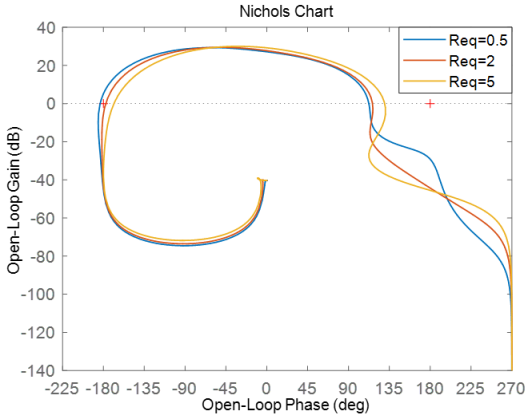


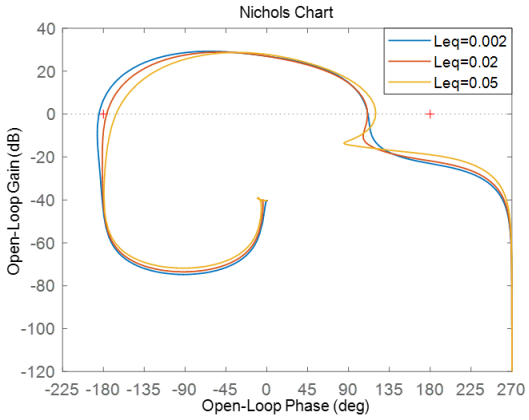
Figure 9. Impedance frequency responses of Z_{dc1} and Z_{dc2} under different equivalent virtual impedance values (**a**) R_{eq} and (**b**) L_{eq}.

4.3. Impact of Virtual Impedance Parameters by Nichols Plots

Figure 10 shows the Nichols plots of T_{m} with different virtual impedance parameters. The DC cable length is 10 km and the transmission power is −500 MW. The proposed strategy in this paper is adopted to the DC-voltage-controlled converter, and the controller parameters are set as $k_{pvdc} = 15$, $k_{ivdc} = 100$, and $k_i = 10$. The blue, red, and yellow lines in Figure 10a show the Nichols plots of T_{m} when the virtual impedance parameters R_{eq} are 0.5 Ω, 2 Ω, and 5 Ω, respectively. Figure 10a shows that T_{m} encircles (−180°, 0), and the system is predicted to be unstable when $R_{eq} = 0.5$ Ω. The system is predicted to be stable when $R_{eq} = 2$ and 5 Ω. Increasing the R_{eq} value in a certain range helps improve the stability of the system. The phase margin of the system is insufficient to suppress DC-side oscillation when $R_{eq} = 0.5$ Ω.



(**a**)



(**b**)

Figure 10. Nichols plots of T_m under different equivalent virtual impedance values (**a**) R_{eq}; (**b**) L_{eq}.

The blue, red, and yellow lines in Figure 10b show the Nichols plots of T_{m} when virtual impedance parameters L_{eq} are 0.002 Ω, 0.02 Ω, and 0.05 Ω, respectively. Figure 10b shows that T_{m} encircles (−180°, 0), and the system is predicted to be unstable when L_{eq} = 0.002 Ω. The system is predicted to be stable when L_{eq} = 0.02 and 0.05 Ω. Increasing the L_{eq} value in a certain range helps improve the stability of the system. The phase margin of the system is insufficient to suppress DC-side oscillation when L_{eq} = 0.002 Ω.

4.4. Impact of DC Cable Length

Figure 11 shows the Nichols plots of the open-loop transfer function T_m under different lengths of DC cable when the transmission power is −500 MW. The control parameters are k_{pvdc} = 15, k_{ivdc} = 100, k_i = 10, R_{eq} = 0.5 Ω, and L_{eq} = 0.002 Ω. The blue, red and yellow lines in Figure 11 represent the Nichols plots of T_m at DC cable lengths of 50, 100, and 150 km, respectively. As shown in Figure 11, the Nichols plot gradually approaches (−180°, 0), with a decrease in DC cable length. The Nichols plot encircles (−180°, 0), and the system is predicted to be unstable when the DC cable length is reduced to 50 km.

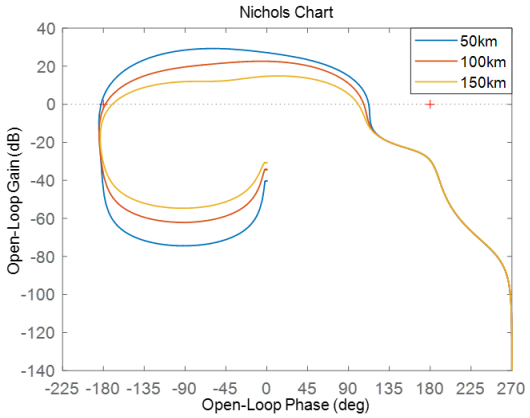


Figure 11. Nichols plots of T_m under different DC cable lengths.

4.5. Impact of DC Side Capacity

Figure 12 shows the Nichols plots of the open-loop transfer function T_m under a different capacitance of the DC side capacity when the transmission power is −500 MW. The control parameters are k_{pvdc} = 15, k_{ivdc} = 100, k_i = 10, R_{eq} = 0.5 Ω, and L_{eq} = 0.002 Ω. The blue, red, and yellow lines in Figure 12 represent the Nichols plots of T_m at the DC side capacity of 300, 450, and 600 μf, respectively. As shown in Figure 12, the Nichols plot gradually approaches (−180°, 0), with a decrease in the DC side capacity. The Nichols plot encircles (−180°, 0), and the system is predicted to be unstable when the DC side capacity is reduced to 300 μf.

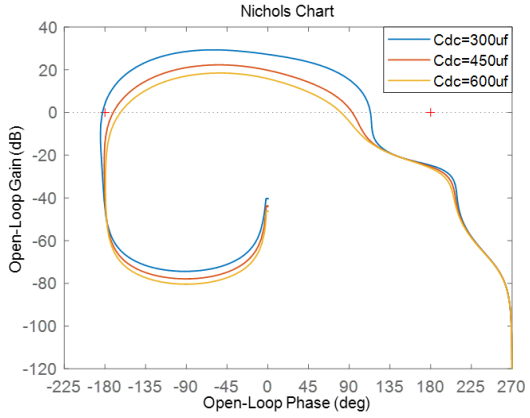


Figure 12. Nichols plots of T_m under different DC side capacities.

From the above stability analysis, it can be concluded that there are three main factors affecting the stability of the system—power flow [24], main circuit parameters, and controller parameters. Among the main circuit parameters, the most important factors are the length of the circuit and the capacitance of the DC side. According to the stability, analysis results in 4.4 and 4.5. The stability margin of the system can be improved by increasing the DC capacitance and DC cable length. When the main circuit parameters are determined and the power flow is determined, the stability of the system can also be improved by optimizing the controller settings.

4.6. Impact of Grid Impedance

Figure 13 shows the Nichols plots of the open-loop transfer function T_m under different grid impedance when the transmission power is −500 MW. The control parameters are k_{pvdc} = 15, k_{ivdc} = 100, k_i = 10, and L_{eq} = 0.02 Ω. The blue and red lines in Figure 13 represent the Nichols plots of T_m when L_n = 1 and 5 mH, respectively. The blue line does not encircle (−180°, 0), while the red line encircles

(−180°, 0), which means and DC-side oscillations are more likely to occur in weaker power grids. The yellow line in Figure 13 represents the Nichols plot of T_m when L_n = 5 mH and R_{eq} = 2. The yellow line does not encircle (−180°, 0), which means the system is predicted to be stable after choosing appropriate virtual impedance parameters.

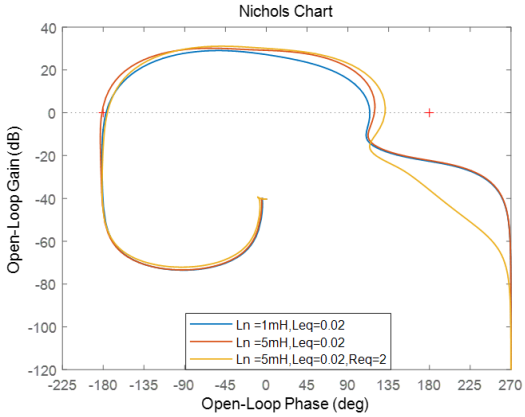


Figure 13. Nichols plots of T_m under a different grid impedance.

5. Simulation Verification

5.1. Impact of DC Cable Length

Figure 14 shows the simulation results of the VSC–HVDC system with virtual impedance control strategy under different DC cable lengths. The voltage control parameters are k_{pvdc} = 15, k_{ivdc} = 100, k_i = 10, R_{eq} = 0.5 Ω, and L_{eq} = 0.002 Ω. At 2 s, the steady-state power command value is set from 500 MW to −500 MW. As shown in Figure 14, the blue line indicates the simulation results when the DC cable length is 50 km, and the red line indicates 100 km. The DC voltage in the blue line drops by approximately 5% and begins to oscillate, and the system loses stability. The DC voltage in the red line drops by approximately 5%, smoothly restoring the instruction value, and the system remains stable. The simulation results are consistent with the theoretical analysis in Section 4.4.

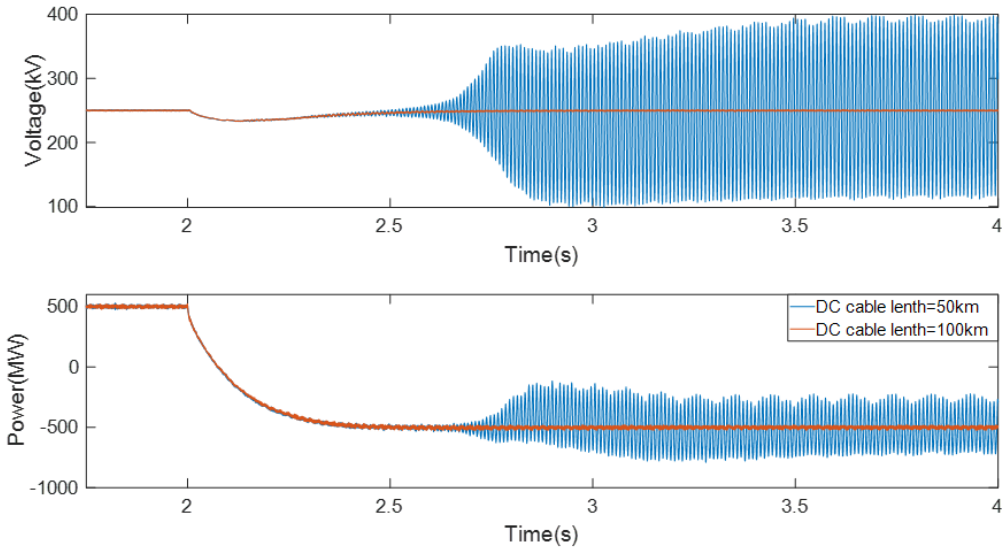


Figure 14. DC-link voltage and active power of the VSC–HVDC system under different DC cable lengths.

5.2. Impact of DC Side Capacity

Figure 15 shows the simulation results of the VSC–HVDC system with a virtual impedance control strategy under a different DC side capacity. The voltage control parameters are k_{pvdc} = 15, k_{ivdc} = 100, k_i = 10, R_{eq} = 0.5 Ω, and L_{eq} = 0.002 Ω. At 2 s, the steady-state power command value is set from 500 MW to −500 MW. As shown in Figure 15, the blue line indicates the simulation results when the DC side capacity is 300 μf, and the red line indicates 450 μf. The DC voltage in the blue line drops by approximately 5% and begins to oscillate, and the system loses stability. The DC voltage in the red line drops by approximately 5%, smoothly restoring the instruction value, and the system remains stable. The simulation results are consistent with the theoretical analysis in Section 4.5.

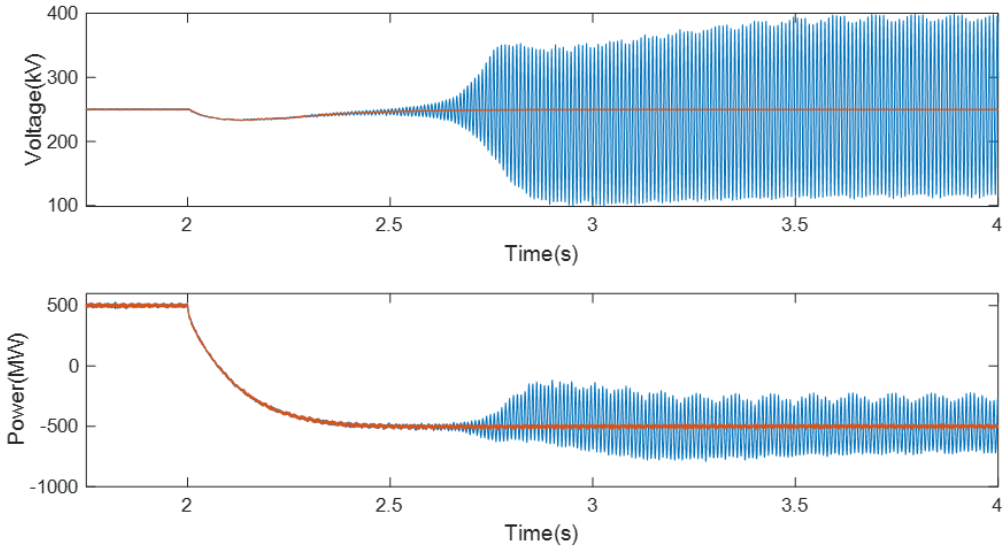


Figure 15. DC-link voltage and active power of the VSC–HVDC system under different DC side capacity.

5.3. Dynamic Performance Comparison

According to [13], reducing the value of k_{pvdc} can improve the output impedance of the DC-voltage-controlled converter, thereby reinforcing the stability of the system. However, this condition influences the dynamic performance of the control. This paper compares the dynamic performance of the two control strategies. Similarly, the DC cable length is 50 km, and the active power instruction changes from 500 MW to −500 MW at 2 s. As shown in Figure 16a, the blue line represents the DC voltage under the traditional control strategy [13]. When k_{pvdc} = 5 and k_{ivdc} = 100, the red line represents the DC voltage under the proposed control strategy when k_{pvdc} = 15, k_{ivdc} = 100, k_i = 10 and R_{eq} = 2 Ω, and the yellow line represents the DC voltage under the proposed control strategy when k_{pvdc} = 15, k_{ivdc} = 10, k_i = 10, and L_{eq} = 0.02 Ω. The DC voltage in the blue line drops by approximately 9% when the instruction value is changed and gradually increases to the instruction value. The DC voltage in the red line drops by only 2% when the instruction value is changed and increases the instruction value by more than 2%. The DC voltage in the yellow line drops by only 4% when the instruction value is changed and gradually increases to the instruction value. The dynamic performance of the proposed control strategy is better than that of the traditional control method.

Figure 16b compares system DC voltages under the proposed control strategy with different virtual impedance parameters when k_{pvdc} = 15, k_{ivdc} = 100 and k_i = 10. The blue line represents R_{eq} = 0.5, L_{eq} = 0.02 Ω, the red line represents R_{eq} = 2 Ω, L_{eq} = 0.02 Ω, and the yellow line represents R_{eq} = 2 Ω, L_{eq} = 0.002 Ω. From the comparison of these three lines, it can be seen that the speed of DC voltage regulation mainly depends on R_{eq}. As can be seen from Figure 9a, increasing R_{eq} can reduce the amplitude response of Z_{dc1} in the low-frequency band. However, increasing L_{eq} has little effect on the amplitude response of Z_{dc1} in the low-frequency band, as in Figure 9b.

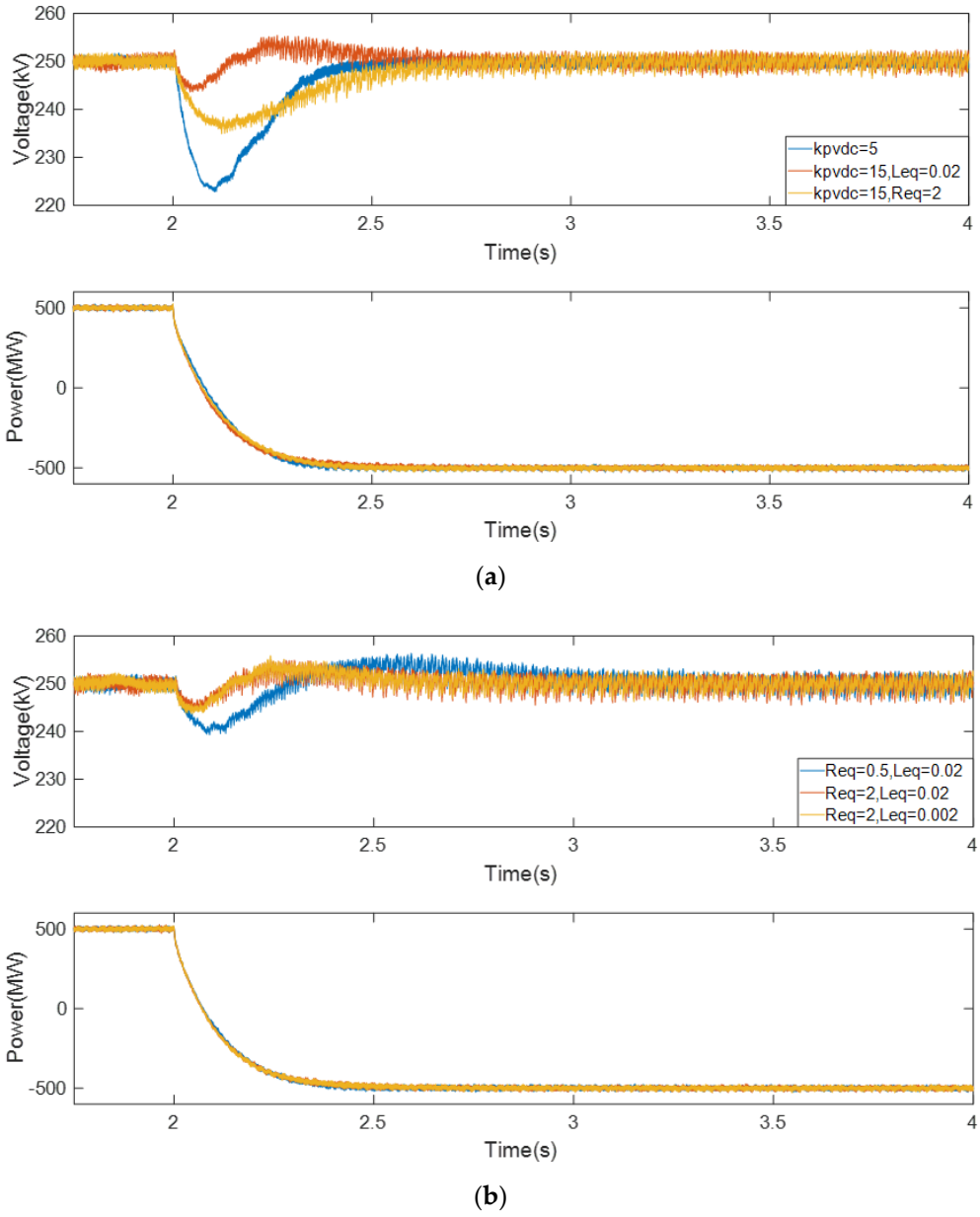


Figure 16. DC-link voltage and active power of the VSC–HVDC system (**a**) under the proposed control strategy and traditional control strategy [13] and (**b**) under the proposed control strategy with different virtual impedance parameters.

5.4. Steady State Error Elimination

On the basis of the previous analysis, although the traditional virtual impedance control strategy can enhance the transmission capacity of the system, it causes the steady-state error of DC voltage. Figure 17 shows the comparison of two virtual impedance control strategies. The length of the DC cable is 50 km. At 2 s, the steady-state power command value is set from 500 MW to −500 MW.

The DC voltage in the blue line represents the traditional virtual impedance, shown as the yellow frame in Figure 5, and the controller parameters are k_{pvdc} = 15, k_{ivdc} = 100, and R_{eq} = 2 Ω. The DC voltage in the red line represents the proposed control strategy, with k_{pvdc} = 15, k_{ivdc} = 100, R_{eq} = 2 Ω, and k_i = 10. Under the two control strategies, the DC voltage fluctuates in a short time and a small range only, and the active power can steadily step down. The DC voltage shown by the red line is close to the instruction value of 250 kV, and the steady-state error of the blue line is approximately 5 kV in both power flow directions, which are consistent with the theoretical analysis. The simulation

results show that the improved virtual impedance control method can improve the stability of the DC system and eliminate the steady-state error of the DC voltage caused by the virtual impedance.

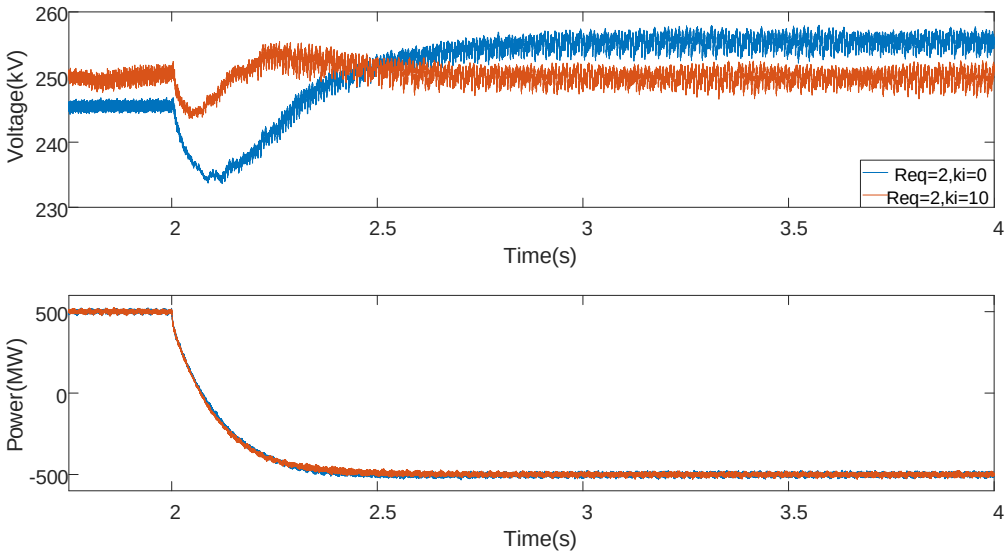


Figure 17. DC-link voltage and active power of the VSC–HVDC system under the proposed control strategy and traditional virtual impedance.

5.5. Impact of Gird Impedance

Figure 18 shows the simulation results of the VSC–HVDC system with a virtual impedance control strategy under a different grid impedance. The voltage control parameters are $k_{pvdc} = 15$, $k_{ivdc} = 100$, $k_i = 10$, and the transmission power is set as −500 MW. At 2 s, the grid impedance is switched from 1 mH to 5 mH. The blue line in Figure 18 indicates the simulation results when the virtual impedance parameter is $L_{eq} = 0.02\ \Omega$. The DC voltage in the blue line begins to oscillate, and the system loses stability. The red line in Figure 18 indicates the simulation results when virtual impedance parameters are $L_{eq} = 0.02\ \Omega$ and $R_{eq} = 2\ \Omega$. The DC voltage in the red line stays stable, and the system remains stable. The simulation results are consistent with the theoretical analysis in Section 4.6.

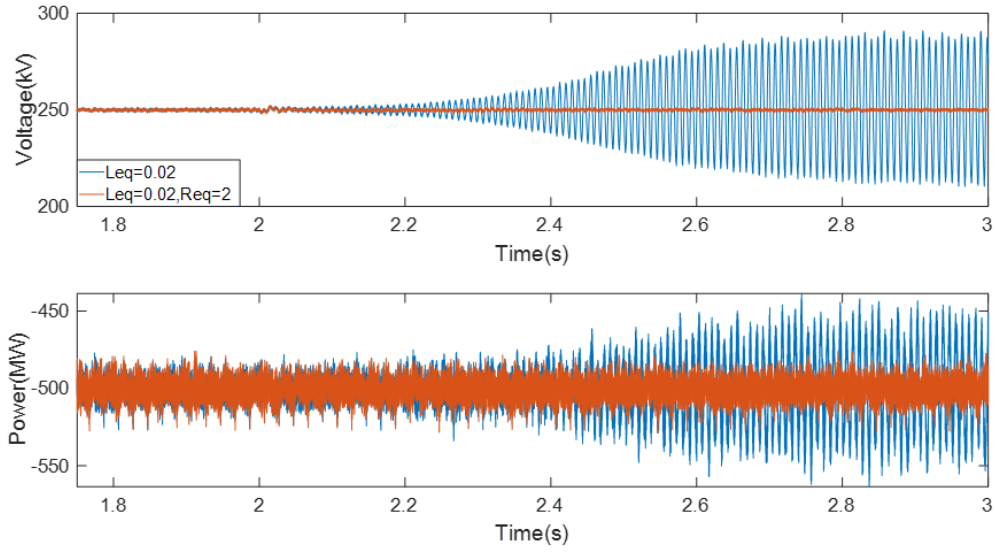


Figure 18. DC-link voltage and active power of the VSC–HVDC system under different gird impedance.

6. Conclusions

This paper investigates the stability of VSC–HVDC operation in a bidirectional power flow mode. DC cable length affects the reverse power transmission power of the system. An improved virtual impedance control strategy is presented to increase the reverse power transmission power of the system. A system stability analysis based on the impedance model is applied to the proposed control strategy. System stability is affected by the power flow, controller parameters, DC cable length, and DC side capacity.

(1) DC-side oscillation occurs when the transmission power of the system is large. The maximum transmission power of a DC voltage-controlled converter to a power-controlled converter is less than that in the opposite transmission direction.
(2) The shorter the DC cable is, the more easily the oscillation of DC voltage will occur.
(3) The smaller the DC side capacity is, the more easily the oscillation of DC voltage will occur.
(4) The weaker the AC grid strength is, the more easily the DC side oscillation will occur.
(5) Appropriate virtual impedance parameters can improve system stability. The phase margin of the system is insufficient to suppress DC-side oscillation when the virtual impedance parameter is small. If the virtual impedance parameters, R_{eq} or L_{eq}, are too large, then the system will enter a new unstable state.

The simulation results show that the proposed improved control strategy can eliminate the steady-state error of DC voltage caused by virtual impedance and maintain the advantage of a virtual impedance strategy to improve system stability. The proposed control method has better dynamic performance compared to the traditional control method.

Author Contributions: All the authors have contributed to this paper in different aspects. Y.L. proposed the original concept and wrote the original draft. K.L. acted as supervisor and gave suggestions on paper improvement. S.Z., X.L., and Q.H. helped with software simulation and methodology improvement.

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Conflicts of Interest: The authors declare no conflict of interest.

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