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Bridgeless Buck-Boost PFC Rectifier with Positive Output Voltage

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Abstract: A bridgeless buck-boost power-factor-correction (PFC) rectifier with positive output voltage is proposed herein. This PFC rectifier operates in the discontinuous conduction mode (DCM). Owing to the DCM, a good performance on PF is easily achieved as well as no reverse recovery currents being generated from the diodes. By means of output voltage sensing along with the traditional voltage-follower control, a proper control force is created to drive the switches. By doing so, not only the output voltage is stably controlled at a given value, but also the input current tracks the input voltage as tightly as possible. In addition, the accompanying harmonic distortion meets the requirements of the IEC6100-3-2 Class C harmonics standard, and accordingly, the proposed rectifier is suitable for the AC-DC LED driver. Finally, via mathematical deductions and experimental results, the effectiveness of the proposed bridgeless buck-boost PFC rectifier is verified.

Keywords: bridgeless; buck-boost; BCM; DCM; PFC rectifier; voltage-follower control

1. Introduction

The AC-DC rectifier with power factor correction (PFC) takes an important role not only in energy saving but also in reduction of the total harmonic distortion (THD). Harmonics standards, such as IEC61000-3-2 [1], JIS-C-61000-3-2, etc., are offered to limit the harmonics generated from the electronic products. For example, the electronic products with output power above 75 W need to pass the corresponding harmonics tests.

There are two kinds of PFC rectifiers. The first kind is named passive PFC rectifier [2,3], which is mainly built up by the inductor, the capacitor and the diode. This kind possesses advantages of circuit simplicity, low cost, and so on, but has disadvantages of large size, heavy weight, low efficiency, low circuit flexibility, and so on. Since the passive PFC rectifier does not work well, the second kind, named active PFC rectifier, is proposed [4,5]. Generally, this kind is mainly constructed by the switch, the inductor, and the diode. The rectifier can make the input current tightly track the input voltage via the proper turning-on of the switch under different input voltages and various output loads. By doing so, the input current can easily meet the required harmonics standard. Compared with the passive PFC rectifiers, the active PFC rectifier has many advantages, such as small size, light weight, high power density, high PF, low THD, etc.

There are three kinds of non-isolated converters widely utilized in the active rectifier: boost, buck, and buck-boost converters. Among them, the active PFC boost rectifier is commonly employed [6–8]. The key merit of this kind is that the current in the input inductor operates in the continuous conduction mode (CCM), thereby obtaining a high PF and a low THD. However, such a kind can be used only under the condition that the output voltage is larger than the peak value of the input voltage.

Consequently, the active buck PFC rectifier is presented [9–11]. Such a rectifier can transfer a high input AC voltage to a low DC voltage. However, as the input voltage is lower than the output

voltage, there is no input current, thus making zero-crossing distortion occur. Consequently, even if this rectifier operates in the CCM, the PF is relatively low and the THD is relatively high.

Based on the aforementioned, the active buck-boost PFC rectifier is proposed [12–14]. In the CCM, such a PFC rectifier possesses relatively high variations in output voltage due to step-up/step-down of the input voltage. However, the output voltage of this rectifier is negative. Consequently, its industrial applications are limited.

On the other hand, the power loss in low-frequency diodes of the traditional active PFC rectifier is huge. Hence, to remove this diode loss, some researchers present bridgeless active PFC rectifiers using high-frequency diodes and switches [15–17].

Accordingly, a bridgeless buck-boost PFC rectifier with positive output voltage is proposed herein. This circuit is derived from the circuit shown in [17] by Jovanovic, M.M.; Jang, Y. The total component count of the proposed circuit is the same as that of the circuit shown in [17]. Basically, there is a difference in specifications between the proposed circuit and the circuit shown in [17], and the comparison between the two is not easy. However, from the point of view of voltage gain in the BCM or CCM, the former has a value of D/(1-D), locating between zero and infinity, where D is the duty cycle, and the latter has a value of 2D, locating between zero and two. This means that the former has relatively low zero crossover distortion as compared to the latter. Namely, the proposed circuit has better performance of PFC and THD than the circuit shown in [17] has. Furthermore, in the proposed circuit, the rectification switches S_1 and S_2 are back-to-back cascaded in the opposite direction, and thus only one gate driver is required.

2. Overall System Configuration

Figure 1 displays the overall system configuration for the proposed circuit. The main power stage contains four high-switching-frequency diodes, D_1, D_2, D_3, and D_4, three high-switching-frequency switches, S_1, S_2 and S_3 with individual gate drivers, one output diode D_o, one output capacitor C_o, and one inductor L. Regarding the control stage, it contains one voltage divider, one analogue-to-digital converter, named *ADC*, and one field programmable gate array, named *FPGA*. The output resistor is signified by R. Note that the switch S_3 is utilized to make the output voltage positive.

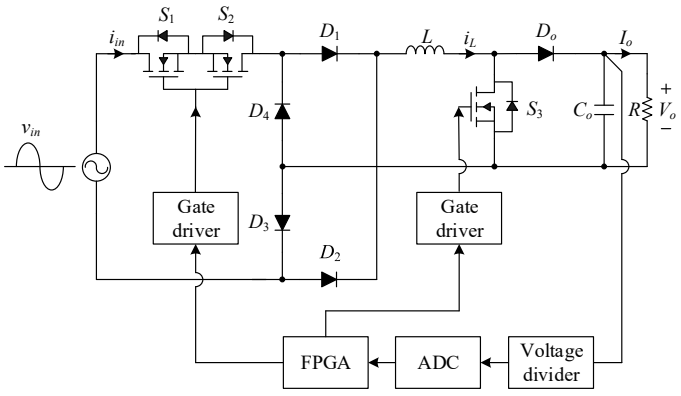


Figure 1. Overall system configuration for the proposed circuit.

The output voltage is sensed from the main power stage and passed to the voltage divider and then to the ADC to generate a digital value. Afterwards, such a digital value is passed to the controller embedded in the FPGA to yield three proper PWM signals for S_1, S_2 and S_3. Note that the voltage-follower control is employed herein. This is because if the main power stage operates in the DCM, the corresponding power factor is inherently high [18].

In addition, the proportional-integral (PI) controller embedded in the FPGA can make the proposed converter operated stably. The parameters of this controller are obtained by the industrial try-and-error tuning method as follows.

Step 1 Under the input nominal voltage of 110 V_{rms} and rated output power, the integral gain k_i is first set to zero, and then the proportional gain k_p is gradually increased, so that the value of k_p stops being increased until the output voltage reaches 75% of the desired value.

Step 2 Under the same conditions, the value of k_p obtained from step 1 is fixed, and then the value of k_i is gradually increased, so that the output voltage is stabilized at the desired value without oscillation.

Step 3 Under the input nominal voltage of 110 V_{rms} but different output powers, the values of k_p and k_i are finely tuned, so that the output voltage is stabilized at the desired value for all the output power range.

Step 4 Change the input voltage levels, and repeat step 3, so that the output voltage is stabilized at the desired value for all the input voltage range and all the output power range.

3. Basic Operating Principles

For analysis convenience, some assumptions are given below:

(1). All the switches, diodes, inductor and capacitor are considered as ideal.
(2). The PWM signals for S_1, S_2 and S_3 are the same.
(3). The value of C_o is large enough to render the voltage across it constant at V_o.
(4). The circuit operates in the DCM.

According to these above assumptions, Figure 2 shows the key waveforms for the proposed PFC rectifier operating under the positive input voltage. There are six states are to be described as following.

(1) *State 1* [$0 \le t \le DT_s$]: As the voltage v_{in} is positive, S_1, S_2, S_3, D_1, and D_3 are ON, whereas D_2, D_4, and D_o are OFF. During this state, the current i_{in} flows through S_1, S_2, S_3, D_1, D_3, and L, as shown in Figure 3a. At the same time, as shown in Figure 2, the voltage across L is v_{in}, making L magnetized and the current i_L increasing linearly. Moreover, the output energy needed is offered by C_o.

(2) *State 2* [$DT_s \le t \le (D+\Delta)T_s$]: As the input voltage is still positive, S_1, S_2, and S_3 are OFF, whereas D_1, D_2, D_3, D_4 and D_o are ON. During this state, the current i_{in} is zero, whereas the current i_L continuously flows through these five diodes, as shown in Figure 3b. At the same time, as shown in Figure 2, the voltage across L is $-V_o$, rendering L *is* demagnetized and the current i_L decreasing linearly. In addition, the output energy needed is provided by the energy stored in L.

(3) *State 3* [$(D+\Delta)T_s \le t \le T_s$]: As the input voltage still keeps positive, S_1, S_2, S_3, D_1, D_2, D_3, D_4 and D_o are OFF, as shown in Figure 3c. Namely, there is no current flowing through L, as shown in Figure 2, and hence the output energy needed is supplied from C_o.

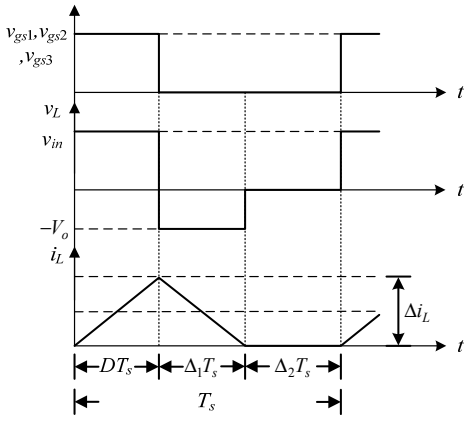


Figure 2. Voltage and current of the inductor operating in the discontinuous conduction mode (DCM) under the positive input voltage.

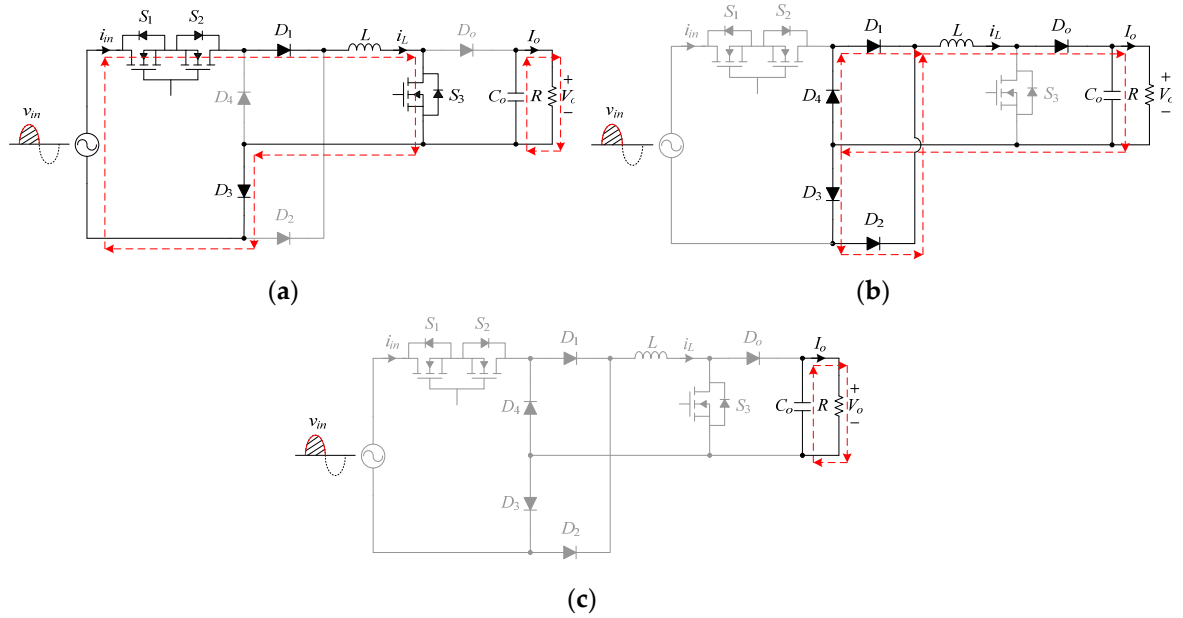


Figure 3. Power flow in: (**a**) state 1; (**b**) state 2; (**c**) state 3.

For the negative input voltage to be considered, there are also three states, that is, states 4, 5 and 6. The behavior in state 4 is similar to that in state 1 except that the diodes D_1 and D_3 conducted in state 1 is replaced by the diodes D_2 and D_4 conducted in state 4. Also, the behaviors in states 5 and 6 are the same as those in states 2 and 3, respectively.

Based on the volt-second balance for the inductor L, the following equation must be held:

$$\frac{1}{L}\cdot v_{in}\cdot D\cdot T_s + \frac{1}{L}\cdot(-V_o)\cdot\Delta_1\cdot T_s + \frac{1}{L}\cdot 0\cdot\Delta_2\cdot T_s = 0 \tag{1}$$

Also,

$$D + \Delta_1 + \Delta_2 = 1 \tag{2}$$

By rearranging (1) according to (2), the voltage gain can be obtained:

$$\frac{V_o}{v_{in}} = \frac{D}{\Delta_1} \tag{3}$$

Equation (3) is only for the convertor working in the DCM. But if the converter operates in the BCM or CCM, then the value of Δ_2 will be zero and the voltage gain shown in (3) can be rewritten to

$$\frac{V_o}{v_{in}} = \frac{D}{1-D} \tag{4}$$

4. Design Considerations

Before we tackle this section, some specifications and assumptions are given below: (i) the input voltage range locates between 90 V_{rms} and 130 V_{rms} with a nominal voltage of 110 V_{rms}; (ii) the output voltage is set at 80 V; (iii) the output power range locates between 22.5 W and 90 W with a rated power of 90 W; (iv) the switching frequency is set at 100 kHz; (v) the rated-load efficiency under the minimum input voltage is set at assumed to be 90%; (vi) the line frequency is set at 60 Hz; (vii) the peak-to-peak value of the output voltage ripple is set at 3% of the output voltage; and (viii) the circuit always works in the DCM except that the circuit works in the BCM at the peak input current which happens under the minimum input voltage and the rated output power.

Furthermore, the sampling frequency is 100 kHz, synchronous with the switching frequency. The number of sampling bits out of the ADC is 10 bits. The voltage ratio of the voltage divider is 3 over 80. The number of PWM signal bits out of the FPGA is 10 bits.

In addition, the product name for the switches S_1 and S_2 and is IXTQ88N28T. The product name for the switch S_3 is STP120NF10. The product name for the diodes D_1, D_2, D_3, and D_4 is APT30D30BCT. The product name for the diode D_o is MBR40100PT. The inductor L has a value of 58.5 μH based on a CM270125 core with 18 turns. The capacitor is constructed by two paralleled Nippon Chemi-Con capacitors, 650 μF//650 μF.

4.1. Inductor Design

Firstly, it is assumed that the voltage v_{in} and the current i_{in} are purely sinusoidal and in phase. Therefore,

$$v_{in} = V_{in,pk} \sin\theta \tag{5}$$

$$i_{in} = I_{in,pk} \sin\theta \tag{6}$$

where $V_{in,pk}$ denotes the peak value of v_{in}, $I_{in,pk}$ indicates the peak value of i_{in}, ω_L equals $2\pi f_L$, f_L signifies the line frequency inversely proportional to the line period T_L, and θ equals $\omega_L t$.

Therefore, the average input power P_{in} can be obtained:

$$\begin{array}{ll} P_{in} & = \frac{1}{T_L} \cdot \int_{t_0}^{t_0+T_L} p_{in}(\theta) d\theta \\ & = \frac{1}{\pi} \cdot \int_0^{\pi} v_{in} \cdot i_{in} d\theta \end{array} \tag{7}$$

By substituting (5) and (6) into (7), P_{in} can be rewritten as

$$\begin{array}{ll} P_{in} & = \frac{1}{\pi} \cdot \int_0^{\pi} V_{in,pk} \sin\theta \cdot I_{in,pk} \sin\theta d\theta \\ & = \frac{V_{in,pk} I_{in,pk}}{\pi} \cdot \int_0^{\pi} \sin^2\theta d\theta \\ & = \frac{V_{in,pk} I_{in,pk}}{\pi} \cdot \int_0^{\pi} \frac{(1-\cos 2\theta)}{2} d\theta \\ & = \frac{V_{in,pk} I_{in,pk}}{2} \end{array} \tag{8}$$

Secondly, it has been assumed that the circuit works in the BCM at the peak input current under the minimum input voltage $V_{in,min,pk}$, named $I_{in,pk,max}$, and the rated output power $P_{o,rated}$. By taking the rated-load efficiency under the minimum input voltage, named η, into consideration, $I_{in,pk,max}$ can be represented based on (8) as

$$I_{in,pk,max} = 2 \cdot \frac{P_{o,rated}/\eta}{V_{in,min,pk}} \tag{9}$$

By putting the numerical values into (9), the calculated value of $I_{in,pk,max}$ can be obtained:

$$I_{in,pk,max} = 2 \times \frac{90/0.9}{90\sqrt{2}} = 1.57\text{A} \tag{10}$$

Thirdly, since the circuit works in the BCM only at the peak input current under the minimum input voltage and the rated output power, the maximum value of the peak value of i_L, named $I_{L,pk,max}$, can be represented by

$$I_{L,pk,max} = \frac{I_{in,pk,max}}{D} \tag{11}$$

where D corresponds to the peak value of i_L under the minimum input voltage and the rated output power.

Fourthly, the peak-to-peak value of i_L, named Δi_L, can be expressed as

$$\Delta i_L = \frac{V_o(1-D)T_s}{L} \tag{12}$$

Hence, if the inductor L operates in the DCM, the following criterion must be held:

$$\begin{array}{l} I_{L,avg,pk} \le \frac{\Delta i_L}{2} \\ \Rightarrow \frac{I_{in,pk,max}}{D} \le \frac{V_o(1-D)T_s}{2L} \\ \Rightarrow L \le \frac{V_o D(1-D)T_s}{2I_{in,pk,max}} \end{array} \tag{13}$$

Eventually, according to (10) and the specifications expressed at the beginning of Section 4, the following criterion based on (13) can be obtained:

$$L \le \frac{80 \times 0.386 \times (1-0.386) \times 10\mu}{2 \times 1.57} = 60.38\mu\text{H} \tag{14}$$

Hence, the value of L is set at 58.5 μH.

4.2. Output Capacitor Design

According to (5) and (6), the instantaneous input power $p_{in}(t)$ can be represented by

$$\begin{array}{rl} p_{in}(t) = & V_{in,pk} \sin \omega_L t \cdot I_{in,pk} \sin \omega_L t \\ & = V_{in,pk} \cdot I_{in,pk} \frac{(1-\cos 2\omega_L t)}{2} \end{array} \tag{15}$$

Also, the instantaneous output power $p_o(t)$ can be written as

$$p_o(t) = V_o \cdot i_{Do}(t) \tag{16}$$

By equalizing (15) and (16), the current flowing through D_o, named i_{Do}, can be expressed by

$$i_{Do}(t) = \frac{V_{in,pk} \cdot I_{in,pk} \cdot \eta}{2V_o} \cdot (1 - \cos 2\omega_L t) \tag{17}$$

Based on (17), the current flowing through C_o, named i_c, can be obtained to be

$$\begin{array}{rl} i_c(t) = & \frac{V_{in,rms} \cdot I_{in,rms} \cdot \eta}{V_o} \cdot (-\cos 2\omega_L t) \\ & = -I_o \cos 2\omega_L t \end{array} \tag{18}$$

where I_o is the output current.

Also,

$$v_c(t) = \frac{1}{C_o} \int i_c(t) dt \tag{19}$$

Therefore, based on (18) and (19), the output voltage ripple $\widetilde{v_o}$ can be represented as

$$\widetilde{v_o}(t) = \frac{-I_o}{2\omega_L C_o} \sin 2\omega_L t \tag{20}$$

From (20), the peak-to-peak value of the output voltage ripple, named Δv_o, can be expressed as

$$\Delta v_o = \frac{I_o}{\omega_L C_o} \tag{21}$$

Since the value of Δv_o is set at 3% of V_o, the value of Δv_o can be obtained:

$$\Delta v_o = V_o \cdot 3\% = 80 \times 0.03 = 2.4\text{V} \tag{22}$$

According to (21), (22) and the specifications given at the beginning of Section 4, the value of C_o can be worked out by setting I_o at the rated output current:

$$C_o = \frac{I_o}{\omega_L \Delta v_o} = \frac{1.125}{2\pi \times 60 \times 2.4} = 1243.4\mu\text{F} \tag{23}$$

Eventually, two Nippon Chemi-Con 650 µF capacitors, connected in parallel, are selected as C_o.

5. Experimental Results

Prior to this section, an input filter with corner frequency of about 10 kHz, constructed by one inductor of 500 µH and one capacitor of 470 nF, is put between the input voltage and the circuit, so as to remove high-frequency component of the input current. Figures 4–8 are measured at the rated output power and the input voltage of 110 V_{rms}. Figure 4 displays the input voltage v_{in} and the input current i_{in}. From Figure 4, it can be seen that the input current i_{in} tracks the input voltage v_{in} as tightly as possible, so as to realize power factor correction. Figure 5 shows the input current harmonic distribution, which meets IEC61000-3-2 Class C. Under the positive input voltage, Figure 6a displays the PWM signal for both S_1 and S_2, named $v_{gs1,2}$, and the voltages across the switches S_1 and S_2, named v_{ds1} and v_{ds2}, whereas under the negative input voltage, Figure 6b shows the PWM signal for both S_1 and S_2, named $v_{gs1,2}$, and the voltages across the switches S_1 and S_2, named v_{ds1} and v_{ds2}. From Figure 6a,b, as the switch S_1 or S_2 is turned off, the voltage across S_1 or S_2 is about 180 V. Note that under the positive cycle, as the PWM signal is low, the voltage across S_1 is high but the voltage across S_2 is zero due to forward bias of the body diode of S_2, whereas under the negative cycle, as the PWM signal is low, the voltage across S_2 is high but voltage across S_1 is zero due to forward bias of the body diode of S_1. Figure 7a displays the PWM signal v_{gs3}, and the voltage across the switch S_3. From Figure 7a, as the switch S_3 is turned off, the voltage across S_3 is about 80 V. Figure 7b shows the PWM signal for both S_1 and S_2, named $v_{gs1,2}$, and the current in L_1, named i_L, whereas Figure 8 displays the low-frequency output voltage ripple $\widetilde{v}_o$. From Figure 7b, it can be seen that the inductor works in the DCM, whereas from Figure 8, it can be seen that the peak-to-peak value of $\widetilde{v}_o$ is about 2.4 V, close to (22).

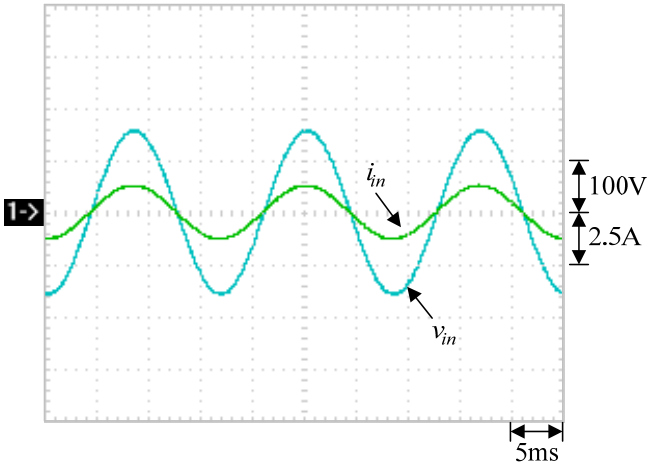


Figure 4. Experimental waveforms at rated output power under 110 V_{rms} input voltage: (1) v_{in}; (2) i_{in}.

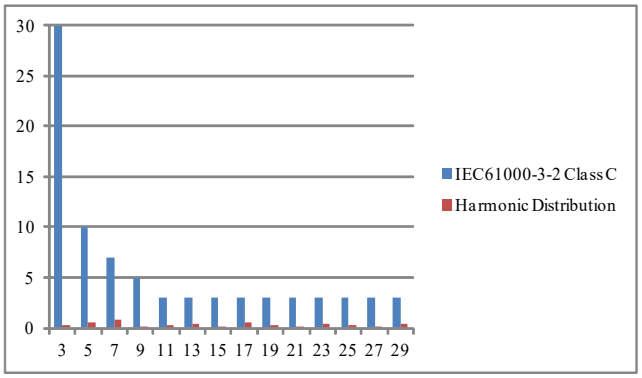


Figure 5. Experimental harmonics distribution at rated output power under 110 V_{rms} input voltage.

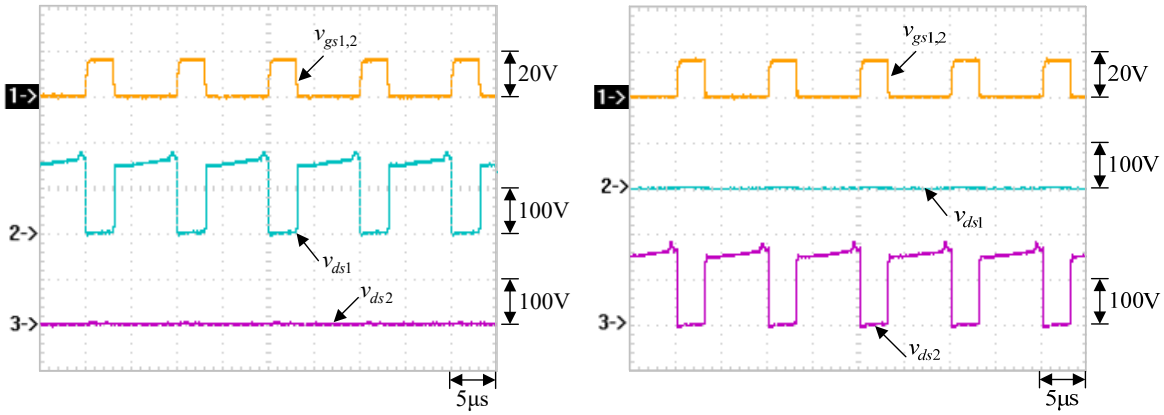


Figure 6. Experimental waveforms at rated output power under: (**a**) the peak value of the positive cycle of 110 V_{rms} input voltage: (1) $v_{gs1,2}$; (2) v_{ds1}; (3) v_{ds2}; (**b**) the valley value of the negative cycle of 110 V_{rms} input voltage: (1) $v_{gs1,2}$; (2) v_{ds1}; (3) v_{ds2}.

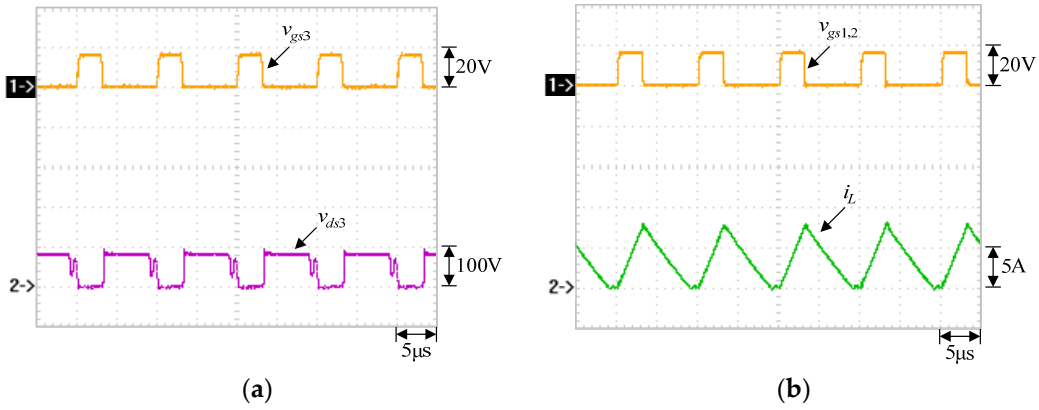


Figure 7. Experimental waveforms at rated output power under 110 V_{rms} input voltage: (**a**) (1) v_{gs3}; (2) v_{ds3}; (**b**) (1) $v_{gs1,2}$; (2) i_L.

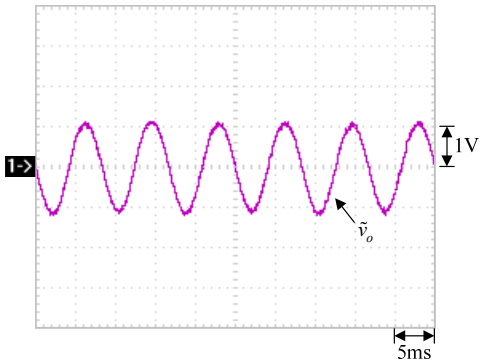


Figure 8. Experimental output voltage ripple $\widetilde{v_o}$ at rated output power under 110 V_{rms} input voltage.

In addition, by the same way, Figures 9–13 are measured under the input voltage of 90 V_{rms}, whereas Figures 14–18 are measured under the input voltage of 130 V_{rms}.

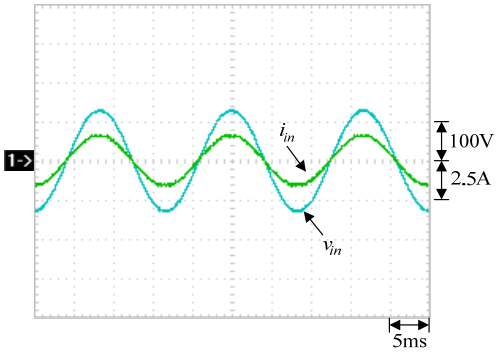


Figure 9. Experimental waveforms at rated output power under 90 V_{rms} input voltage: (1) v_{in}; (2) i_{in}.

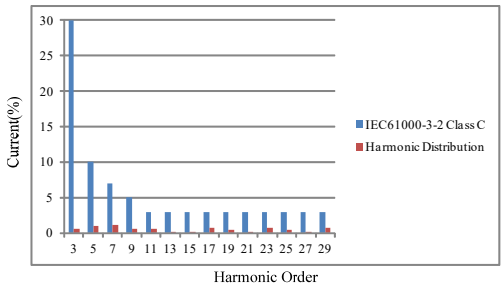


Figure 10. Experimental harmonics distribution at rated output power under 90 V_{rms} input voltage.

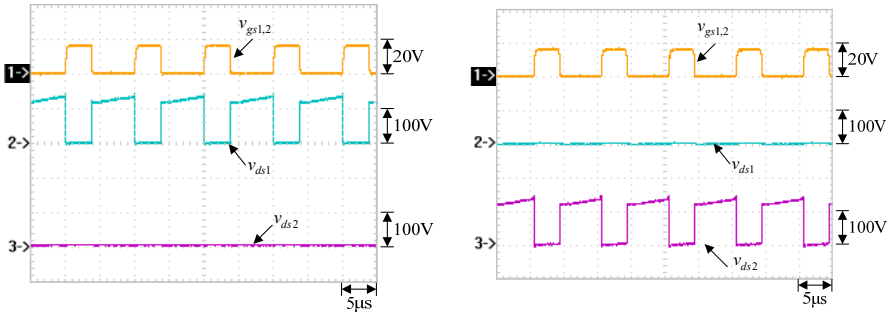


Figure 11. Experimental waveforms at rated output power under: (**a**) the peak value of the positive cycle of 90 V_{rms} input voltage: (1) $v_{gs1,2}$; (2) v_{ds1}; (3) v_{ds2}; (**b**) the valley value of the negative cycle of 90 V_{rms} input voltage: (1) $v_{gs1,2}$; (2) v_{ds1}; (3) v_{ds2}.

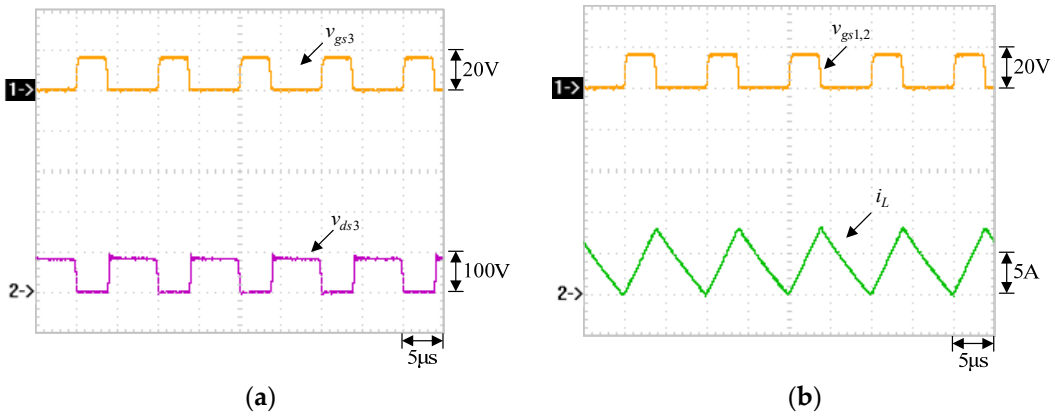


Figure 12. Experimental waveforms at rated output power under 90 V_{rms} input voltage: (**a**) (1) v_{gs3}; (2) v_{ds3}; (**b**) (1) $v_{gs1,2}$; (2) i_L.

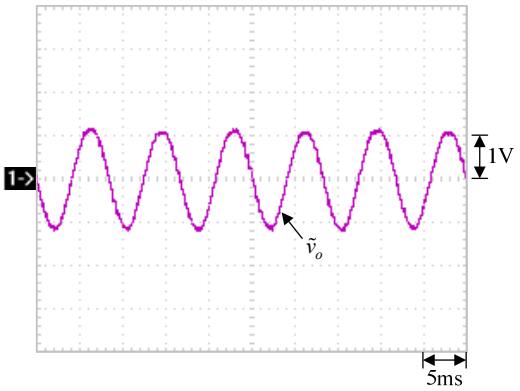


Figure 13. Experimental output voltage ripple $\widetilde{v_o}$ at rated output power under 90 V_{rms} input voltage.

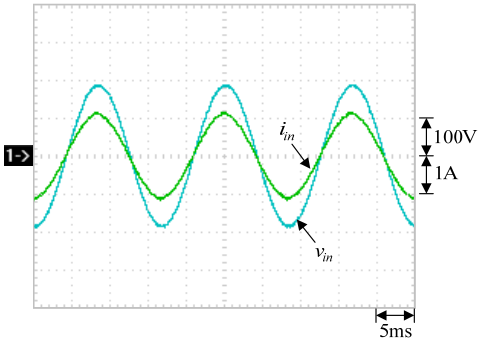


Figure 14. Experimental waveforms at rated output power under 130 V_{rms} input voltage: (1) v_{in}; (2) i_{in}.

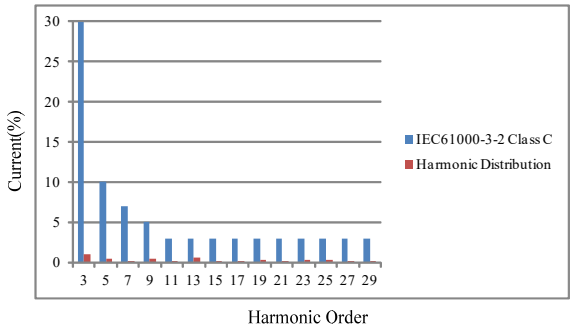


Figure 15. Experimental harmonics distribution at rated output power under 130 V_{rms} input voltage.

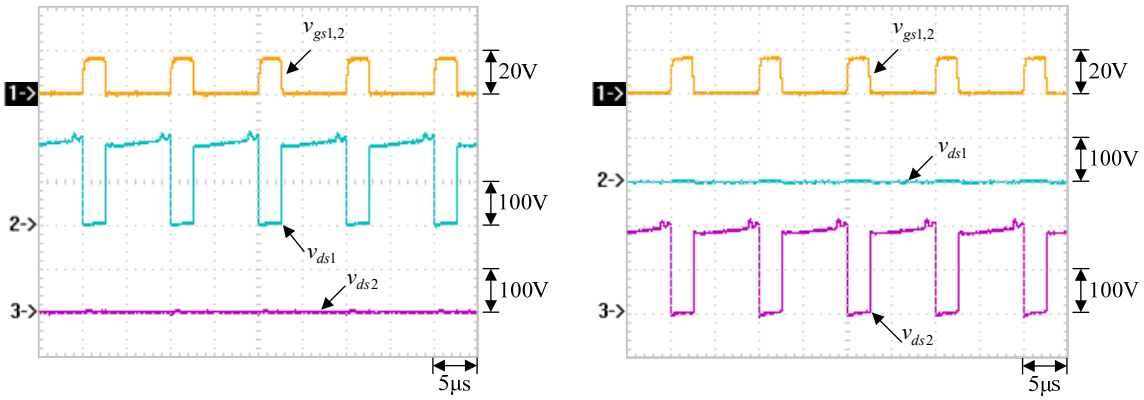


Figure 16. Experimental waveforms at rated output power under: (**a**) the peak value of the positive cycle of 130 V_{rms} input voltage: (1) $v_{gs1,2}$; (2) v_{ds1}; (3) v_{ds2}; (**b**) the valley value of the negative cycle of 130 V_{rms} input voltage: (1) $v_{gs1,2}$; (2) v_{ds1}; (3) v_{ds2}.

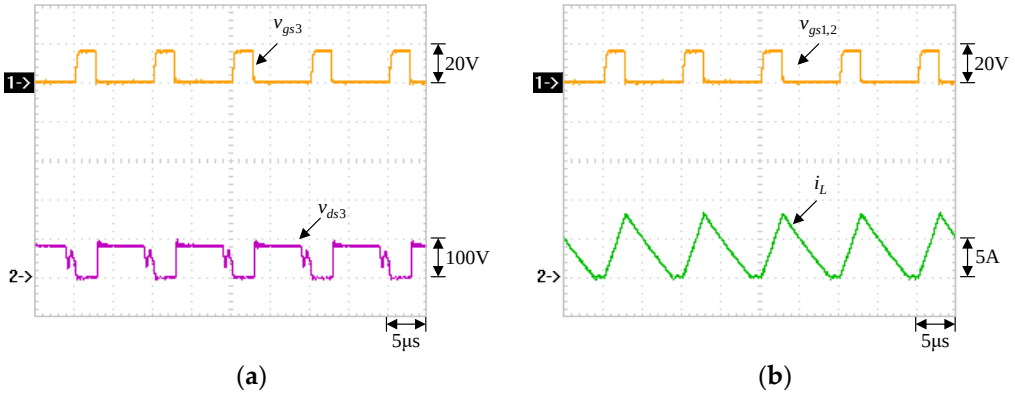


Figure 17. Experimental waveforms at rated output power under 130 V_{rms} input voltage: (**a**) (1) v_{gs3}; (2) v_{ds3}; (**b**) (1) $v_{gs1,2}$; (2) i_L.

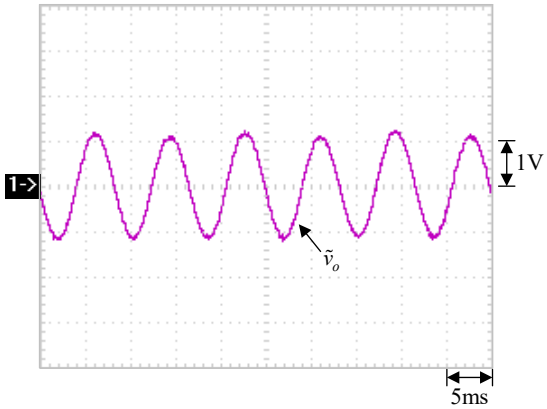


Figure 18. Experimental output voltage ripple $\widetilde{v}_o$ at rated output power under 130 V_{rms} input voltage.

Figure 19 displays the curves of total harmonic distortion versus output power under three input voltage levels. From this figure, it can be seen that all the values of THD are within 2%. Figure 20 shows the curves of power factor versus output power under three input voltage levels. From this figure, it can be seen that all values of PFC are above 0.971. Figure 21 displays the curves of efficiency versus output power under three input voltage levels. From this figure, it can be seen that all the

efficiency is above 91% and the efficiency can be up to 94.68%. In addition, Figure 22 shows a photo of the proposed circuit.

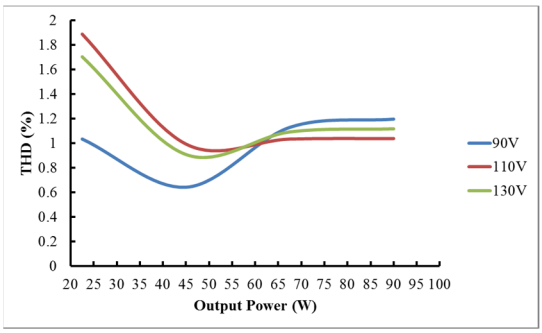


Figure 19. Curves of total harmonic distortion versus output power.

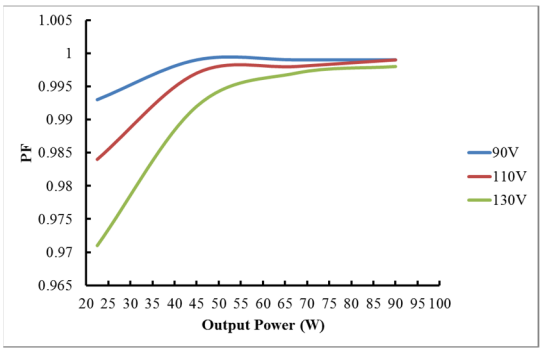


Figure 20. Curves of power factor versus output power.

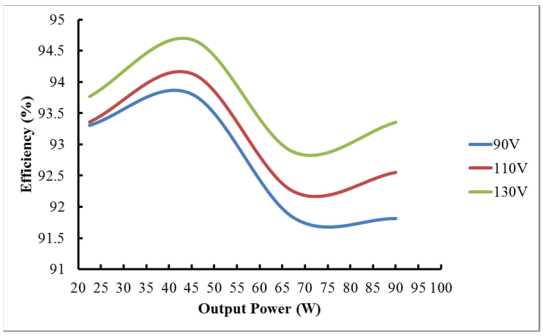
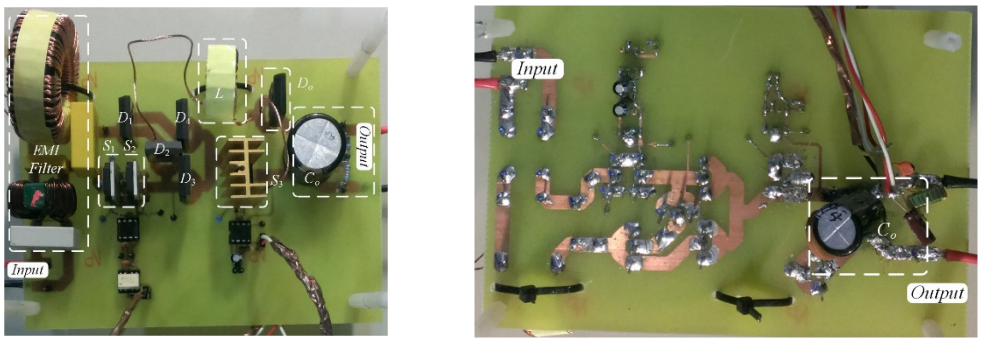


Figure 21. Curves of efficiency versus output power.



(**a**) (**b**)

Figure 22. Photo of the prototype of the proposed circuit: (**a**) top view; (**b**) bottom view.

6. Conclusions

A bridgeless buck-boost PFC rectifier with positive output voltage is proposed herein. For implementation convenience, this rectifier is operated in the DCM based on the voltage-mode control. By doing so, this rectifier has good performance on THD and PF, along with the output voltage controlled at a desired value. Moreover, the harmonic distortion meets the requirements of the IEC6100-3-2 Class C harmonics standard, and hence the proposed circuit is suitable for the AC-DC LED driver.

Author Contributions: The conception was presented by K.-I.H., who also was responsible for editing this paper. Y.-K.T. surveyed the existing papers and wrote the software program. Y.-P.H. carried out experimental setup and verification. K.-I.H. was in charge of project administration.

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Conflicts of Interest: The authors declare no conflict of interest with commerce.

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