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Compact Model for L-Shaped Tunnel Field-Effect Transistor Including the 2D Region

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Abstract: The L-shaped tunneling field-effect transistor (LTFET) is the only line-tunneling type of TFET to be experimentally demonstrated. To date, there is no literature available on the compact model of LTFET. In this paper, a compact model of LTFET is presented. LTFET has both one-dimensional (1D) and 2D band-to-band tunneling (BTBT) components. The 2D BTBT part dominates in the subthreshold region, whereas the 1D BTBT dominates at higher gate-source biases. The model consists of 1D and 2D BTBT models. The 2D BTBT model is based on the assumption that the electric field originating from the gate and terminating at the source edge is perfectly circular. Tunneling path length is obtained by calculating the distance along an electric field arc that runs from gate to source. The 1D BTBT model is based on a simultaneous solution of the 1D Poisson equation in source and channel regions. Expressions for electric field and potential obtained from integrating the Poisson equation in source and channel regions are solved simultaneously to find the surface potential. Once the surface potential is known, all the other unknown variables, including junction potential and source depletion length, can be calculated. Using the potential profile, tunneling lengths were found for both the source-to-channel BTBT regime, and channel-to-channel BTBT regime. The tunneling lengths were used to calculate the BTBT tunneling rate, and finally, the drain-source current as a function of gate-source, and drain-source bias was calculated. The model results were compared against technology computer-aided design (TCAD) simulation results and were found to be in reasonable agreement for a compact model.

Keywords: band-to-band tunneling; L-shaped tunnel field-effect-transistor; 2D BTBT; corner-effect

1. Introduction

With the power requirements of complementary metal–oxide–semiconductor (CMOS) technology surging beyond unreasonable levels to meet the high computing demands of today's world, there has been a desperate push for devices that can perform better for less power [1]. The tunnel field-effect transistor (TFET) is one such device among the potential candidate devices [2]. TFET works on the principle of band-to-band-tunneling (BTBT) and achieves a steeper subthreshold slope (SS) than a metal–oxide–semiconductor field-effect transistor (MOSFET) of equivalent dimensions and electrical parameters.

However, the on-current (I_{ON}) of TFET is lower than that of MOSFET of equivalent dimensions/electrical parameters. To overcome this problem, different types of TFET architectures have been suggested, including the line-tunneling type [3] TFETs. The structure of line tunneling type TFETs has a gate-source overlap. This overlap increases the BTBT area and consequently increases the I_{ON}. The L-shaped TFET (LTFET) [4] is an example of a line-tunneling TFET that features the channel region grown vertically in the form of an L-shape. The LTFET offers the same benefits as a conventional

line-tunneling type TFET, but with a much lower device footprint. More significantly, LTFET is the only example of a line-tunneling TFET that has been experimentally realized.

Compact modeling is an important part of the circuit design process. While there are compact models available for the conventional TFET [5–7], the literature is almost completely lacking in compact models for the line-tunneling type TFETs. Vandenberghe et al. [3] developed a compact model for conventional line-tunneling TFET. Najam et al. [8] developed a compact model for LTFET. However, the line-tunneling TFET considered in [3] features a significant difference from the LTFET: The gate directly overlaps with the source region, as shown in Figure 1 in [3], whereas in the LTFET, there is a channel region present between the source and the gate. Direct overlapping of gate/source without any channel layer present in between completely changes the electrostatics of the device and makes the model presented in [3] inapplicable to LTFET. In [8], only the one-dimensional (1D) model is presented. In LTFET, both 1D and 2D BTBT components are present.

This paper presents a complete model of the LTFET, including both the 2D and 1D BTBT, which is presented in Section 2. The model presented is continuous from the subthreshold region to strong inversion. The model is tested for LTFETs with varying geometries, and the results are presented in Section 3. A conclusion is presented in Section 4.

2. Model Development

Figure 1 shows the schematic of the LTFET. The channel region shown in blue color is found in an L-shape and is sandwiched between the gate and the source. The part of the channel region found in between the source and gate regions is termed as C_{overlap} with height (H_{overlap}) = 40 nm and length (T_{j}) = 4 nm. The source and drain are p^+ ($N_{\text{a}} = 10^{20}$ cm^{-3}) and n^+ ($N_{\text{drain}} = 10^{20}$ cm^{-3}) doped, respectively, while the channel is lightly n^- doped ($N_{\text{d}} = 10^{15}$ cm^{-3}). The source region height (H_{s}) and length (L_{s}) are 40 and 50 nm, respectively. The bottom part of the channel, which is not in between the source and gate regions, is termed as $C_{\text{nonoverlap}}$ and has a height ($H_{\text{nonoverlap}}$) = 20 nm, and length ($L_{\text{nonoverlap}}$) = 50 nm. An HfO_2 dielectric of thickness (t_{ox}) = 2 nm for gate oxide was considered.

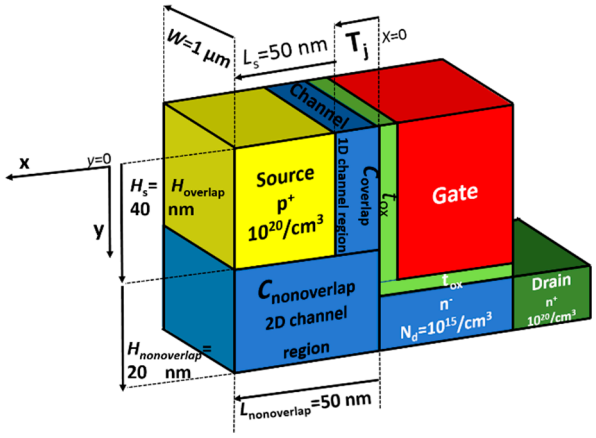

Figure 1. Schematic of the L-shaped tunneling field-effect transistor (LTFET).

Dynamic nonlocal BTBT model [9], fermi statistics, and constant mobility models were considered in the technology computer-aided design (TCAD) simulation.

As shown in Figure 1, the source has a sharp corner marked by an X in Figure 1. The electric field from the gate converges at and around this sharp source corner, increasing the potential around this point. The right axis in Figure 2a shows surface potential (φ_{s}) at V_{gs} = 0.15 V and V_{ds} = 0.5 V. As shown in Figure 2a, φ_{s} sharply rises in $C_{\text{nonoverlap}}$ because of convergence of the electric field, whereas φ_{s} is less in C_{overlap} where this convergence does not take place. This convergence affects the BTBT threshold voltage of C_{overlap} and $C_{\text{nonoverlap}}$. $C_{\text{nonoverlap}}$ is found to have a lower BTBT threshold voltage because of this increased φ_{s}. Meanwhile, C_{overlap} has a significantly higher BTBT threshold

voltage because of the lower potential [10]. This can be seen in Figure 2b, which shows integrated BTBT tunneling rates [10] (G_{tun}s) in x and y directions in $C_{overlap}$ and $C_{nonoverlap}$, respectively; that is, $\int_{L_s+T_j}^{0}\int_{0}^{H_{overlap}} G_{tun}dxdy$ in $C_{overlap}$ (black triangles) and $\int_{L_{nonoverlap}}^{0}\int_{H_{overlap}}^{H_{nonoverlap}} G_{tun}dxdy$ in $C_{nonoverlap}$ (red circles) in the left axis. Figure 2b clearly shows that $C_{nonoverlap}$ turns on earlier than $C_{overlap}$. The right axis in Figure 2b shows the drain-source current (I_{ds}) as a function of gate–source bias (V_{gs}) of LTFET. It is shown that in the subthreshold part of the I_{ds}–V_{gs} characteristics, only the $C_{nonoverlap}$ is active. $C_{overlap}$ turns on at V_{gs} = 0.15 V. When $C_{overlap}$ turns on, its G_{tun} is significantly higher because of 1D BTBT paths. As a result, it dominates the 2D G_{tun} in $C_{nonoverlap}$, as can be seen in Figure 2b. Based on this analysis, I_{ds}–V_{gs} characteristics of LTFET were modeled in two parts, first the 2D model in $C_{nonoverlap}$ for the subthreshold region and then the 1D model in $C_{overlap}$.

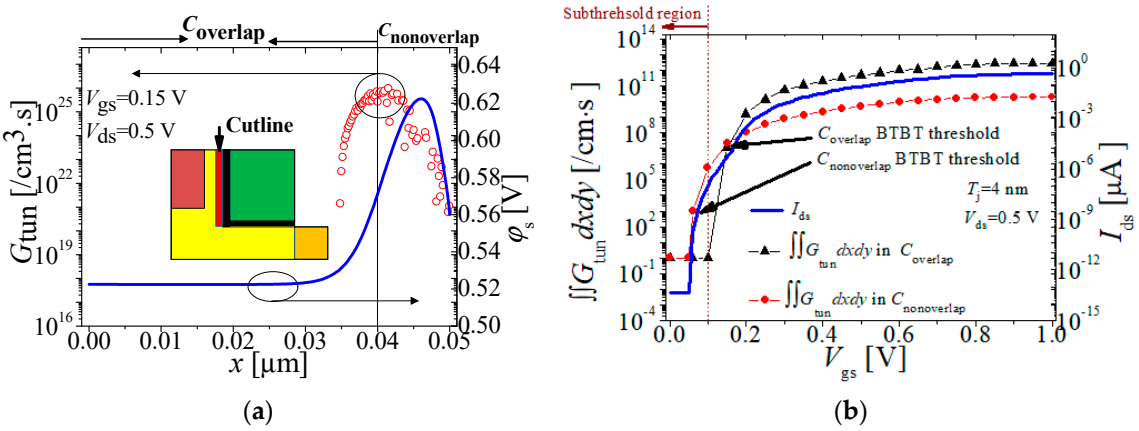

Figure 2. (**a**) G_{tun} along the surface of $C_{overlap}$ and $C_{nonoverlap}$ (left axis), and φ_s along the channel (right axis) at V_{gs} = 0.15 V and V_{ds} = 0.5 V. (**b**) Integrated band-to-band tunneling (BTBT) tunneling rates in $C_{overlap}$ (black triangles) and $C_{nonoverlap}$ (red circles) as a function of V_{gs} (left axis), and I_{ds}–V_{gs} characteristics of LTFET (right-axis). BTBT threshold voltages for $C_{overlap}$ and $C_{nonoverlap}$ are indicated by arrows.

2.1. 2D Model: $C_{nonoverlap}$ Model

The 2D model is based on the work in [3]. The following assumptions are used in this model: (1) Electric fields are assumed to be completely circular and terminate from gate to source. This helps in obtaining a convenient expression for the tunneling length (W_t); (2) Gate dielectric is treated as the same material as the channel with an equivalent dielectric thickness t'_{ox} given by $t'_{ox} = t_{ox}\varepsilon_{si}/\varepsilon_{ox}$, where t_{ox}, ε_{si}, and ε_{ox} are the physical dielectric thickness, silicon dielectric permittivity, and oxide dielectric permittivity, respectively. This is necessary to ensure a continuous and perfectly circular electric field from the gate-to-channel/gate dielectric interface, and finally terminate at the source. Without this assumption, the electric field will be discontinuous, that is, not perfectly circular in its path from gate to source. In this work, W_t is conveniently calculated as the length along the perfectly circular electric field arc, from gate to source, as will be shown below. If a discontinuity arises in the circularity of the electric field arc, such convenient calculation of W_t will not be possible; (3) The source is assumed to be completely depleted, and depletion length is ignored. The source is heavily doped. Depletion length is inversely proportional to doping concentration [3]. This makes the source depletion length negligible. Including the source depletion length would add complexity to the model without significantly increasing the accuracy of the model; (4) The source is assumed to be touching the gate. Table 1 mentions most of the symbols used in the equations below.

With these assumptions, the boundary conditions at source and gate can be given by

$$\varphi(x,0) = \varphi_{source} \quad \text{and} \quad \varphi(0,y) = \varphi_g. \tag{1}$$

where φ_{source} is assumed to be 0 V and φ_g is the gate–source bias minus the flat band voltage (V_{fb}), that is, $\varphi_g = V_{gs} - V_{fb}$. The solution of potential in polar co-ordinates is given by

$$\varphi(x, y) = \frac{2\theta\varphi_g}{\pi}, \qquad 0 \le \theta \le \frac{\pi}{2}. \tag{2}$$

The above boundary condition along with θ_0 is shown in Figure 3a. Thanks to assumptions 1 and 2, W_t is calculated as the length along a perfectly circular electric field line as follows:

$$W_t = r_0\theta_0 \tag{3}$$

where θ_0 is given by $\theta_0 = \pi E_g/(2q\varphi_g)$, (where E_g is the bandgap, and q is the charge on an electron) and is the angle when the potential difference between the source edge and some point along the electric field line becomes equal to E_g/q. θ_0 is obtained by substituting the BTBT condition, that is, $\varphi = E_g/q$ in (2), and inverting it. Since θ_0 is bias-dependent, θ_0 decreases, and W_t decreases as V_{gs} bias increases. This is illustrated in Figure 3b. r_0 is the radius of the electric field arc and is given by $r_0 = t'_{ox}/cos\ (\theta_0)$. Drain current expression in $C_{nonoverlap}$ ($I_{ds\_Cnonoverlap}$) is given by the following equation for D = 2.5 [3]:

$$I_{ds\_Cnonoverlap} = \frac{qWA_kE_gt'_{ox}}{q^{4.5}B_k^2} \cdot \frac{1}{\theta_0^{4.5}r_0^{3.5}} \cdot \exp\left(-qB_kr_0\theta_0\sqrt{E_g}\right), \tag{4}$$

where W (=10^{-4} cm) is the device width, and $A_k = 1 \times 10^{15}$ $eV^{0.5}{\cdot}cm^{-1/2}{\cdot}s^{-1}{\cdot}V^{-2.5}$ and $B_k = 1.5 \times 10^7$ $V{\cdot}cm^{-1}{\cdot}eV^{-1.5}$ are the parameters used in the dynamic nonlocal BTBT model. There is one notable difference between this work and [3] which is that, as $C_{overlap}$ turns on, $I_{ds\_Cnonoverlap}$ is assumed to saturate. This is in line with the results presented in Figure 2b. Once $C_{overlap}$ turns on, it dominates, and $C_{nonoverlap}$ does not have any significant contribution beyond that point. Without this assumption, the model overestimates $I_{ds\_Cnonoverlap}$ in the high V_{gs} region.

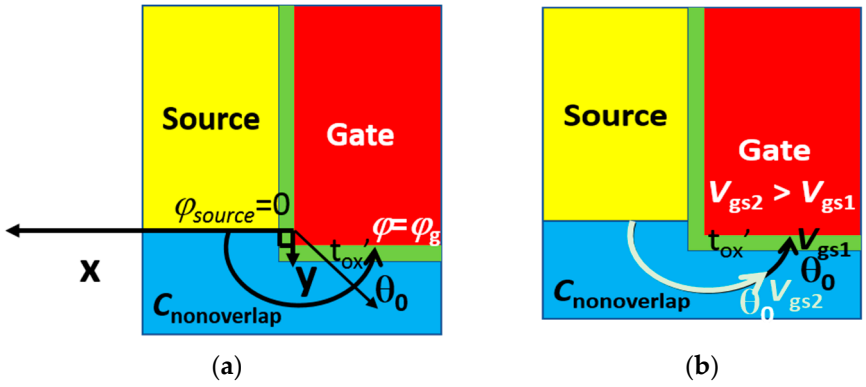

Figure 3. (**a**) Schematic illustrating the boundary conditions and the assumptions used in the model. (**b**) Schematic showing θ_0 at a lower V_{gs} bias, V_{gs1} (black), and at a higher V_{gs} bias, V_{gs2} (white).

Table 1. List of all the symbols specific to the two-dimensional (2D) model.

Symbol	Description	Value/Unit
φ_{source}	Potential at source edge	V
φ_g	Potential at gate	V
t_{ox}	Physical oxide thickness	2×10^{-7} cm
t'_{ox}	Equivalent semiconductor thickness	cm
ε_{si}, ε_{ox}	Silicon, oxide permittivity	11.9, 25 F/cm
θ_0	Angle when the BTBT condition is satisfied	Radian
r_0	Radius of an electric field arc	cm/radian

2.2. 1D Model: $C_{overlap}$ Model

Figure 4a shows a magnified $C_{overlap}$ and source regions. The channel region considered in the 1D model comprises the $C_{overlap}$ region. Figure 4a mentions the important parameters used in the 1D model, including the location of φ_s and junction potential (φ_j). φ_j is the potential at the junction of the source and channel region in Figure 4a. The device origin is at the top of the channel/gate dielectric interface, and $x_{channel}$ and x_{source} correspond to the x-coordinate in channel and source regions, respectively. The dimension for the 1D model is along the x-direction, as shown by the cutline shown in Figure 4b. The cutline begins at the channel/gate dielectric interface and ends in the source region. Figures 5d–f and 6a,b are along the black cutline shown in Figure 4b.

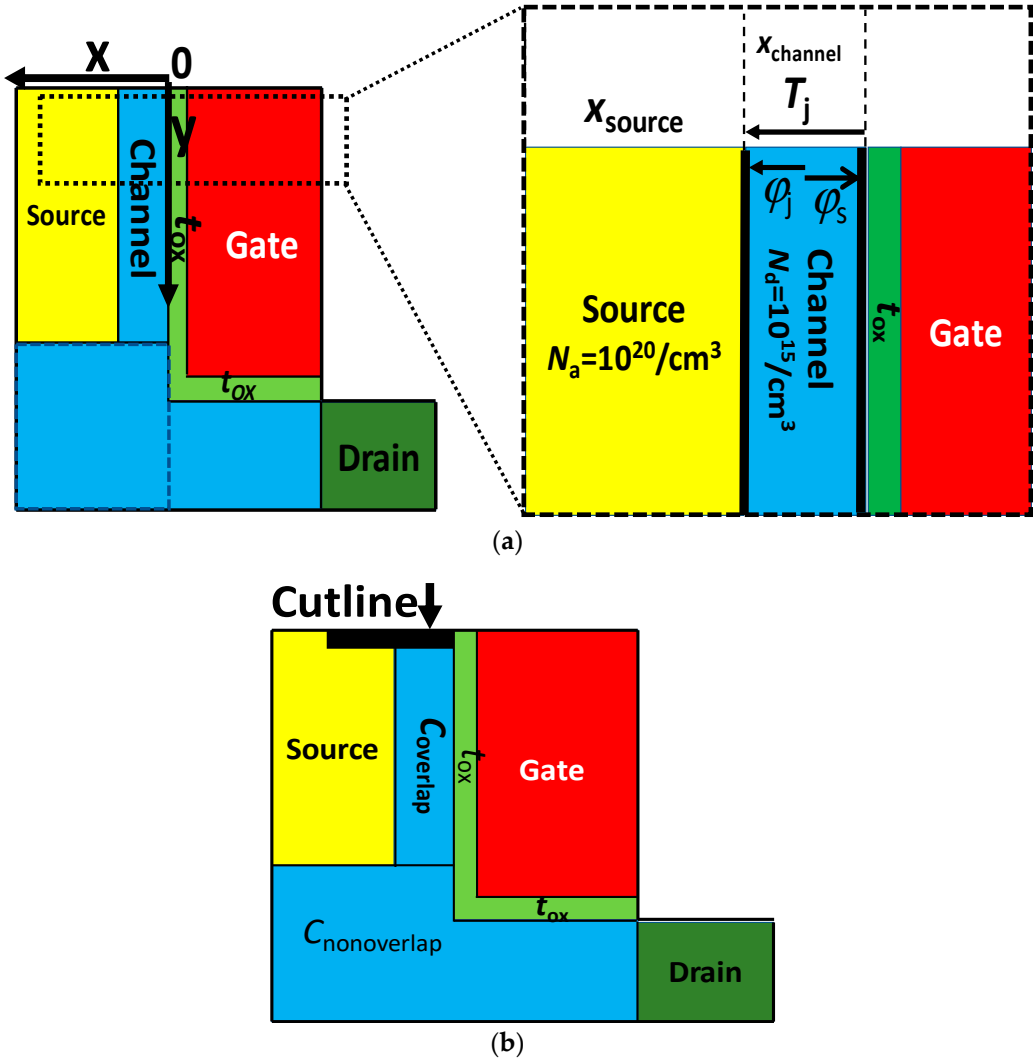

Figure 4. (**a**) Magnified part of $C_{overlap}$ and source regions of the LTFET to illustrate parameters used in the 1D model. Device origin is at the dielectric/channel interface. x and y are in the horizontal and vertical directions, respectively. (**b**) Only a single y-point is considered in the 1D model, illustrated by the cutline. Figures 5d–f and 6a,b to follow are along the same cutline with x = 0 nm at the channel–dielectric interface.

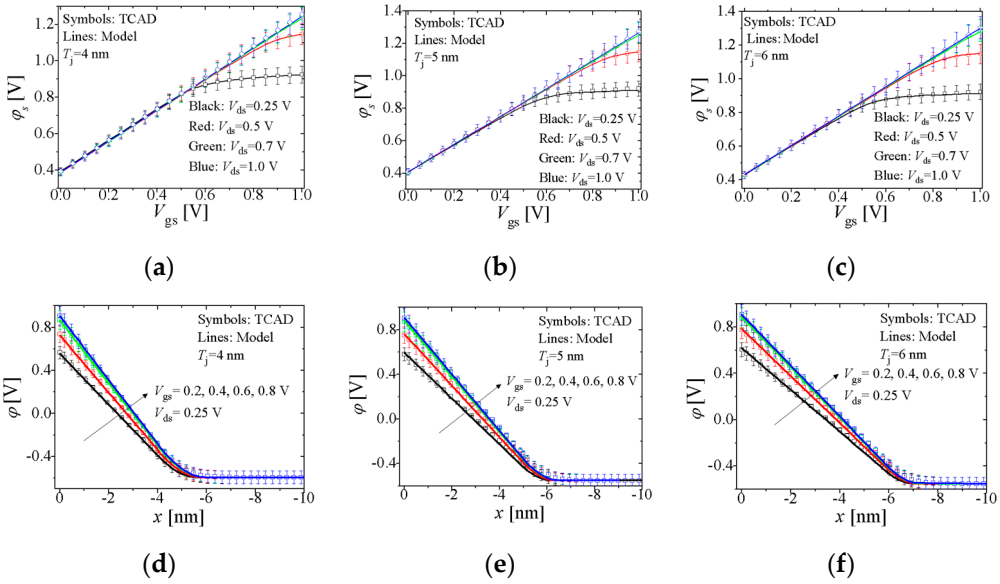

Figure 5. (**a**–**c**) φ_s as a function of V_{gs}, for T_j = 4, 5, and 6 nm, respectively, at V_{ds} = 0.25 (black), 0.5 (red), 0.7 (green) nm, and 1 V (blue). Error bar: 5%. (**d**–**f**) potential profile in channel, and source regions, for T_j = 4, 5, and 6 nm, respectively, at V_{gs} = 0.2 (black), 0.4 (red), 0.6 (green), and 0.8 V (blue) at V_{ds} = 0.25 V. Error bar: 10%. Lines: Potential model. Symbols: technology computer-aided design (TCAD). Figure 5d–f is along the cutline of Figure 4b.

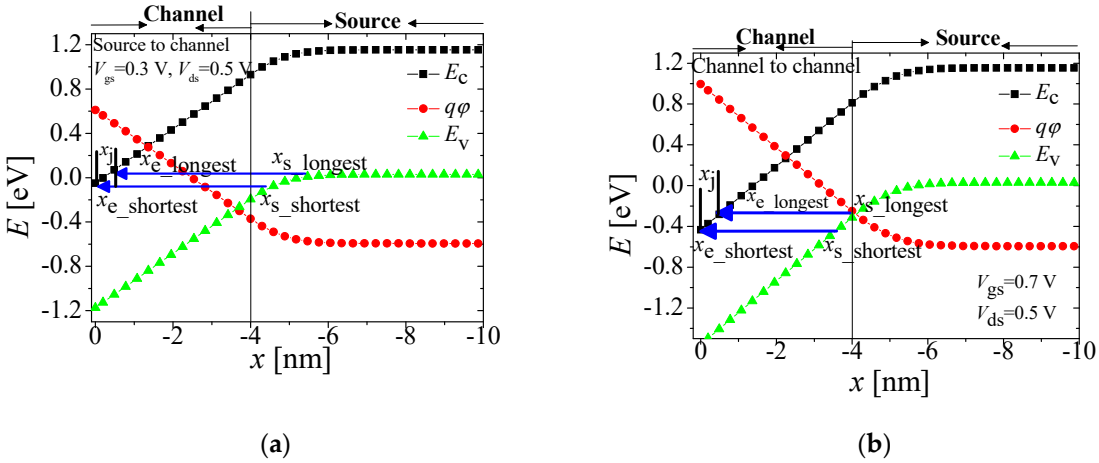

Figure 6. (**a**,**b**) Band diagram at V_{gs} = 0.3 and 0.7 V, respectively, and both at V_{ds} = 0.5 V, along the cutline of Figure 4. Black squares, green triangles, and red circles represent E_c, E_v, and $q\varphi$. respectively. Source-to-channel (**a**) and channel-to-channel (**b**) BTBT mechanisms are indicated with the help of arrows.

The 1D model is based on the solution of the 1D Poisson equation. Integrating the 1D Poisson equation once, in source and channel regions, and neglecting electron and hole carrier concentrations yields the electric field in the respective regions, which are given by

$$\frac{\partial \varphi_{source}}{\partial x_{source}} = \frac{qN_a}{\varepsilon_{si}} x_{source} + \frac{qN_a}{\varepsilon_{si}} \left(L_{dep} \right), \tag{5}$$

$$\frac{\partial \varphi_{channel}}{\partial x_{channel}} = \frac{qN_d}{\varepsilon_{si}} x_{channel} + \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}} \left(V_{gs} - V_{fb} - \varphi_s \right), \tag{6}$$

where L_{dep} is the depletion length of the source region. Integrating (5) and (6) again yields potential in source and channel regions, which is given by

$$\varphi_{source}(x_{source}) = \frac{qN_a}{2\varepsilon_{si}}\left(x_{source} + L_{dep}\right)^2 + \varphi_{dep} \tag{7}$$

$$\varphi_{channel}(x_{channel}) = \frac{qN_d}{2\varepsilon_{si}}x_{channel}^2 + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\left(V_{gs} - V_{fb} - \varphi_s\right)x_{channel} + \varphi_s \tag{8}$$

$$\varphi_s = V_{gs} - V_{fb} + \frac{q(N_a+N_d)}{C_{ox}}T_j + \frac{q\varepsilon_{si}N_a}{C_{ox}^2} - \gamma\sqrt{V_{gs} - V_{fb} + \frac{q(N_a+N_d)}{2\varepsilon_{si}}T_j^2 + \frac{q(N_a+N_d)}{C_{ox}}T_j + \frac{q\varepsilon_{si}N_a}{2C_{ox}^2} - \varphi_{dep}} \tag{9}$$

where C_{ox} is the gate oxide capacitance, φ_{dep} is the source depletion potential, and $\gamma = (2\varepsilon_{si}qN_a)^{1/2}/C_{ox}$. With the potential profile known, W_t can be calculated. Because (9) is derived from the depletion approximation, the smoothing function from [11–13] was used to model strong inversion of the electron.

There are two different 1D BTBT mechanisms present in LTFET [8]. One is the source-to-channel BTBT, which starts at low bias, and the other is the channel-to-channel BTBT, which takes place at high V_{gs} bias. The first source to channel the 1D BTBT model is discussed.

The potential profile within the channel is assumed to be linear, as seen in Figure 5d–f, which is given by

$$\varphi_{channel}(x_{channel}) = mx_{channel} + \varphi_s \tag{10}$$

where m is the slope of the linear potential profile in the channel, $m = (\varphi_s - \varphi_j)/T_j$. φ_j can be found from (8) by using $x_{channel} = T_j$. Figure 5a–c shows φ_s as a function of V_{gs} of LTFET with T_j = 4, 5, and 6 nm at different V_{ds} biases, respectively. Figure 5d–f shows the potential profile along the cutline shown in Figure 4b for LTFET with T_j = 4, 5, and 6 nm at different V_{gs} and V_{ds} = 0.25 V, respectively. Symbols and lines denote the simulation results of TCAD and the proposed potential model, respectively. Reasonable agreement is observed within a maximum error of 10% between the model and TCAD simulations.

Figure 6a shows a band diagram at V_{gs} = 0.3 V and V_{ds} = 0.5 V, along the cutline of Figure 4b. Black and green symbols represent conduction band minimum energy (E_c) and valence band maximum energy (E_v), respectively. Red circles represent potential. Arrows denote W_ts. The longest W_t ($W_{t\_longest}$) originates where $\varphi_{source} = \varphi_{dep}$, and the shortest W_t ($W_{t\_shortest}$) originates from where the potential is the highest, that is, φ_s. The starting and ending points for $W_{t\_shortest}$ are $x_{s\_shortest}$ and $x_{e\_shortest}$, respectively, and the starting and ending points for $W_{t\_longest}$ are $x_{s\_longest}$ and $x_{e\_longest}$, respectively, which are all indicated by arrows in Figure 6a. $x_{s\_longest}$ naturally starts from L_{dep}, that is, $x_{s\_longest} = -abs(L_{dep} + T_j)$, and the ending point for the $W_{t\_shortest}$ is the surface, that is, $x_{e\_shortest} = 0$. $x_{e\_longest}$ is the point where the BTBT condition for $W_{t\_longest}$, that is, $\varphi(x_{e\_longest}) = \varphi_{dep} + E_g/q$, is satisfied. By substituting this BTBT condition in (10) and inverting it, $x_{e\_longest}$ is given by $x_{e\_longest} = (\varphi_{dep} + E_g/q - \varphi_s)T_j/(\varphi_s - \varphi_j)$. $x_{s\_shortest}$ is the point where the BTBT condition for $W_{t\_shortest}$, that is, $\varphi(x_{s\_shortest}) = \varphi_s - E_g/q$, is satisfied. By substituting this BTBT condition in (7) and inverting it, $x_{s\_shortest}$ is given by

$$x_{s\_shortest} = \sqrt{\varphi_{dep} + \varphi_s - \frac{E_g}{q}\left(\frac{2\varepsilon_{si}}{qN_a}\right)} - abs\left(L_{dep} + T_j\right) \tag{11}$$

Finally, $W_{t\_shortest}$ and $W_{t\_longest}$ are given by

$$W_{t\_shortest} = x_{e\_shortest} - x_{s\_shortest} \tag{12a}$$

$$W_{t\_longest} = x_{e\_longest} - x_{s\_longest} \tag{12b}$$

G_{tun} is given by Kane's model [14]

$$G_{tun} = \frac{A_k}{\sqrt{E_g}}\left(\frac{E_g}{qW_t}\right)^{2.5} \exp\left(-qB_k W_t \sqrt{E_g}\right). \quad (13)$$

I_{ds} for source-to-channel BTBT ($I_{ds\_s\_c}$) is given by

$$I_{ds\_s\_c} = qW \int_0^{H_s} \int_0^{x_j} G_{tun}(x) dy dx = qWH_s x_j \left(\frac{G_{tun\_shortest} + G_{tun\_longest}}{2}\right) \quad (14)$$

where x_j is the integration limit indicated in Figure 6a, and is equal to $x_j = x_{e\_shortest} - x_{e\_longest}$. In (14), a constant average G_{tun}, that is, $\frac{G_{tun\_shortest}+G_{tun\_longest}}{2}$, is used. Here, $G_{tun\_shortest}$ and $G_{tun\_longest}$ are found by using $W_t = W_{t\_shortest}$ and $W_{t\_longest}$ in (13), respectively. G_{tun} is a function of W_t, as can be inferred from (13). The integral in (14), however, is with respect to x. Finding a closed-form expression for $I_{ds\_s\_c}$ then necessitates expressing W_t as a function of x. However, because W_t cannot be expressed as a function of x, W_t can only be found for fixed BTBT boundary conditions, as done in (12a, b). In this scenario, dW_t/dx cannot be evaluated. As a result, there is no closed-form expression available for G_{tun} integrated as a function of x. Therefore, the simplification of using average G_{tun} was necessary and, as it will be shown in Section 3, the average G_{tun} approximates the integral of G_{tun} with respect to x reasonably well. When the bias is high enough, the potential increases so much that BTBT becomes possible from even inside the channel. This is illustrated by the band diagram shown in Figure 6b along the cutline of Figure 4b. Here, E_v/E_c becomes aligned within the channel, as illustrated by the arrows, in addition to the source/channel E_v/E_c alignment. Here, $W_{t\_longest}$ starts from $x_{s\_longest} = T_j$ and ends at $x_{e\_longest}$, where the BTBT condition, $\varphi(x_{e\_longest}) = \varphi_j + E_g/q$, is satisfied. Similarly, $W_{t\_shortest}$ starts at $x_{s\_shortest}$, where the BTBT condition, $\varphi(x_{s\_shortest}) = \varphi_s - E_g/q$, is satisfied and ends at $x_{e\_shortest} = 0$. By substituting these boundary conditions in (10) and inverting it, $x_{e\_longest}$ and $x_{s\_shortest}$ can be calculated as $x_{e\_longest} = (\varphi_j + E_g/q - \varphi_s)T_j/(\varphi_s - \varphi_j)$ and $x_{s\_shortest} = -E_g T_j/(q(\varphi_s - \varphi_j))$. As can be seen in Figure 6b, W_t is almost constant within the channel. Therefore, in the channel-to-channel regime, $G_{tun\_shortest} \approx G_{tun}(W_{t\_longest}) \approx G_{tun}(W_{t\_shortest})$. This means that $G_{tun}(x)$ can be taken out of the integral in the channel-to-channel drain current ($I_{ds\_c\_c}$) expression, which is given by

$$I_{ds\_c\_c} = qWH_s x_j G_{tun} \approx qWH_s x_{e\_longest} G_{tun\_shortest} \quad (15)$$

The total I_{ds} is given by

$$I_{ds} = I_{ds\_Cnonoverlap} + I_{ds\_s\_c} + I_{ds\_c\_c} \quad (16)$$

3. Results

Figure 7a–c shows I_{ds}–V_{gs} characteristics of LTFET with T_j = 4, 5, and 6 nm, respectively. Symbols and lines denote the simulation results of TCAD and the proposed model, respectively. Blue, red, and black colors denote V_{ds} = 0.25, 0.5, and 0.7 V, respectively. A kink is observed in Figure 7a–c, at the transition point where the 1D model takes over the 2D model. This is observed because the 1D and 2D models are independent of each other and don't produce the same and continuous G_{tun} at the transition point.

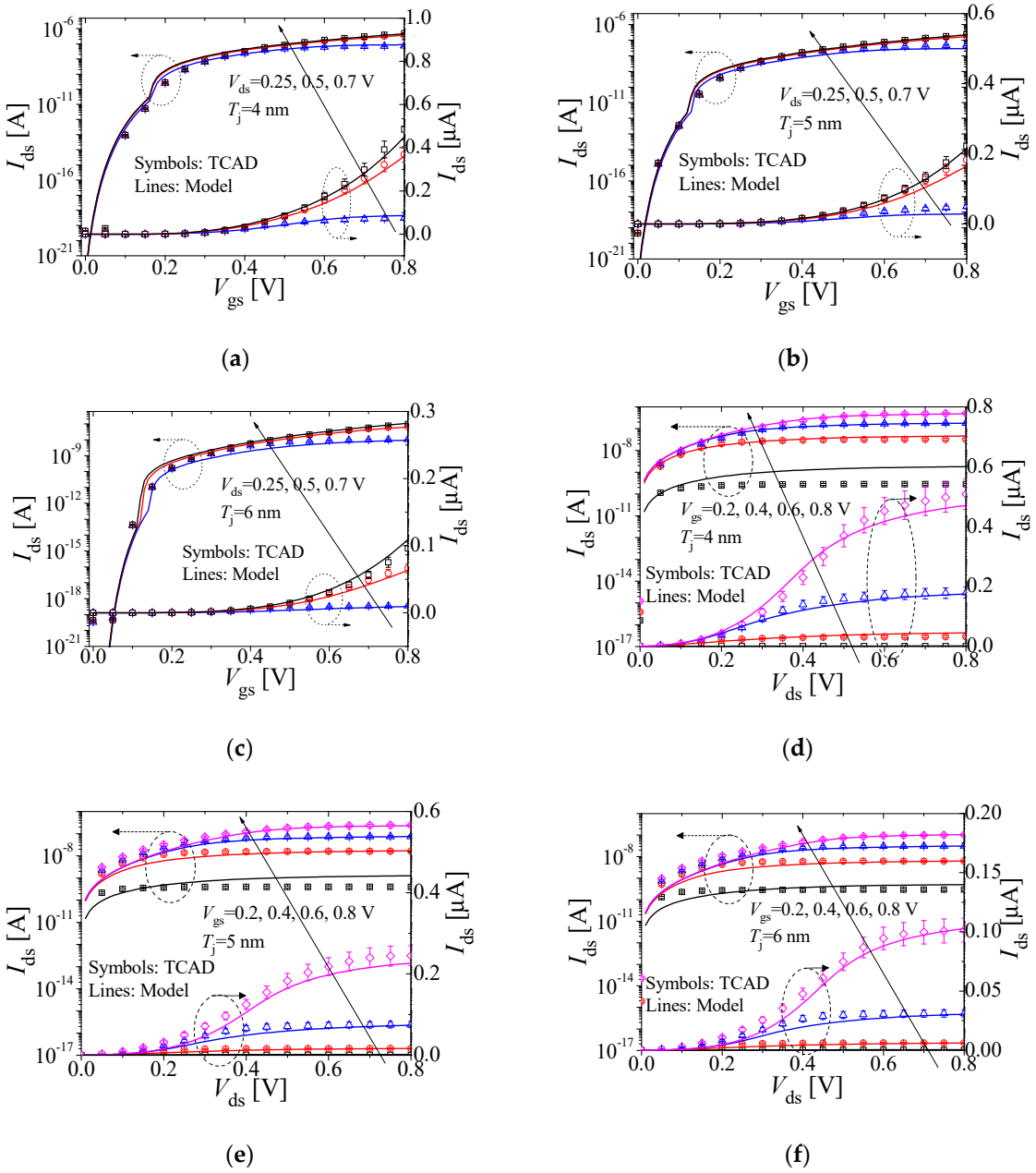

Figure 7. (**a**–**c**) I_{ds}–V_{gs} characteristics of LTFET with T_j = 4, 5, and 6 nm, respectively, at V_{ds} = 0.25 (blue), 0.5 (red), and 0.7 V (black). (**d**–**f**) I_{ds}–V_{ds} characteristics of LTFET with T_j = 4, 5, and 6 nm, respectively, at V_{gs} = 0.2 (black), 0.4 (red), 0.6 (blue), and 0.8 V (magenta). Error bar: 10%. Lines: Model. Symbols: TCAD.

There is no noticeable change observed in the subthreshold behavior as T_j is changed from 4 nm to 6 nm. However, the on-current (I_{ON}) is observed to decrease as T_j is increased. I_{ON} at V_{gs} = 0.8 V and V_{ds} = 0.7 V is 0.48, 0.22, and 0.09 μA for T_j = 4, 5, and 6 nm, respectively. This is because W_t and G_{tun} are inversely proportional, as can be observed from (13); the longer W_t in T_j = 5 and 6 nm results in lower G_{tun}, and consequently, lower I_{ds}. This effect is captured by the model reasonably well. This suggests that shorter T_j is more desirable for getting higher I_{ON}.

Figure 7d–f shows I_{ds}–V_{ds} characteristics of the LTFET for T_j = 4, 5, and 6 nm, respectively. Symbols denote TCAD simulation results, and lines denote model results. Black, red, blue, and magenta denote V_{gs} = 0.2, 0.4, 0.6, and 0.8 V, respectively. As shown in Figure 7d–f, the saturation characteristics of the LTFET are predicted reasonably well by the model.

Figure 8 shows I_{ds}–V_{gs} characteristics of LTFET with T_j = 4 nm and $H_{overlap}$ = H_s varied at V_{ds} = 0.5 V. Symbols denote TCAD simulation results and lines denote model results. Blue, red, and black represent $H_{overlap}$ = 40, 50, and 60 nm, respectively. It is shown in Figure 8 that, as $H_{overlap}$ = H_s is increased, the I_{ds} increases. This is because, with an increase in $H_{overlap}$, the BTBT area increases. This results in an increase in I_{ds}. Once again, the model captures this effect reasonably well.

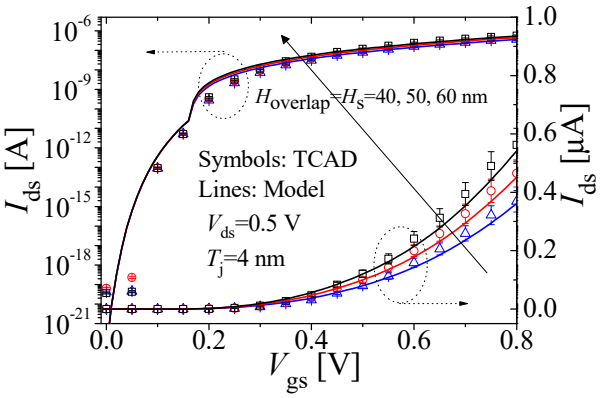

Figure 8. I_{ds}–V_{gs} characteristics of LTFET with T_j = 4 nm, $H_{overlap}$ varied, and V_{ds} = 0.5 V. Blue, red, and black represent $H_{overlap}$ = H_s = 40, 50, and 60 nm, respectively. Symbols and lines denote TCAD simulation and model results, respectively. Error bar: 10%.

Compared to the planar TFET, the LTFET offers better SS and I_{ON} performance. This can be gauged from the fact that while in planar TFET, the dominant BTBT generation area comprises the surface source/channel depletion regions. In the LTFET, however, because of the gate–source overlap, this area is significantly amplified by the height of the source and $C_{overlap}$ regions. Furthermore, because of this overlap, the electrostatic coupling between gate and source is stronger in LTFET. In other words, the electric field is stronger in the LTFET as compared to the planar TFET, which also results in higher I_{ON} and lower inverse subthreshold slope in LTFET, as was demonstrated even in the case of the experimental LTFET and planar TFET in [4].

For a compact model, the simulation results of the model agree reasonably well with those of TCAD within a maximum error of 10%. However, it is not entirely accurate. The inaccuracy results from the simplified integral expression in (14). Numerical integration of G_{tun} with respect to x will significantly improve the result. Another source of error is the use of the smoothing function to model electron inversion. The smoothing function only approximates surface potential saturation due to electron inversion, and is thus not very accurate at high bias. Considering the electron concentration term in the Poisson equation and doing a self-consistent solution for potential and electron concentration will also improve the model accuracy significantly. However, both numerical integration and self-consistent potential electron concentration solution will significantly add to the computational complexity of the model. This will make the model unsuitable for SPICE applications.

It should also be mentioned that the model was bench-marked only against TCAD data and not experimental data. This is because the experimental LTFET demonstrated significant trap-assisted tunneling (TAT), and Shockley–Read–Hall (SRH) generation–recombination current- and ambipolar current-induced degradation of the I_{ds}–V_{gs} characteristics [4]. In particular, TAT in line TFETs is a significant topic and requires its own modeling framework [9]. This work with the equations for surface and junction potentials lays the foundation for the TAT model. However, due to space constraints, TAT, SRH, ambipolar, quantum confinement [15], and breakdown models [16] could not be included in this manuscript.

4. Conclusions

A compact model for LTFET was presented. The model calculates both the 1D BTBT and 2D BTBT present in LTFET. The 1D model is based on the simultaneous solution of 1D Poisson equations in the channel and source region. The Poisson equation is integrated twice in both regions, and the expression for electric field and potential are equated at the source–channel junction point to yield expression for surface potential. To model electron inversion, a simple smoothing function was used. After obtaining the potential profile, starting and ending points of tunneling paths were determined using BTBT boundary conditions. The shortest tunneling path was considered in the drain current expression for source-to-channel BTBT. This was done to obtain a simplified expression for the source-to-channel drain current. Tunneling path lengths were similarly determined for the channel-to-channel BTBT regime. The model was compared against I_{ds}–V_{gs}/V_{ds} results obtained from the simulator for different V_{ds}/V_{gs} biases, and for different channel region thicknesses, and heights. The results of the compact model are in reasonable agreement with the simulator results.

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