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Spin Qubits Confined to a Silicon Nano-Ridge

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Featured Application: The proposed multi-qubit device generates a single- and double-array of tunnel-coupled quantum dots, respectively, each filled with a single electron spin. Each electron spin defines one qubit. Such devices can be applied to define a quantum-error-corrected logical qubit. Another application is a single electron conveyor, which shuttles a single electron spin coherently over a distance of 1–10 microns. Such conveyors are required for mid-range coherent links in future quantum computing architectures.

Abstract: Electrostatically-defined quantum dots (QDs) in silicon are an attractive platform for quantum computation. Localized single electron spins define qubits and provide excellent manipulation and read-out fidelities. We propose a scalable silicon-based qubit device that can be fabricated by industry-compatible processes. The device consists of a dense array of QDs localized along an etched silicon nano-ridge. Due to its lateral confinement, a simple dense array of metallic top-gates forms an array of QDs with controllable tunnel-couplings. To avoid potential fluctuations because of roughness and charged defects at the nano-ridge sidewall, the cross-section of the nano-ridge is trapezoidal and bounded by atomically-flat {111} facets. In addition to side-gates on top of the low-defect oxidized {111} facets, we implement a global back-gate facilitated by the use of silicon-on-insulator. The most relevant process modules are demonstrated experimentally including anisotropic wet-etching and local oxidation of the silicon nano-ridge, side-gate formation with chemical-mechanical polishing, and top-gate fabrication employing the spacer process. According to electrostatic simulations, our device concept allows forming capacitively-coupled QD double-arrays or adjacent charge detectors for spin-readout. Defining a logical qubit or realizing a single electron conveyor for mid-range qubit-coupling will be future applications.

Keywords: electron spin qubit; silicon nano-ridge; TMAH-etching; MOS structure; interface defects; self-aligned spacer process; device simulation

1. Introduction

A single electron spin confined in a quantum dot (QD) can be used to define a quantum bit (qubit) [1]. For the realization of a large-scale quantum computer, silicon turned out to be a promising material [2]. Silicon qubits stand out by their extremely long coherence times, compatibility with reliable and reproducible industrial fabrication techniques, and the feasibility to integrate classical electronics [3]. The basic building blocks for a quantum computer, i.e., qubit initialization and read-out, as well as single- and two-qubit gates have been demonstrated. Observed single-qubit fidelities higher than 99.9% [4–7] are beyond the quantum error correction threshold of the surface code [8], and the fidelity of two-qubit gates is steadily increasing [7,9,10]. Isotopically-purified ^{28}Si [11,12]

rendered this progress possible, as qubit dephasing by randomly-fluctuating nuclear spins is largely suppressed [6,13].

Since quantum error correction comes at the cost of requiring on the order of 1000 physical qubits to represent one logical qubit, reliable and reproducible manufacturing of individual qubits becomes mandatory to enable an up-scaling of the number of physical qubits in a multi-qubit device [3,14]. Furthermore, the potential landscape setting the charge state and the tunnel barriers has to be homogeneous and well controllable by the voltages applied to metallic gates across the entire multi-qubit device [15]. Limiting factors include fabrication inaccuracy and most significantly potential disorder due to charged defects near the confined electron spin.

Several approaches for forming QDs in silicon are being pursued by various research groups that exhibit different strengths and weaknesses [16]. The first types of devices are planar and confine electrons either in a strained undoped Si/SiGe quantum well [6,10,17] or at the Si/SiO_2 interface [13] along the out-of-plane direction. However, the lateral two-dimensional QD confinement requires elaborated multi-layer metallic gate stacks [17,18], the fabrication of which is involved. The valley splitting of the strained Si/SiGe heterostructure is typically low and limits qubit coherence and operation temperature [18–20]. Progress in the growth of the Si/SiGe stack will lead to enhanced valley splittings [21]. The second type, planar metal-oxide-semiconductor (MOS) devices, exhibits conveniently large valley splittings of up to 1 meV [22], but potential disorder and strain due to the close vicinity of the oxide interface and the metal layers, respectively, are very challenging [23]. An alternative to these planar devices is modified fin field-effect transistor (FinFET) structures [12,24,25]. For the latter, a one-dimensional silicon channel etched from a silicon-on-insulator substrate sets the confinement in two dimensions. Hence, the complexity of the metal top-gates is reduced. These modified FinFET structures are compatible with industrial foundries and have been fabricated on 300-mm wafers. Hole spins and electron spins have been confined, and Pauli spin blockade was observed in double-quantum wells [26]. Electron spin resonance triggered by microwaves applied to the gates mediated via spin-orbit interaction was observed [27,28]. However, all realized devices based on FinFET transistors are limited to four QDs in a cross-shaped structure [29] so far, as the technology is highly demanding. Moreover, compared to planar devices, the potential disorder due to the mesa channel is enhanced, and it has to be seen whether this will set a fundamental limit for this device species.

Here, we present a novel silicon nano-ridge qubit device concept that allows circumventing the issues related to fluctuating confining potentials mentioned above. We discuss the versatility of the device design by electrostatic simulations, in which we employ the multiple degrees of freedom arising from the various independently voltage-tunable gates, as well as some flexibility in the modification of the nano-ridge tip. Furthermore, the technology modules required to realize our new device design will be presented. We demonstrate the fabrication of the silicon nano-ridge and analyze the atomic flatness of the etched {111} facets and the charged defect density in the vicinity of the Si/SiO_2 {111} interface. Furthermore, we present the SiO_2 spacer process required for the fabrication of the top-gate array. We expect reduced potential disorder compared to state-of-the-art modified FinFETs because of the wet-chemically-etched, atomically-flat nano-ridge sidewalls. This might overcome one of the main current challenges arising from the need for single electron control.

2. Silicon Nano-Ridge Qubit Device

2.1. Device Concept

We invented a new silicon qubit device design consisting of a linear array of electrostatically-defined and tunnel-coupled QDs with source and drain reservoirs at both of its ends as shown in Figure 1. It is based on a one-dimensional silicon channel on top of a fully-depleted silicon-on-insulator wafer and exhibits a back-gate, two TiN side-gates, and an array of thin TiN top-gates. In contrast to the modified FinFET devices of [24,25,27], the channel is anisotropically

wet-etched by tetramethylammonium hydroxide (TMAH), which results in a trapezoidal nano-ridge with atomically-flat {111} facets [30,31]. The angle of the tip of the trapezoidal nano-ridge can be further tuned by the local-oxidation of silicon (LOCOS) process of the {111} silicon facets. Two TiN side-gates insulated by SiO_2 cover the two sidewalls of the silicon nano-ridge and control the perpendicular QD confinement of the nano-ridge. As the nano-ridge sidewalls are atomically flat, the disorder impact from side-gates or interface defects is low. The side-gates are realized by covering the nano-ridge with TiN and subsequent chemical mechanical polishing. This provides electrical insulation of the two side-gates, yielding a highly-tunable QD potential. In addition, the planarized sample surface is indispensable for the fabrication of multiple top-gate electrodes with spacer and damascene processes. For the top-gate array, we target a gate pitch of 45 nm (metal gate width of 30 nm and 15 nm of SiO_2 insulation). The gates are used alternatingly to accumulate QDs and tunnel barriers by applying voltages $V_{P,n}$ and $V_{B,n}$, respectively. Thus, an arbitrarily-long array of QDs can be formed, where each QD can be filled with a single electron, the spin of which encodes one qubit (Figure 1). Such linear arrays of tunnel-coupled QDs are suitable for quantum error correction [32]. At both ends of the silicon nano-ridge, two large top-gates accumulate two-dimensional source and drain reservoirs (Figure 1).

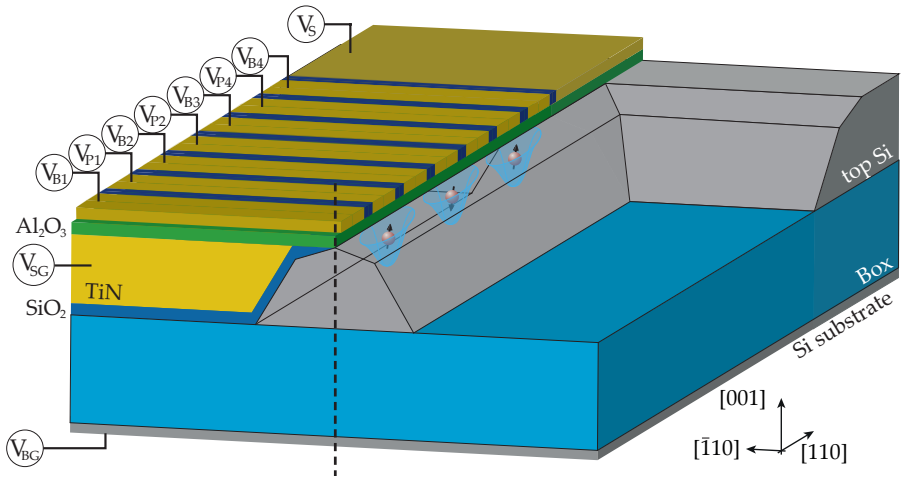

Figure 1. Schematic of the envisioned qubit device showing the silicon nano-ridge and the TiN gate array for electron spin localization. The trapezoidal silicon nano-ridge is fabricated on a fully-depleted silicon-on-insulator (FDSOI) substrate, providing a global back-gate set on voltage V_{BG} underneath the buried oxide (Box). Buried TiN side-gates are used to tune the confinement of the electron wave function along the [$\bar{1}$10] crystal axis. TiN gates, perpendicular to the silicon nano-ridge, tune the chemical potential within each quantum dot by applying a voltage $V_{P,n}$ and the potential barrier between adjacent quantum dots by applying a voltage $V_{B,n}$. Two electronic reservoirs, each tunnel-coupled to one end of the nano-ridge, are induced by applying a positive voltage to large top-gates covering the area adjacent to the ends of the nano-ridge (here, V_S for the source reservoir is shown). The dashed line indicates a symmetry axis with respect to the gate structure. Note that the side-gate and top-gate pattern on the right-hand side of the device, as well as the drain reservoir at the front end of the nano-ridge are not shown.

Applying voltages to the various independently-tunable top-, side-, and back-gates allow for a flexible control of the potential landscape. For instance, the valley splitting of the QD and the tunnel-coupling of adjacent QDs can be tuned by applying suitable voltages at the various gates [22,33]. Moreover, using a split top-gate array, we can also form two capacitively- or tunnel-coupled arrays of QDs (i.e., double-array) in each corner of the nano-ridge. Alternatively, an array of QDs is formed on one side of the silicon nano-ridge, while on the other side, a single electron transistor (SET) biased by V_{SD} applied across the source and drain reservoirs is formed. The SET can be operated as a charge detector for the whole QD array, since its QD is capacitively coupled to a few QDs of the opposing array. Furthermore, the SET can be formed at an arbitrary position along the nano-ridge. Such a charge

detector in combination with spin-to-charge conversion is sufficient for spin qubit initialization and read-out [17,34]. For the double-array of QDs, spin-readout can be achieved by gate reflectometry [28]. A low-disordered array of tunnel-coupled QDs is also highly suitable for transferring qubit information over a distance of about 1–10 µm using a bucket brigade [35] or conveyor approach [36].

2.2. Electrostatic Device Simulations

We perform device simulations based on the presented device geometry to demonstrate the general functionality and identify the relevant feature sizes. Furthermore, we investigate two metallic top-gate structures. Firstly, we focus on a single set of top-gates, which crossed the silicon nano-ridge, as indicated in Figure 1. As a proof-of-principle, the electronic wave functions of a device tile consisting of three QDs are calculated within their electrostatic potential and tuned to be tunnel-coupled to all adjacent QDs. Secondly, we present a top-gate array, which is split and insulated along the symmetry axis shown in Figure 1. Signal routing from both sides of the nano-ridge is required in this case. Being able to apply different voltages to the top-gates on each side of the silicon nano-ridge, we tune one array of quantum dots and one single electron transistor (SET) in opposing corners of the silicon nano-ridge. Both gate structures are transversely symmetric and thus can be in principle extended to an arbitrarily-long tuned QD array.

For all simulations, the width w_r of the wet-etched trapezoidal silicon nano-ridge before LOCOS is set to 100 nm. The insulation of the silicon nano-ridge towards the top-gate structure consists of 10 nm of Al_2O_3. We use a metallic top-gate structure with a 30-nm gate width and 15 nm of SiO_2 insulation. For the second device containing the split gate structure, gates on opposing sides are insulated by 15 nm of SiO_2. The electrostatic potentials are calculated by solving the Poisson equation by the COMSOL Multiphysics® software package [37]. The electronic ground state energy levels and corresponding wave functions are calculated by solving the three-dimensional (3D) Schrödinger equation on a next-neighbor tight-binding model. We use the low temperature value $E_\mathrm{G} = 1.17\,\mathrm{eV}$ for the fundamental band gap of silicon in our calculations [38].

In bulk silicon, the conduction band minimum is six-fold degenerate along the <100> crystal directions [2]. Confinement of an electron in the, e.g., [001] direction splits this degeneracy into a two-fold degenerate out-of-plane valley labeled $\pm k_\mathrm{z}$ with the longitudinal effective mass $m_\mathrm{l} = 0.98\,m_{0,\mathrm{e}}$ relevant for the confinement energy and a four-fold degenerate in-plane valley labeled $\pm k_\mathrm{x}$, $\pm k_\mathrm{y}$ with relevant transverse effective mass $m_\mathrm{t} = 0.19\,m_{0,\mathrm{e}}$, where $m_{0,\mathrm{e}}$ is the free electron mass. While the $\pm k_\mathrm{z}$ valley is split off from the perpendicular valleys due to the confinement, potential strain, and the anisotropic masses, the mixing of the $-k_\mathrm{z}$ and $+k_\mathrm{z}$ valley states depends on the atomistic details of the confinement potential. We calculate the valley splitting between perpendicular valley states due to confinement and the effective anisotropic mass, but the remaining valley splitting within the $\pm k_\mathrm{v}$ ($v = x, y, z$) valley spaces are beyond the scope of our manuscript. Notably, the silicon nano-ridge is oriented along the equivalent <110> crystal axis due to the anisotropic wet-etching. Hence, the in-plane valleys $\pm k_\mathrm{x}$, $\pm k_\mathrm{y}$ will mix, and calculating the approximate valley splitting by confinement requires a $\phi = 45^\circ$ rotation of the effective mass tensor M about the z-axis. Therefore, we apply a unitary rotation $R(\phi, \theta)$ with $\theta = 0$, as depicted in Figure 2a. If the ground states are in the ellipsoidal energy surfaces k_z, there is no effect on the energy splitting of the lowest two eigenstates due to the identical in-plane effective masses $m_\mathrm{x} = m_\mathrm{y} = m_\mathrm{t}$. However, if the ground state is, e.g., within the $\pm k_\mathrm{y}$ valley space (e.g., due to strong confinement and thus large zero-energy in the z-direction), the effective masses are $m_\mathrm{y} = m_\mathrm{l}$ and $m_\mathrm{x} = m_\mathrm{z} = m_\mathrm{t}$. The effect of valley mixing for different rotation angles ϕ for a ground state in the $\pm k_\mathrm{y}$ valley is shown in Figure 2b. For $\phi = 45^\circ$ (relevant for our nano-ridge orientation), we identify a mixing of the rotated k'_y valley as a combination of $\pm k_\mathrm{x}$ and $\pm k_\mathrm{y}$ where the masses of the rotated $\pm k'_\mathrm{x}$ and $\pm k'_\mathrm{y}$ valleys are equal. This effective mass alignment leads to an energy level crossing and an additional four-fold degeneracy of these energy levels. In the following, we evaluate the respective energy level configuration by calculating the ground and first excited state for

each valley. Note that all energy levels are additionally two-fold spin-degenerate, since magnetic fields are not included in our simulations.

First, we present the calculations on the non-split metallic top-gate array, which allows the formation of a tunnel-coupled QD array. After tuning all the voltages applied to the gates, we find an electrostatic potential for three adjacent quantum dots, the calculated ground-state wave functions of which are shown in Figure 2c. The 3D wave functions are confined along the z-direction at the top of the silicon nano-ridge by the Si/SiO_2 interfaces. The corresponding potential is plotted along and perpendicular to the silicon nano-ridge through the maximum of the middle QD potential and an adjacent potential barrier. The additional strong confinement of the Si/SiO_2 interface in combination with the tuned electrostatic confinement of the gates ensure the intended formation of only a single energy level of all valleys below the Fermi level for every quantum dot. Adjacent QDs are tunnel-coupled with individually-tunable tunnel-couplings over multiple orders of magnitude. The tunnel-coupling between adjacent quantum dots is $t_c = 3.7\,\mu$eV for both tunnel barriers. The energy level splitting 1.7 meV is determined by the ground state towards the first orbital excited state within the same k_z valley space (Figure 2g). Note that the splitting within the mixed k_z valley space depends on the atomistic details of the barrier and is not calculated here. Energy splittings have to be much larger compared to the typical thermal energy of ~ 0.01 meV at operating temperatures of ~ 100 mK. Due to the strong confinement of the wave function along the z-axis by the interface, the energetic levels of the $\pm k'_x$ and $\pm k'_y$ in-plane valleys are lifted with respect to $\pm k_z$. Electron spin manipulation can be achieved by electric dipole spin resonance (EDSR) using a magnetic field gradient-inducing micro magnet [39]. Applying voltage differences of ± 1 mV on the opposing side-gates shifts the electron wave function by 2 nm. This controlled shift in combination with an assumed 1 mT/nm magnetic field gradient eads to an expected Rabi frequency of $f_{\mathrm{Rabi}} \approx 55$ MHz. Alternatively, the electron spin can be manipulated using electron spin resonance (ESR) using a strip line fabricated along the silicon nano-ridge [13].

Using the split top-gate array, the device is voltage-tuned to localize three adjacent quantum dots in one corner of the silicon ridge, as well as a single electron transistor (SET) in the opposite corner. The calculated electron wave functions and the corresponding electrostatic potential are depicted in Figure 2d. The adjacent three quantum dots are tunnel-coupled. The tunnel-coupling can be tuned over multiple orders of magnitude by changing the corresponding voltages applied to the barrier gates V_{B2} and V_{B3} (Figure 2e,f). This yields the possibility of performing dedicated two-qubit gates, as well as controlled electron shuttling. The energy level splittings between the ground state and first excited state of the different valleys are shown in Figure 2g. As discussed above, the strong confinement at the {111} interfaces of the silicon nano-ridge decreases the energetic levels of the $\pm k'_x$ and $\pm k'_y$ valley compared to the tuned QD located in the top of the ridge. The ground states of $\pm k'_x$ and $\pm k'_y$ cross the first excited state of the $\pm k_z$ valley. The energy level splitting 2.7 meV is larger due to the stronger confinement, but in comparison to the discussion above, limited by the two-fold degenerate ground state of the orthogonal $\pm k'_x$ and $\pm k'_y$ valleys. The operable temperature range for the proposed device is limited by the residual energetic splitting of the ground state in the $\pm k_z$ valley, which is out of the scope of this work. Previously-measured valley splittings range from 100 µeV up to 1 meV [22]. Thus, the device is operable at a temperature below 100 mK. The capacitive coupling of the middle QD and the QD of the single electron transistor is approximately 3.4 aF, dominantly determined by the width w_r.

The simulations show the high degree of tunability of the proposed spin qubit device. Using the split gate structure, a tunnel-coupled quantum dot array can be tuned in one corner of the silicon nano-ridge, while a capacitively-coupled SET can be formed in the opposing corner, allowing spin-to-charge conversion for qubit read-out.

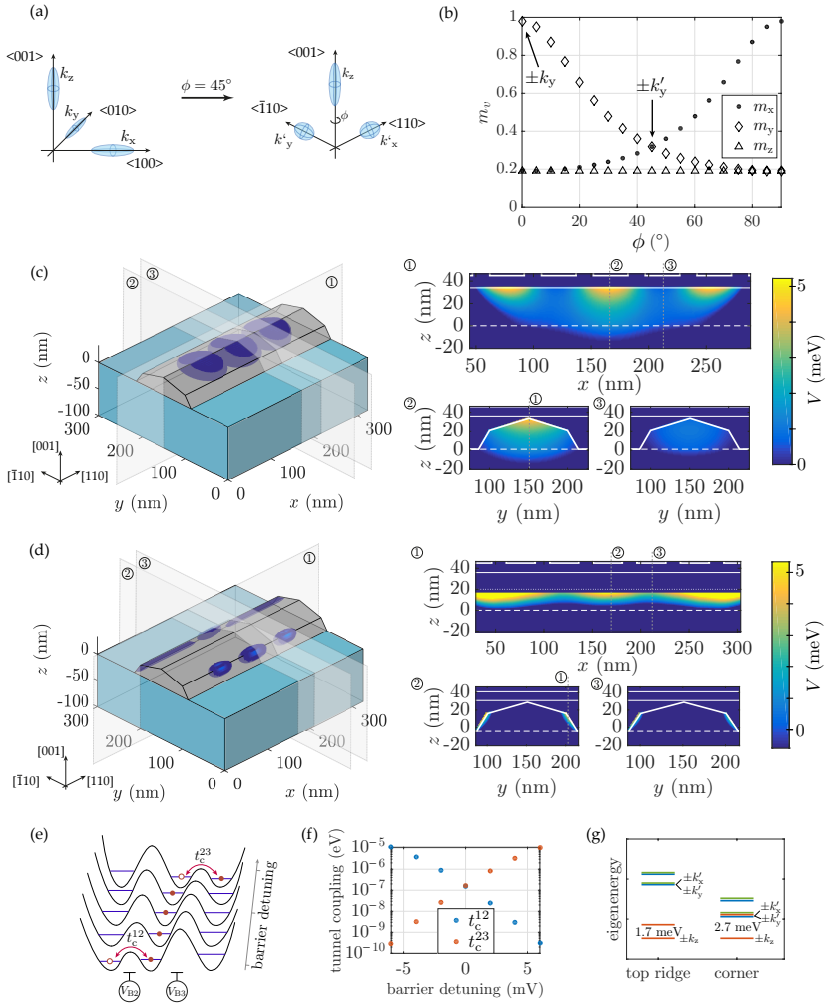

Figure 2. Electrostatic simulation of the silicon nano-ridge qubit device. (**a**) Schematic of the different ellipsoidal energy surfaces of the degenerate valleys present in the silicon crystal lattice. For simplicity, only one quadrant of the reciprocal space is shown. For rotating angle ϕ around the <001> crystal axis, the transverse effective masses mix changing the momentum ellipsoid for in-plane valleys k'_x and k'_y. (**b**) Effective masses m_v with $v = \{x, y, z\}$ of all crystal directions for different rotation angles. For $\phi = 45\,°$, the effective masses m_x and m_y are indistinguishable, leading to a crossing of the corresponding energetic states. (**c**) Simulated wave function of the electronic ground state for three tuned adjacent quantum dots located in the top of the schematically-shown silicon nano-ridge. All adjacent QDs are tunnel-coupled. Along three cross-sections, the electrostatic potential is shown within the overall device. The simulation is based on a 3D next-neighbor tight-binding model with a calculated electrostatic potential. $V = 0$ is defined as the conduction band minimum. (**d**) Simulated wave function of the electronic ground state for three tuned adjacent quantum dots and a single electron transistor (SET) located in opposite corners of the schematically-shown silicon nano-ridge. The electron reservoirs of the SET are sketched for clarity. Along three cross-sections, the calculated electrostatic potential is shown. $V = 0$ is defined as the conduction band minimum. (**e**) Schematic of the confining potential along the QD array for different barrier voltages $V_{B,2}$ and $V_{B,3}$. (**f**) Calculated tunnel couplings t_c for different voltage detuning of the barrier gates. (**g**) Energy levels of the ground and excited state within each valley for different wave function localizations corresponding to (c) top-ridge state and (d) corner states. For top-ridge states, the ground and first excited orbital state are built by $\pm k_z$ valleys. For corner states, the ground state is in the $\pm k_z$ valley space, while the first excited state is the first orbital state in the $\pm k'_y$ valley space.

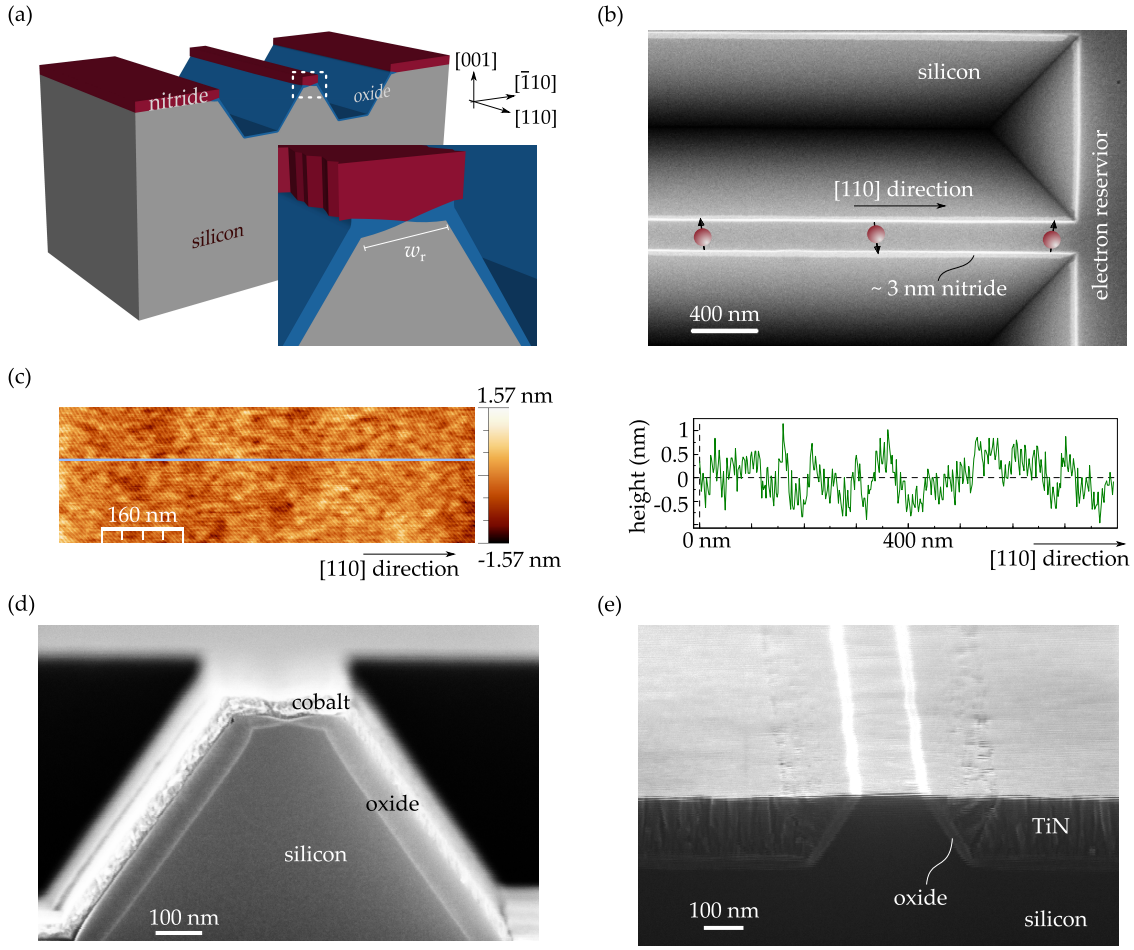

Figure 3. Fabrication, polishing, and topology of the silicon nano-ridge. (**a**) Schematic drawing (not to scale) of the silicon nano-ridge realized with anisotropic wet-etching of <100>-oriented silicon and dry oxidation. The inset depicts a close-up of the tip-area of the nano-ridge. (**b**) Top-view scanning electron micrograph (SEM) image of the trapezoidal structure formed after TMAH-etching. A small undercut of the thin silicon nitride hard mask is visible at the edge of the line structure, which reduces the impact of line-edge roughness of the initial lithography process on the resulting {111} facets. (**c**) Atomic force microscopy image of the etched (111) plane from a different sample with larger feature size. The root-mean-squared value 0.3992 nm is measured in a scanning area of 800 nm × 250 nm. A line-cut along the [110] direction shows a peak-to-peak value of < 2 nm. (**d**) SEM cross-section of the fabricated silicon nano-ridge. An additional cobalt layer is deposited to achieve better contrast during SEM imaging. The nitride hard mask is not visible due to its low thickness. (**e**) Electron micrograph of the planarized TiN side-gate electrodes. Reactively-sputtered TiN shows the typical columnar growth behavior.

3. Technology Modules

The technology modules needed for the realization of the presented device include the fabrication of the silicon nano-ridge with appropriate geometrical cross-section and high-quality Si/SiO_2 interfaces, the realization of side-gates with a damascene process, and the fabrication of an array of multiple nanoscale top-gate electrodes suitable for electron localization. To probe the quality of the nano-ridge sidewalls, we perform capacitance voltage measurements and determine the defect densities at the Si/SiO_2 interface and within the oxide. Chemical-mechanical polishing is used to prepare appropriate TiN side-gates, and for the top-gate fabrication, we develop a self-aligned spacer process that can be combined with a damascene process.

3.1. Fabrication of the Silicon Nano-Ridge

The silicon nano-ridge is fabricated by employing anisotropic wet-etching of crystalline silicon in a tetramethylammonium hydroxide (TMAH)-based solution and local-oxidation of silicon (LOCOS). The starting material is a Czochralski-grown, <100>-oriented 4″ silicon wafer. A standard cleaning procedure, consisting of piranha, SC-1, and SC-2, is carried out. After stripping the native/chemical oxide, silicon nitride is grown thermally in ammonia in a rapid thermal processing (RTP) chamber with high-vacuum capability. Despite its low thickness (~ 3 nm), thermally-grown silicon nitride exhibits an extremely low etching rate in TMAH and excellent impermeability to oxygen. Subsequently, electron beam lithography in combination with reactive ion-etching is used to define a line-pattern along the [110] direction, as illustrated in Figure 3a. After resist removal and directly after an additional short buffered oxide etch, TMAH (25 wt%) mixed with surfactant (isopropyl alcohol) is used to anisotropically etch the exposed silicon area at 80 °C. Figure 3b shows a trapezoidal structure bounded by two {111} facets formed due to the distinct etch-rate anisotropy of different crystallographic planes [40]. The inset in Figure 3a and the edge of the line structure in Figure 3b show a small undercut of the nitride hard mask due to the low etching rate of {111} facets. This is beneficial for reducing the line-edge-roughness of the line structure induced by imperfections of the initial lithography step.

In order to obtain a quantitative measure of the surface roughness of the wet-etched (111) facets, atomic force microscopy (AFM) is used. The measurement is performed on a large step structure (step height ~ 800 nm) formed by two {100} facets and a (111) facet. A silicon cantilever (nominal tip radius 10 nm, cone angle 40 °) is used to profile the tapered (111) surface in tapping mode (nominal values: resonance frequency 325 kHz, constant force 40 N/m). The tip axis is tilted by 15 ° with respect to the substrate normal in order to facilitate the imaging of the (111) facet. Figure 3c shows an AFM image and a line-cut of the wet-etched (111) facet in a scanning area of 800 nm × 250 nm. The measured root-mean-squared (RMS) = 0.3992 nm is well within the range of a commercial prime-grade silicon wafer (RMS = 0.2–0.8 nm) [41].

This top-down CMOS-compatible fabrication technique yields a high-quality trapezoidal nanostructure with minimal plasma damage and smooth surfaces comparable to a commercial prime-grade silicon wafer. In order to form a tip on top of the trapezoidal structure that not only allows the formation of a single QD, but also facilitates the generation of two corner-states located opposite of each other, dry oxidation in oxygen is carried out at 1050 °C. As a result of oxygen diffusion at the edges of the silicon nitride mask, a so-called bird's beak is formed from both sides, yielding the desired tip geometry of the nano-ridge (displayed in Figure 3d). The oxidation temperature is chosen to be higher than the viscous flow point to grow a relatively thick oxide in order to minimize the degradation of the Si/SiO_2 interface due to roughness induced by the oxidation process [42,43]. Note that the formation of the bird's beak and hence the geometry of the tip region of the nano-ridge can be adjusted with the thickness of the silicon nitride layer. Indeed, a nitride thickness (>75 nm) completely suppresses the formation of a bird's beak [44]. As a result, choosing an appropriate nitride thickness in combination with the oxidation process allow manipulating the geometry and thus the electrostatic potential of the tip-region employed for the generation of QDs.

For our final device, an *n*-type <100>-oriented silicon-on-insulator wafer will be used to define the silicon nano-ridge as illustrated in Figure 1. The LOCOS oxide needs to be relatively thick in order to enable a proper adjustment of the tip region of the nano-ridge. Therefore, if a thin oxide is desired as the insulator for the side-gates (for instance, to provide improved screening of electrically-active defects), the LOCOS oxide can be removed, and a thin, high-quality gate oxide can be deposited via remote plasma-enhanced chemical vapor deposition (CVD). In contrast to a second thermal oxidation, depositing an oxide preserves the geometry of the tip of the nano-ridge. As will be shown in the next section, our CVD-deposited oxide exhibits a quality level comparable to a thermally-grown oxide [45]. Subsequently, titanium nitride (TiN) is deposited via reactive sputtering with a thickness substantially larger than the depth of the TMAH-etched grooves. Chemical-mechanical polishing is then used to planarize the wafer to form self-aligned TiN side-gates, as depicted in Figure 3e. The columnar growth

behavior of reactively sputtered TiN leads to void formation where the (100) and (111) facets meet. This might be circumvented by changing sputter conditions or depositing the TiN layer conformally via atomic layer deposition (ALD). Note that in Figure 3e, slight over-polishing removed the tip-region of the nano-ridge; adding extra support structures in close vicinity to the silicon nano-ridge would be effective to avoid over-polishing. Next, a thin Al_2O_3 layer will be deposited onto the planarized sample surface via ALD that serves as the gate dielectric for the array of top-gate electrodes. High-density top-gates aligned perpendicular with respect to the nano-ridge will then be fabricated, as discussed in more detail in Section 3.3.

3.2. Characterization of the Si/SiO$_2$ Interface Quality

The electrical charge of single atomic bond defects is a source of potential disorder and can lead to the formation of unintentional QDs [15]. Therefore, the quantification and reduction of these charged defects is an important issue for quantum computing devices. To probe the quality of our oxides, we perform high-frequency capacitance-voltage measurements on macroscopic metal-oxide-semiconductor capacitors (MOSCaps) [46]. We characterize SiO_2 thermally grown at temperatures of 1050 °C, as well as CVD-SiO_2 deposited at temperatures of 350 °C. Furthermore, we quantifie defect concentrations on {111} facets (corresponding to our proposed device) in comparison to the {100} facet usually used for planar MOSFET devices. To improve the overall quality of our oxides, we perform a post-metal annealing in forming gas and measure the effect of defect passivation. The conceptual layout of such a MOSCap is shown in Figure 4a. We measure the parallel capacitance C_p and conductance G_p by an HP 4284A Precision LCR meter at room temperature, as displayed in Figure 4b. A voltage V is applied to the patterned top-electrode. The global metallic back contact is forced to a virtual ground potential using an auto-balancing bridge. We use *n*-type silicon substrates to be sensitive to defects that trap and emit electrons.

Varying V, the MOSCap can be tuned into different working regimes of accumulation, depletion, and inversion [46] (pp. 71–98). By applying $V > 0$ V, electrons are accumulated at the SiO_2 interface (accumulation region). By decreasing V, the electrons are repelled from the interface, and the capacitive contribution of the semiconductor increases (depletion). Within this region, we identify the flat band voltage V_fb at which the band bending of the semiconductor at the interface is zero. By decreasing $V < 0$ V further, a hole inversion layer is induced at the MOS-interface (inversion). The quasi-static theoretical capacitance over all working regimes is indicated by the red dashed lines in Figure 4. To perform high-frequency capacitance measurements, an oscillating signal of amplitude of 20 mV is added to V, and its frequency f is varied between 20 Hz and 1 MHz, effectively suppressing the hole inversion layer [46] (pp. 99–155). Hence, the resulting discrepancies of the quasi-static theoretical model and the measured high-frequency data can be attributed to this suppression of inversion and additional influences of defects within the oxide-semiconductor layer stack. Using the electrical model shown in Figure 4b, we extract the dielectric constant of the oxide ε_r, defects within the oxide at a fixed location D_f, rechargeable defects D_r as a subset of D_f, and interface-induced defects D_it [46]. The dielectric constant is determined by tuning the MOSCap in accumulation and measuring the oxide capacitance. By comparing the measured data and the theoretical expectation in flat band condition, we calculate D_f and D_r by evaluating the overall shift and the hysteresis between forward and backward voltage sweeps of V. The interface defect density D_it is determined using the conductance method described in [46] (pp. 176–234).

The measured capacitance and conductance of an Al/SiO_2/Si capacitor are shown in Figure 4b,c. Here, SiO_2 is deposited by chemical vapor deposition on (111) substrates with a thickness of 17.0 ± 0.1 nm measured with ellipsometry. Square-shaped aluminum electrodes with an area of 0.52 mm^2 are patterned with electron-beam evaporation and lift-off. The frequency of the oscillating voltage bias changes from low frequencies encoded in light blue towards high frequencies encoded in dark blue. The extracted dielectric constant $\epsilon_\mathrm{r} = 3.95 \pm 0.04$ is well within the reported range of 3.70–4.00 [47,48] and does not show any frequency dispersion. The clear shift of the measured

data depending on the frequency compared to the calculated theoretical curve is caused by all charges, i.e., $D_{tot} = D_f + D_{it}$, in the vicinity of the interface. The polarity of this ensemble is positive. The frequency dispersion is also visible in the G_p/ω-peak voltage location. From the polarity of the ensemble and the decreasing deviation from theory in the flatband condition with increasing frequency, we conclude that P_b defects located at the interface are predominant. This defect originates from a free bond of a Si atom, which was backbonded to three other Si atoms ($Si^\circ \equiv Si_3$) [49]. The positive polarity is caused by its 0-1 electron charge transition, where a single electron is loaded into the unoccupied, positively-charged Si atom [50,51]. By using the conductance method, we extract $D_{it} = (5.6 \pm 0.5) \cdot 10^{11}\,V^{-1}cm^{-2}$. From the hysteresis of the measured data for a single frequency, we extract $D_r = (2 \pm 0.3) \cdot 10^{11}\,cm^{-2}$ without any frequency dispersion observed. Subsequently, we approximate D_f to be on the order of $10^{12}\,cm^{-2}$ due to the indistinguishability of all charges causing the capacitance voltage shift. Defects might also be distributed across the bulk of the oxide layer and then result in a bulk density of approximately $D_f = 5 \cdot 10^{17}\,cm^{-3}$.

In order to reduce defect concentrations, a post-metal annealing is carried out in forming gas N_2H_2 at 400 °C for 30 min [52,53]. The measured capacitance and conductance of the annealed $Al/SiO_2/Si$ capacitor are shown in Figure 4d,e with an oxide thickness of 16.0 ± 0.1 nm and a top aluminum pad area of 1.05 mm^2. The extracted dielectric constant is $\epsilon_r = 4.18 \pm 0.04$, indicating incorporated hydrogen [48]. Single hydrogen atoms form strong O-H bonds to oxygen atoms, which lead to a low concentration of SiOH within the SiO_2 layer [54]. In comparison to the unannealed sample, the measured data does not show any frequency dispersion due to the successful passivation of the previously-measured P_b defects with hydrogen ($HSi \equiv Si_3$) [55–58]. The polarity of the ensemble of these charges is negative. We extract $D_{it} = (2 \pm 1) \cdot 10^{10}\,V^{-1}cm^{-2}$, which agreed well with the literature [59] and is comparable to thermally-grown high-quality interfaces on (100) silicon substrates. Subsequently, we determine $D_f = 1.41 \cdot 10^{12}\,cm^{-2}$. Based on the low D_{it} and the absent frequency dispersion, we conclude the polarity of D_f to be negative. The subset of rechargeable defects $D_r = (1.2 \pm 0.1) \cdot 10^{11}\,cm^{-2}$ decreases only slightly.

As a reference, measurements of an annealed $Al/SiO_2/Si$ capacitor with thermally-grown SiO_2 using RTP at a process temperature of 1050 °C in oxygen on (111) *n*-type silicon substrate are carried out. The post-metal annealing is done using the same set of process parameters as stated above. The dielectric constant is measured to be $\epsilon_r = 3.74 \pm 0.04$. The interface defect density $D_{it} = (3 \pm 1) \cdot 10^{10}\,V^{-1}cm^{-2}$ is comparable to the passivated interface of the CVD-deposited SiO_2 discussed above. Similar fixed defect concentrations are measured with $D_f = (1.31 \pm 0.01) \cdot 10^{12}\,cm^{-2}$, while $D_r = (2 \pm 1) \cdot 10^{10}\,cm^{-2}$ is significantly smaller due to the higher process temperature. Further measurements of the $Al/SiO_2/Si$ capacitor on (100) silicon substrates show similar defect concentrations.

The presented Si/SiO_2 interface using our CVD-deposited SiO_2 exhibits a similar fixed defect and interface defect concentrations as our thermally-grown high-temperature RTP layers. Furthermore, CVD processes offer a lower thermal budget, while the characterized SiO_2 layer indicates higher concentrations of incorporated hydrogen than thermally-grown SiO_2 layers. For electron spin qubit experiments, the total amount of defects within the SiO_2 layer can be minimized by reducing the thickness of the SiO_2 layer while still preserving the insulating properties. In addition, defect concentrations on the order of $10^{10}\,cm^{-2}$ can be compensated electrostatically by applying suitable voltages to the respective gates [15]. The frequency-dependent response of the measured defects are measured up to frequencies of 1 MHz limited by the setup. Qubit manipulation experiments are typically performed with voltage signals applied to gates at a frequency of 20 GHz (electron spin resonance with an externally applied magnetic field) [21]. For increasing frequencies, the effect of defect-induced charge noise is negligible compared to Johnson noise sources. To compensate the static effect of charged interface defects, the development of a high-density gate structure in close vicinity with the interface is mandatory to preserve the necessary tunability.

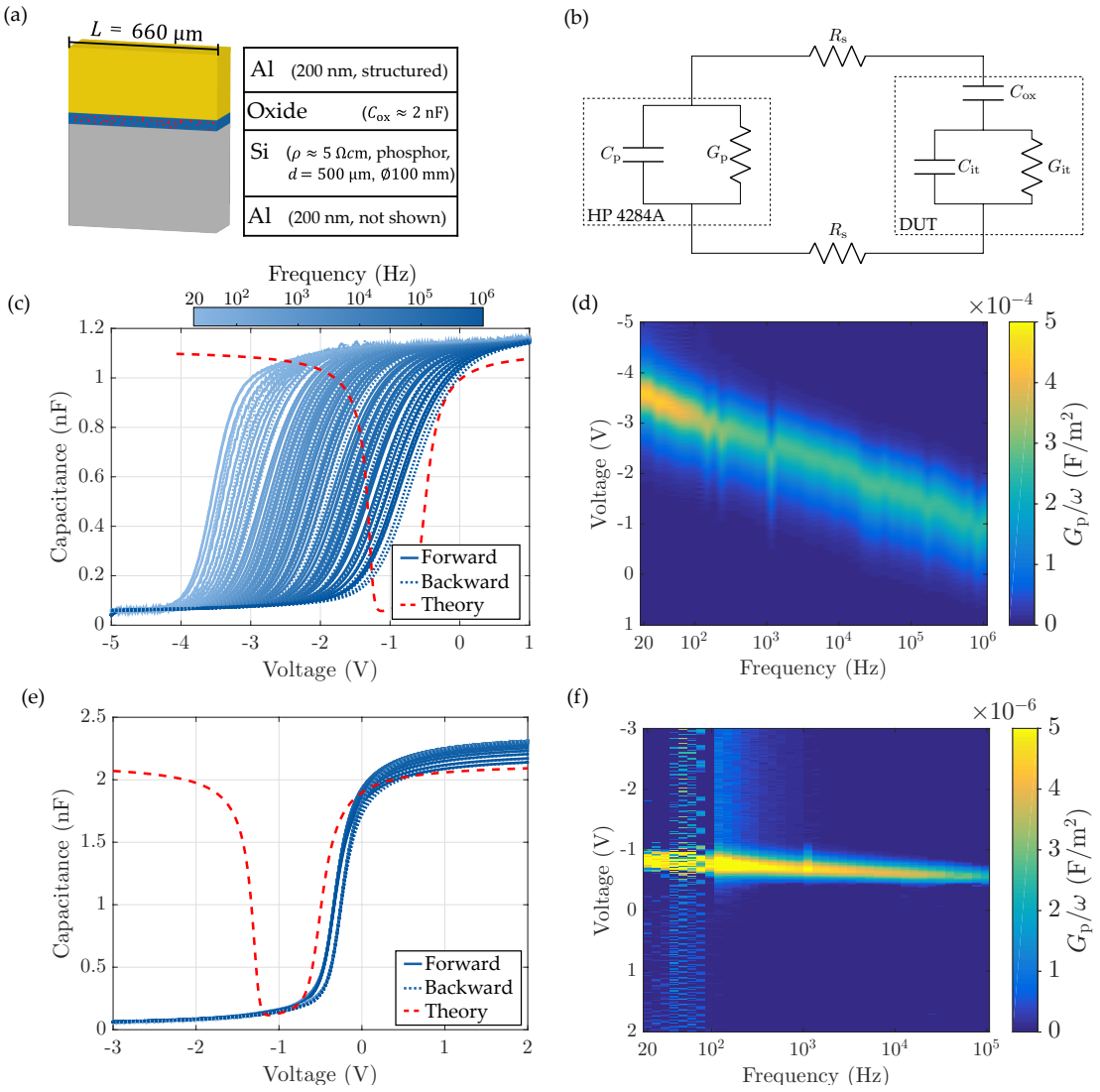

Figure 4. Electrical characterization of the Si/SiO_2 layer stack with respect to defect densities and post-metal annealing. (**a**) Schematic of a metal-oxide-semiconductor capacitor with a structured top metal electrode with an area L^2. (**b**) Equivalent circuit of the measurement setup tuned in depletion. The device under test (DUT) is modeled by an oxide capacitance C_{ox} and a parallel capacitance C_{it} and conductance G_{it}. Additional contact resistances are modeled by R_s. The parallel capacitance C_p and conductance G_p are measured. (**c**) Measurement of $Al/SiO_2/Si$ capacitor. SiO_2 is deposited by CVD on a <111>-oriented substrate with a measured thickness of (17.0 ± 0.1) nm and an aluminum top electrode with an area of 0.52 mm^2. Darker curves indicate higher frequencies and lighter curves lower frequencies. The dashed curves indicate voltage backward sweeps. The red dashed line corresponds to the calculated theoretical quasi-static CV-curve. (**d**) Measurement of the parallel conductance over angular frequency G_p/ω corresponding to (c). (**e**) Measurement of annealed $Al/SiO_2/Si$ capacitor. SiO_2 is deposited by CVD on a <111>-oriented substrate with a measured thickness of (16.0 ± 0.1) nm and an aluminum top electrode with an area of 1.05 mm^2. Post-metal annealing is carried out in N_2H_2 at 400 °C for 30 min. (**f**) Measurement of the parallel conductance over angular frequency G_p/ω corresponding to (e). For frequencies $f \leq 100$ Hz, ground oscillations are visible.

3.3. High-Density Spacer Gate Patterning

To fabricate the gate structure for quantum dot tuning and qubit manipulation, electron beam lithography in combination with metal lift-off gates have been widely used [13,60,61]. To achieve small gate pitches and high-density gate structures, multiple layers have to be aligned and electrically insulated [17,18]. Depending on the used material combination, strong variations in gate size and uncontrolled oxidation of the metal gates can lead to additional variations in the final gate structure [62]. Furthermore, multiple gate layers lead to differences in the controllability of the chemical potential depending on the applied voltages due to the different gate dielectric thicknesses above the silicon surface.

In this work, we aim at a high-density gate array in a single layer using a self-aligned spacer process in combination with a damascene process. The fabrication scheme for the used spacer process is shown in Figure 5a. The layer-stack includes an Al_2O_3 etch stop layer (green), a sacrificial amorphous silicon (αSi) layer (dark grey), and a SiO_2 hard mask (blue). Electron beam lithography (EBL) is initially used to pattern the gate structure (60-nm lines with 120-nm pitch) in the resist (red) with a 30-kV RAITH eLine system. The structured resist is transferred into the sacrificial layer using a highly-anisotropic SF_6/O_2 reactive ion etching process at a temperature of $-130\,^{\circ}C$ in an Oxford Instrument PlasmaPro 100 Cobra etching system. Then, SiO_2 is conformally deposited by a high-pressure SiH_4/O_2 CVD process at a temperature of $350\,^{\circ}C$ in an Oxford Instruments Plasmalab System 100. Finally, we etch the gate structure by a second SF_6/O_2 dry-etching process developed for a high SiO_2/αSi etch rate selectivity. The deposited SiO_2 on the sidewall of the transferred structure withstand the back-etch, while the sacrificial layer is fully removed. The remaining SiO_2 sidewalls (from now on referred to as spacers) provide the electric insulation of the metallic gate array. Similar to the fabrication of the side-gates as discussed above, subsequently over-depositing these spacers with TiN by atomic layer deposition (ALD) followed by a TiN/SiO_2 selective damascene process using chemical mechanical polishing yields insulated gates within one single layer. This step has to be done in the future.

Fabricated SiO_2 spacers of 15 nm in width with a (75 ± 5) nm pitch are shown as cross-section and top-view images taken with scanning electron microscopy (SEM) in Figure 5b. The spacer height is measured with 45 nm limited by the second anisotropic dry-etching process. Smaller feature sizes have been achieved by downscaling the initial gate structure and decreasing the conformally-deposited SiO_2 layer thickness. A top-view image of fabricated SiO_2 spacers of 10 nm in width with a 50-nm pitch taken with SEM is shown in Figure 5c. Due to the reduced feature size, SEM leads to significant charging effects and deformations of the fabricated SiO_2, prohibiting cross-section images. Therefore, we cannot provide a cross-section image of these smaller SiO_2 spacers. Electrical contacts are schematically added for clarity including ohmic contacts to the silicon nano-ridge indicated by crossed squares. The final gate structure is used for top-ridge localization, as discussed above.

The final size and pitch of these SiO_2 spacer depend predominantly on the initial resolution of the electron beam lithography. By downscaling the gate structure, a target gate width of 30 nm with a pitch of 45 nm can be achieved. Especially, the high density gate structure within a single layer results in a sensitive control of the electrostatic potential within the silicon ridge. This allows the possibility to compensate disorder sources as discussed above. By adjusting the gate design, we can fabricate an additional spacer along the symmetry axis of the silicon nano-ridge. By contacting the gates on each side of the nano-ridge, we achieve further individual gate tuning capabilities in each corner of the silicon nano-ridge.

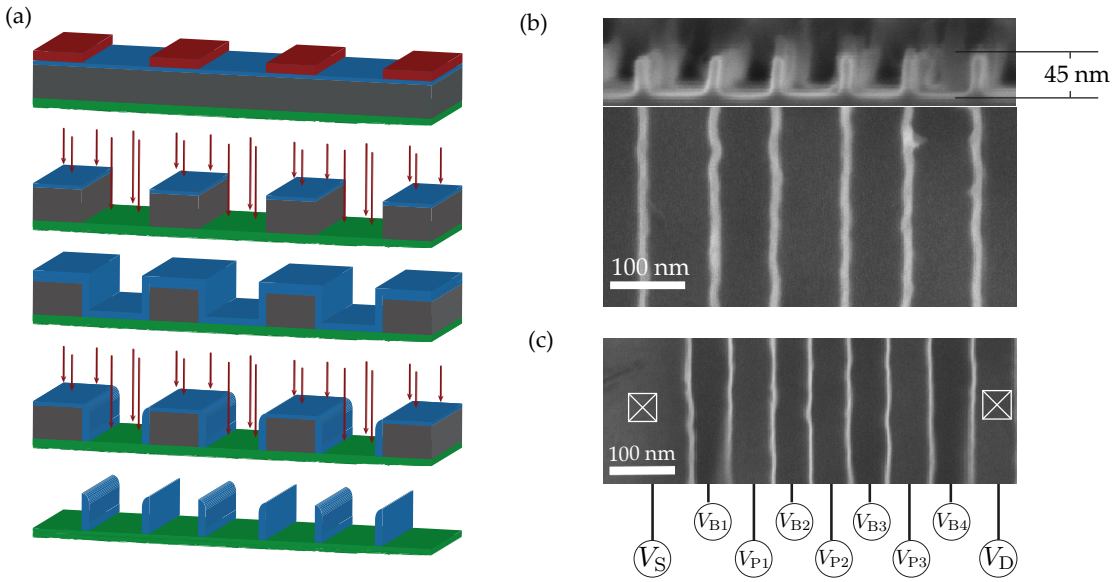

Figure 5. Fabrication steps of the self-aligned spacer process as the basis of a high-density gate structure. (**a**) Schematic of the self-aligned spacer process. Top to bottom: structured resist (red) on the layer-stack including the SiO_2 hard mask (blue), the αSi sacrificial layer (dark grey), and the Al_2O_3 etch stop layer (green); anisotropic dry-etching; conformal SiO_2 deposition; anisotropic dry back-etching; free-standing oxide spacer. (**b**) Cross-section and top-view scanning electron micrograph of the free-standing SiO_2 spacer with a width of 15 nm on a (75± 5) nm pitch. The spacer height is 45 nm. (**c**) Scanning electron micrograph of top-viewed 10 nm free-standing SiO_2 spacer with a 50 nm pitch. Metallic gates between the spacers are not shown here, but voltage labels are added for clarity (cf. Figure 1). The final gate structure is used for top-ridge localization. Ohmic contacts to the electron reservoirs at the ends of the silicon nano-ridge are indicated by crossed squares.

4. Conclusions

We presented a new silicon qubit device design consisting of a linear array of electrostatically-defined quantum dots, each of them hosting one electron spin qubit. The QDs are confined along a trapezoidal silicon nano-ridge with wet-chemically-etched {111} facets for reduced potential disorder. We perform electrostatic simulation on the device design and demonstrate the required technology modules, which are adapted from the well-developed industry-compatible processes and thus promise scalable multi-qubit device fabrication.

According to the electrostatic simulations, we can generate a translationally-symmetric array of QD with tunable tunnel barriers in our device and in principle with an arbitrary length. Using a split-gate array as the top-gate structure, a linear double-QD array or alternatively a linear QD array with adjacent a single electron transistor can be formed. The perpendicular valley states are sufficiently split off (>1 meV) from the mixed $\pm k_z$ valley states due to confinement and the anisotropic electron mass. Thus, the <110> lattice orientation of our silicon nano-ridge does not impose complications on the valley-orbital states for the qubit.

The fabrication of the nano-ridge is based on selective anisotropic wet-etching using TMAH, resulting in atomically-flat {111} sidewalls with RMS = 0.3992 nm and dry oxidation at a temperature above the viscous flow point. Thus, the high-quality, confining Si/SiO_2 interface is intrinsically protected and comparable to industrial standards. After deposition of two TiN side-gates, chemical-mechanical polishing enables the fabrication of a linear array of metal gates by a SiO_2 spacer (10 nm in width) process. We achieve a 50-nm gate pitch, already very close to the simulation requirement of 45 nm. Electrical defect characterization of the CVD deposited SiO_2 on the {111} silicon facet shows an interface defect density of $D_{it} = (5.6 \pm 0.5) \cdot 10^{11}\,V^{-1}cm^{-2}$ and $D_{it} = (2 \pm 1) \cdot 10^{10}\,V^{-1}cm^{-2}$ before and after thermal treatment, respectively. The polarity of the dominating

defects is changed by the treatment. The defect density observed is similar to our thermally-grown SiO_2 on the {001} facet.

In the future, our proposed multi-qubit device can be operated in two ways, both significant for future scalable quantum computing architectures with quantum error correction: (1) A long linear array of physical qubits with next-neighbor two-qubit gates is sufficient to define a logical, thus quantum error-corrected qubit [32]. Such a linear chain can be realized with our device concept. (2) Looking toward the future, a 2D grid of silicon nano-ridges with high-density gate arrays is within reach. In this case, the electrons and thus the qubits can be shuttled coherently through a 2D grid structure and interact with their four next-neighbor qubits, which is sufficient for the realization of the surface code [8]. In this case, our suggested device acts as a coherent link between adjacent qubits of about 10 µm in distance. This approach corresponds to a qubit architecture as proposed in Ref. [3] with one physical qubit at each crossing point of the coherent links. It constitutes a sparse qubit array, which relaxes constraints on signal fan-out.

Author Contributions: J.K. fabricated the spacers, performed device simulations, and material characterization measurements, and wrote the paper; B.S. fabricated the silicon nano-ridge and wrote the paper; J.B. performed the simulations; S.K. fabricated MOS-capacitors and performed material characterization measurements; L.H. developed the chemical-mechanical polishing process. J.K. and L.R.S. invented the device concept and fabrication scheme and contributed to the writing of the paper.

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