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Improving the Lot Fabrication Stability and Performance of Silica Optical Films during PECVD

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Abstract: Silica optical film specifications are determined by their processing capability and their fabrication stability. Here, a statistical process control (SPC) approach usually used in planar lightwave circuits (PLC) is adopted to analyze the stability of the silica optical film fabrication process. Apart from the raw materials, certain key external factors have to be taken into consideration during the PLC process, such as temperature, relative humidity, process variation and machine aging. The fabrication process can be adjusted according to SPC-based results in real-time, so as to produce high quality silica optical film. By using this method, it is possible to assess the effectiveness of older production lines and extend their production capacity at minimal cost.

Keywords: silica optical waveguide; planar lightwave circuit; optical film; PECVD; lot fabrication stability

1. Introduction

Following recent developments in planar lightwave circuits (PLC), silica optical waveguides have come to play an important role in optical fiber communications and optical fiber sensor systems. They offer a number of notable advantages, including low propagation loss, low fiber-to-chip loss, an adjustable refractive index, good integration capability and high mechanical stability [1–3]. There are various silica optical waveguide devices, including $1 \times N$ (N = 2, 4, 8, 16, 32, 64 . . . . . .) power splitters, arrayed waveguide gratings (AWG), variable optical attenuators (VOA), ring resonators and star couplers, all of which have been successfully fabricated using PLCs [4,5]. A silica optical waveguide consists of a core layer, an upper cladding layer and a lower cladding layer. The core layer has a high refractive index (RI), whilst the cladding layers have a lower RI. Their low propagation loss is a particularly important property of silica optical waveguides. Typically, this is lower than 0.1 dB/cm. Similarly, they have a low fiber-to-chip coupling loss of less than 0.1 dB/point and a low RI contrast (Δ = 0.25–1.5%) [6–8]. Usually, silica optical waveguides are fabricated using Si or a fused silica substrate. The fabrication process includes the lower cladding layer deposition, the core layer deposition, a masking deposition, photolithography, the core etching and the upper layer deposition. Silica optical films can be used for the core layer, lower cladding layer and upper cladding layer [7,8]. By adding materials such as germanium (GeO_2-SiO_2), phosphorous (P_2O_5-SiO_2), nitrogen (SiON-SiO_2) and boron (B_2O_3-SiO_2), or a combination of these materials, silica optical films can be used to precisely adjust the RI. Their thickness and residual stress can be controlled during the processing phase. They can be fabricated by means of thermal oxidation and chemical vapor deposition (CVD). The latter can include atmospheric pressure CVD (APCVD), low pressure CVD

(LPCVD), plasma enhanced CVD (PECVD) and electron cyclotron resonance CVD (ECRCVD), or a combination of these methods [9–12]. Flame hydrolysis deposition (FHD) and a sol gel method can also be used [12,13]. Out of all of these methods, PECVD offers particular advantages. This is because of its ability to control the RI, thickness, residual stress and surface roughness [14,15]. A lot of research has been devoted to studying the relationship between various process parameters (Radio frequency power, gas flow, chamber temperature, chamber pressure, etc.) and the quality of the film (RI, film thickness, etc.) [14,15]. However, very few papers have examined the relationship and process stability between them in lot fabricating.

In this paper, we focus on lot fabrication stability using PECVD for GeO_2-SiO_2-based silica optical films in relation to certain key parameters, such as the RI and film thickness. This can be used to determine how well the fabrication process will cope with the required tolerances, for the selection or modification of the fabrication process during optical waveguide design, for the specification of the processing requirements for PECVD machines and, above all, to reduce variability in the fabrication process.

2. Lot Fabrication

A 6 μM ± 0.4 μM thick GeO_2-SiO_2 optical film was deposited on 23 lots (with 15 pieces per lot) of 6″ fused quartz wafers, 1 mm thick and 1.4574 at 632.8 nm. The RI contrast between the core layer and the cladding layer was 0.36% (Δ = 0.36% ± 0.05%). The GeO_2-SiO_2 optical film was produced by means of $SiH_4/GeH_4/N_2O$ high density plasma chemistry in an AMAT CENTRUA 5200 PECVD machine, where the plasma was generated at 13.56 MHz. The plasma parameters were fixed as follows: An RF (Radio frequency) power of 350 W; a processing pressure of 2.7 Torr; an electrode and wafer gap of 450 mils (11430 μM); a wafer temperature of 350 °C; and a chamber wall temperature of 60 °C. The other processing parameters were as follows: A SiH_4 flow of 40 sccm; a GeH_4 (combined with 95% H_2) flow of 72 sccm; and a N_2O flow of 2500 sccm. The deposition time was set to 1090 s. Each wafer was complete after the PECVD deposition. The deposition chamber was cleaned by running 20 cycles of a standard plasma cleaning process with the gas CF_4. After the PECVD deposition process, the wafers were annealed at 1100 °C for 2 h.

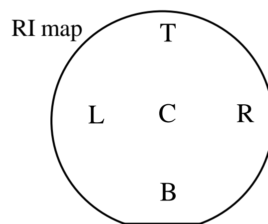
One lot of the fused quartz wafers was subjected to deposition each day for 23 days, so that we ended up with a total of 345 wafers. The GeO_2-SiO_2 optical film's RI was measured using a prism coupling instrument and its thickness was measured using a film thickness gauge. The measurement error was approximately ±0.0001 for the RI and ±0.1% for the thickness. For each wafer, five positions (T for top, C for center, B for bottom, R for right and L for left) were measured on the wafer and the RI and thickness values were analyzed. RI-T, RI-C, RI-B, RI-R and RI-L refer to the RI of the top, center, bottom, right and left points on each wafer, respectively. THK-T, THK-C, THK-B, THK-R and THK-L refer to the thickness of the layer at the top, center, bottom, right and left points on each wafer, respectively.

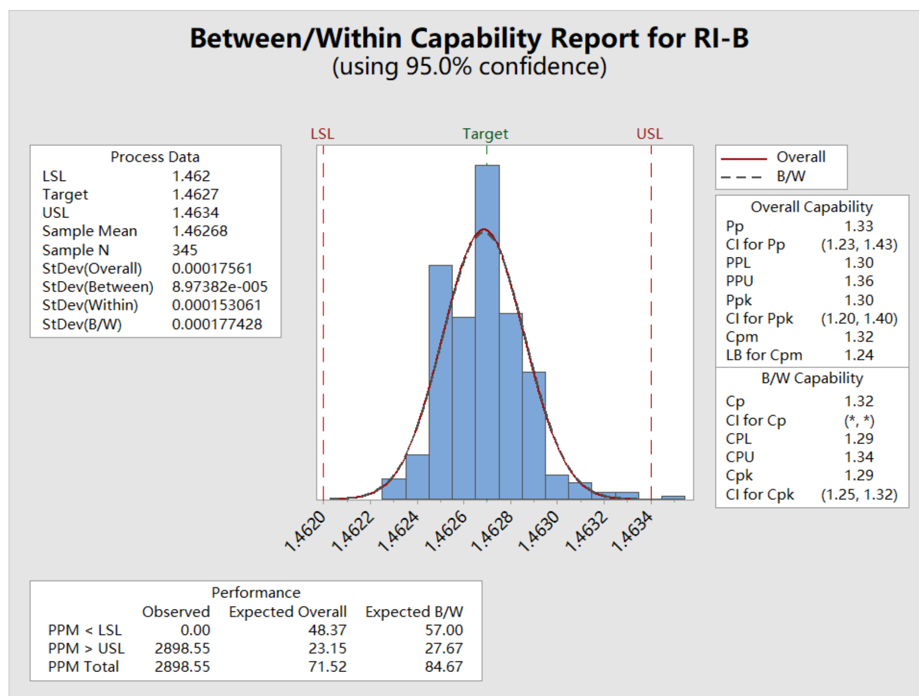
3. Results and Discussion

3.1. RI of the GeO_2-SiO_2 Optical Film

Figure 1 shows the RI maps and histograms for the 345 wafers with their specification limits and targets for RI-B, RI-C, RI-T, RI-R and RI-L. According to the requirements for silica optical waveguides, the lowest specification limit for the RI was set at 1.4620, the highest specification limit was set to 1.4634 and the RI target was set to 1.4627. The data presented in Figure 1 suggests the wafers were very close to having a normal distribution. The RI for RI-B, RI-R and RI-L were closest to the RI target. The RI for RI-C was lower than the RI target and the RI for RI-T was higher than the RI target. Cp is a measure of the potential capability of the process. Cp = (USL − LSL)/(6 × StDev), where USL is the upper specification limit, LSL is the lower specification limit and StDev is the standard deviation. According to statistical process control (SPC) theory, the benchmark can be divided into several grades.

Each grade represents the precision or potential capability of the process. In many industries, the Cp is divided into 4 grades: Cp $\geq$ 1.33 means that the process is stable and the deviation can be reduced; 1.00 $\leq$ Cp < 1.33 means that there is a risk of defective products in the process, so the specific reasons need to be checked and adjusted in time; 0.83 $\leq$ Cp < 1.00 means that the process is unstable and that the specific reasons need to be found and adjusted in time; Cp < 0.83 means that the process is unsatisfactory and that it will need to analyzed and corrected [16]. RI-C, RI-T, RI-R and RI-L all returned values of more than 1.33, but the Cp index for RI-B was 1.32, suggesting the quality of the fabrication was a mildly variable, though the process was still under control. The Cp can be compared to the Cpk. This is another measure of the potential capability of the process, however it is based on the minimum CPU and CPL. CPU is a potential capability measure based on the upper specification limit. CPL is a potential capability measure based on the lower specification limit. The Cpk benchmark has the same status as the Cp [16] and they are approximately equal, with the fabrication process being centered between the specification limits.





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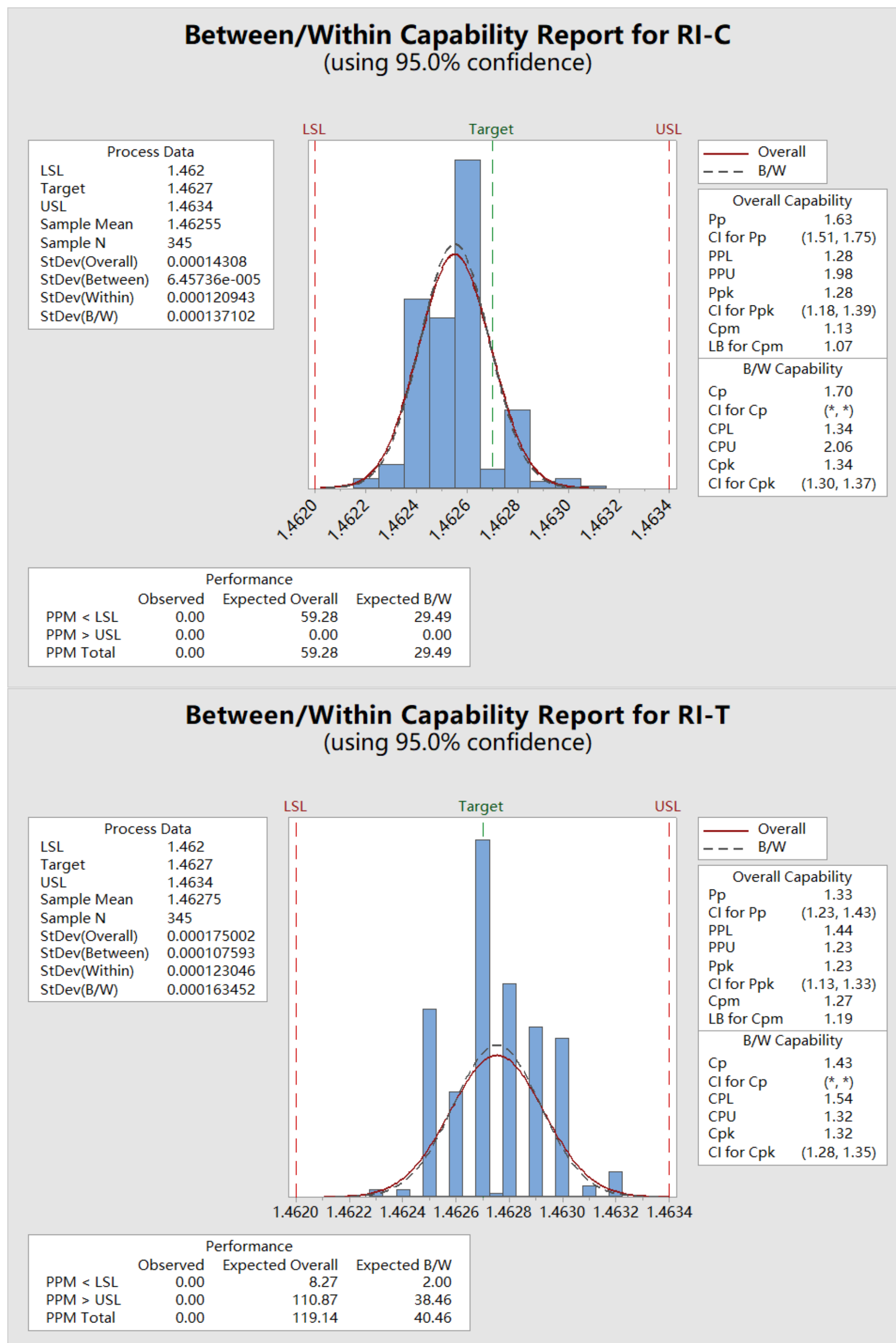

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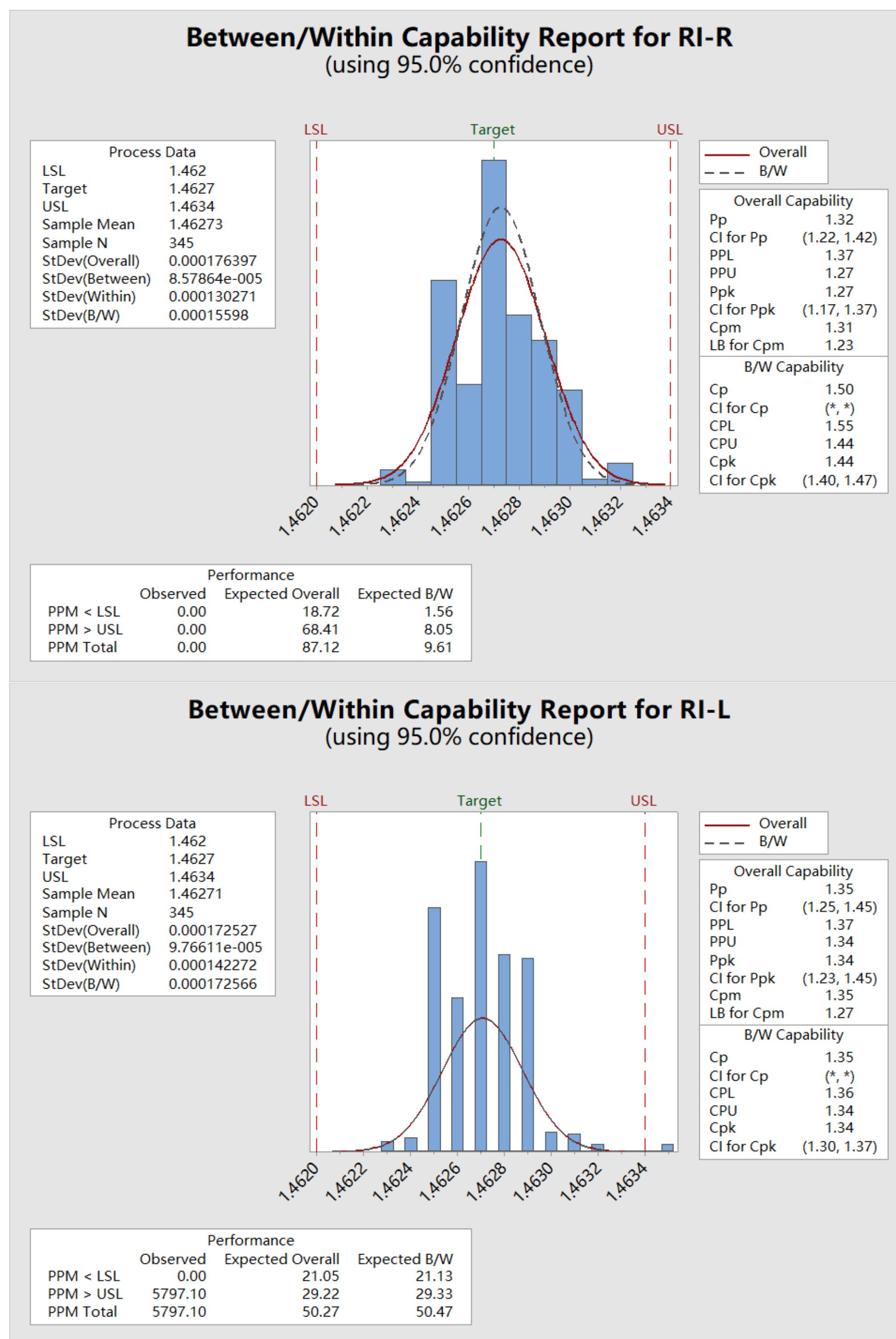


Figure 1. Refractive index (RI) maps and histograms for the 345 wafers with their specification limits and target for RI-B, RI-C, RI-T, RI-R and RI-L. LSL = 1.4620, USL = 1.4634 and the target = 1.4627.

Figure 2 shows the RI between/within capability sixpack report for the 23 lots, and Figure 3 shows the RI between/within capability sixpack report for the 345 wafers. For the data in Figures 2 and 3, p (the probability value test) < 0.05. This means that the RI of the 23 lots (or 345 wafers) did not have a normal distribution for some reason (possibly temperature, relative humidity, material variation, process variation or machine aging). Looking at the data in Figures 2 and 3, the RI for the first six lots is very close to the RI target of 1.4627. It was the subsequent lots that began to deviate, with a maximum RI of 1.4632. The Cp/Cpk of the 23 lots and 345 wafers, however, exceeded 1.33, which indicates a capable process overall.

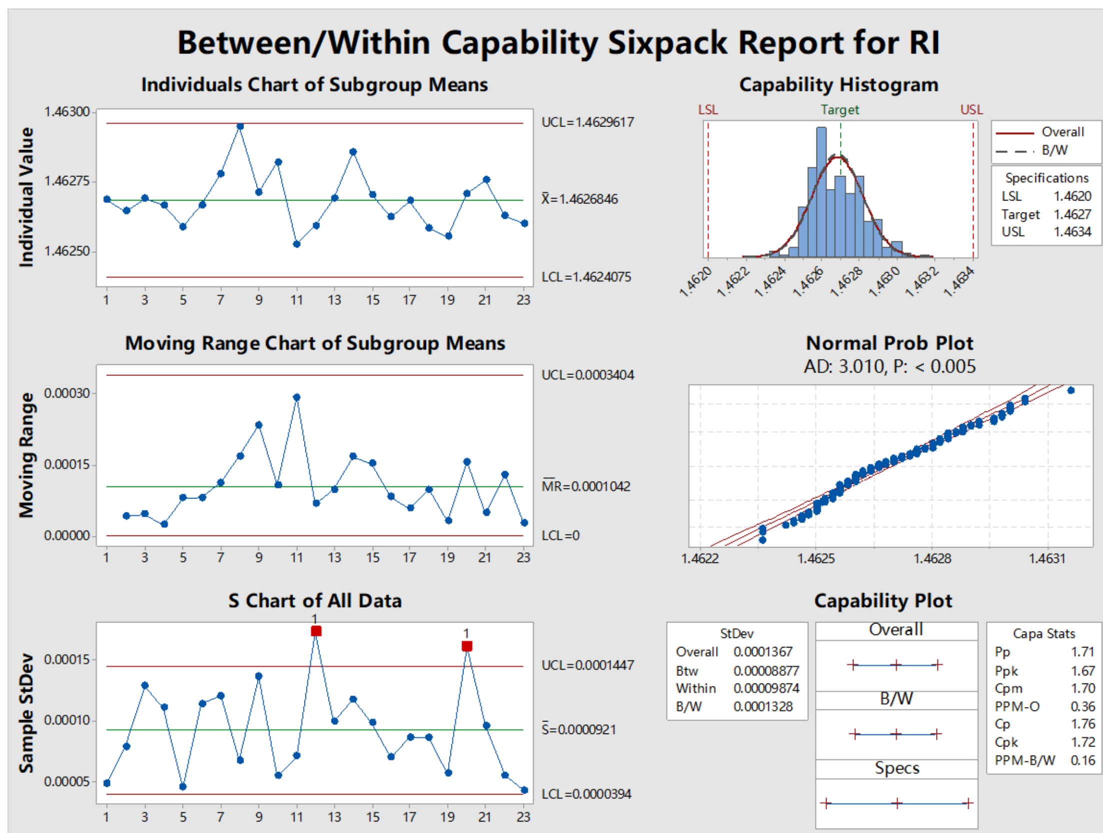


Figure 2. RI between/within capability sixpack report results for the 23 lots.

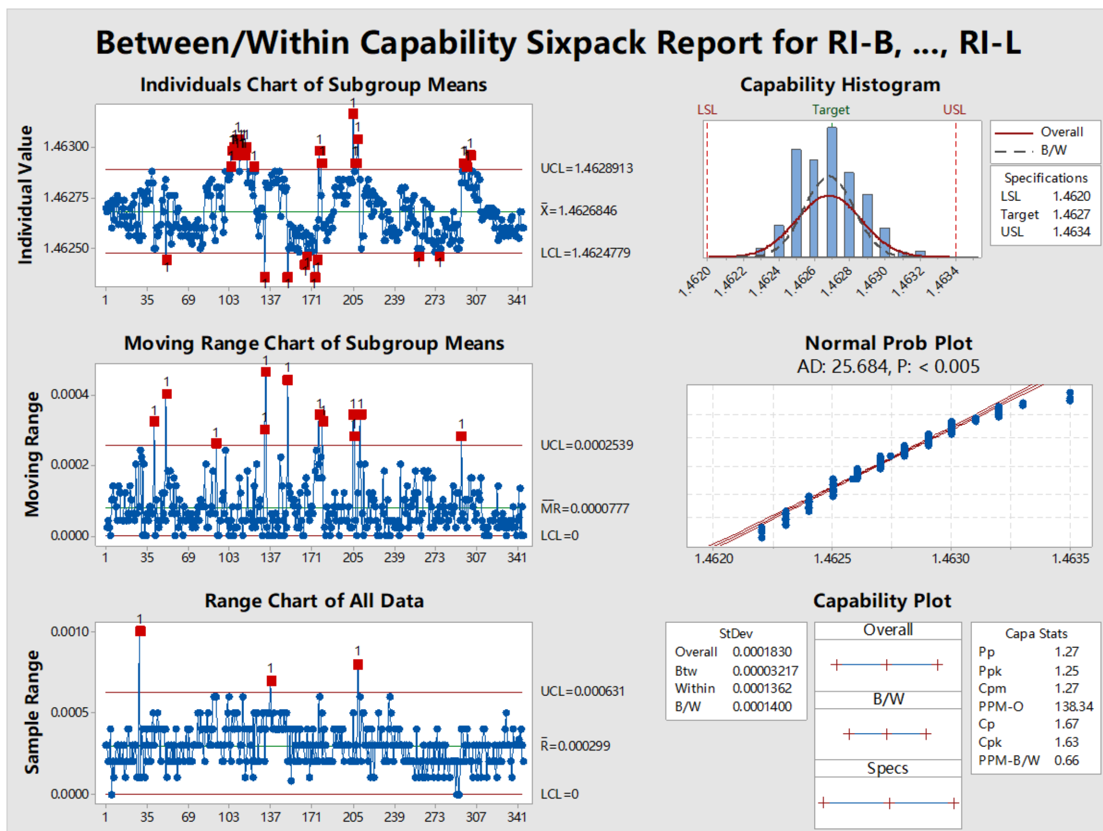
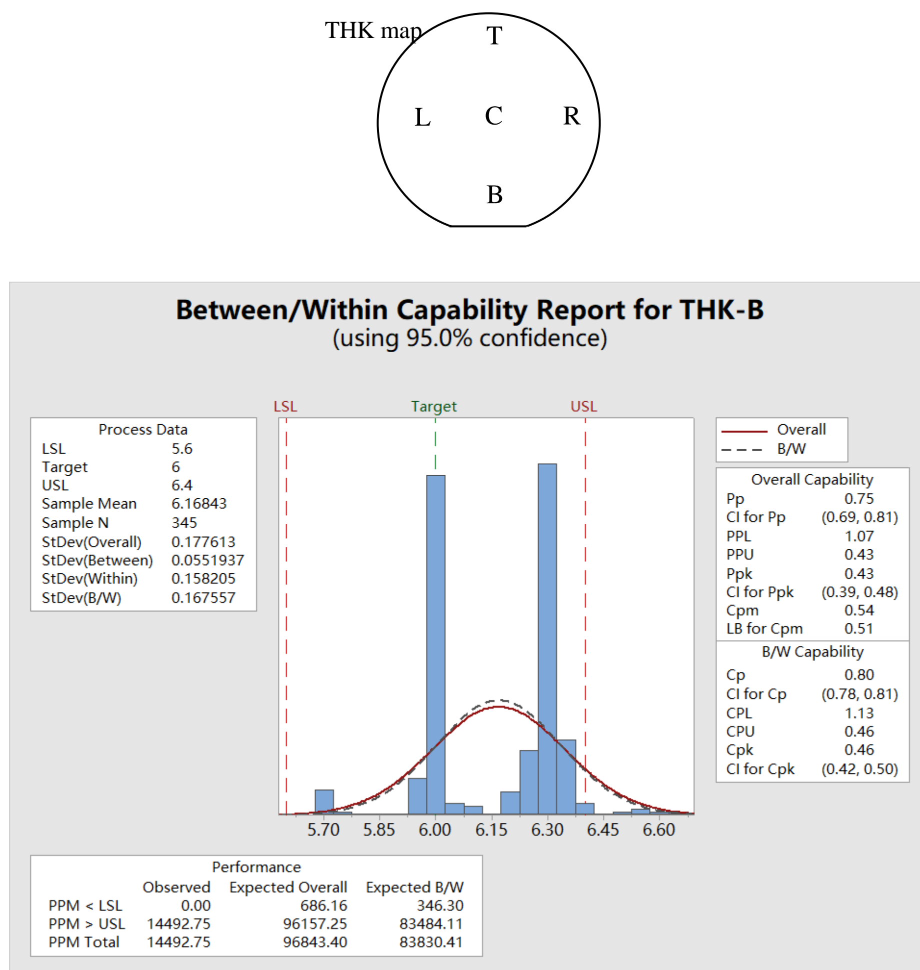


Figure 3. RI between/within capability sixpack report results for the 345 wafers.

In this case, there was only a one-to-one mapping between the PLC process capability and the RI in the short term, with it becoming unstable in the longer term. In Figure 3, the tests for specific causes were set to "six points in a row, all increasing or all decreasing". When the number of wafers exceeded 120 [120 pcs/15 (pcs/lot) = 8 days], the RI value was higher than the UCL (upper control limit). In other words, after eight days, the Cp of the RI was below 1.33 and the UCL of the RI exceeded 1.4632. At this point, the SiH_4 flow needed to be adjusted. The main reason for this may have been aging of the PECVD machine.

3.2. Thickness of the GeO_2-SiO_2 Optical Film

Figure 4 shows the thickness maps and histograms for the 345 wafers with the specification limits and targets for THK-B, THK-C, THK-T, THK-R and THK-L. The lower specification limit for the thickness was set at 5.6 µM. The upper specification limit was set at 6.4 µM and the thickness target was set at 6 µM. The data in Figure 4 does not have a normal distribution and there is an obvious divergence in the thickness of the 345 wafers. The thickness at points THK-B, THK-T, THK-R and THK-L was mainly distributed around 6.3 µM, while the thickness at THK-C was distributed around 6.0 µM. This is because the wafer was warped, resulting in a PECVD electrode gap between the showerhead reactor and the wafer. Wafer warpage is caused by insufficient cladding being deposited and annealed at 1100 °C, which is difficult to control.



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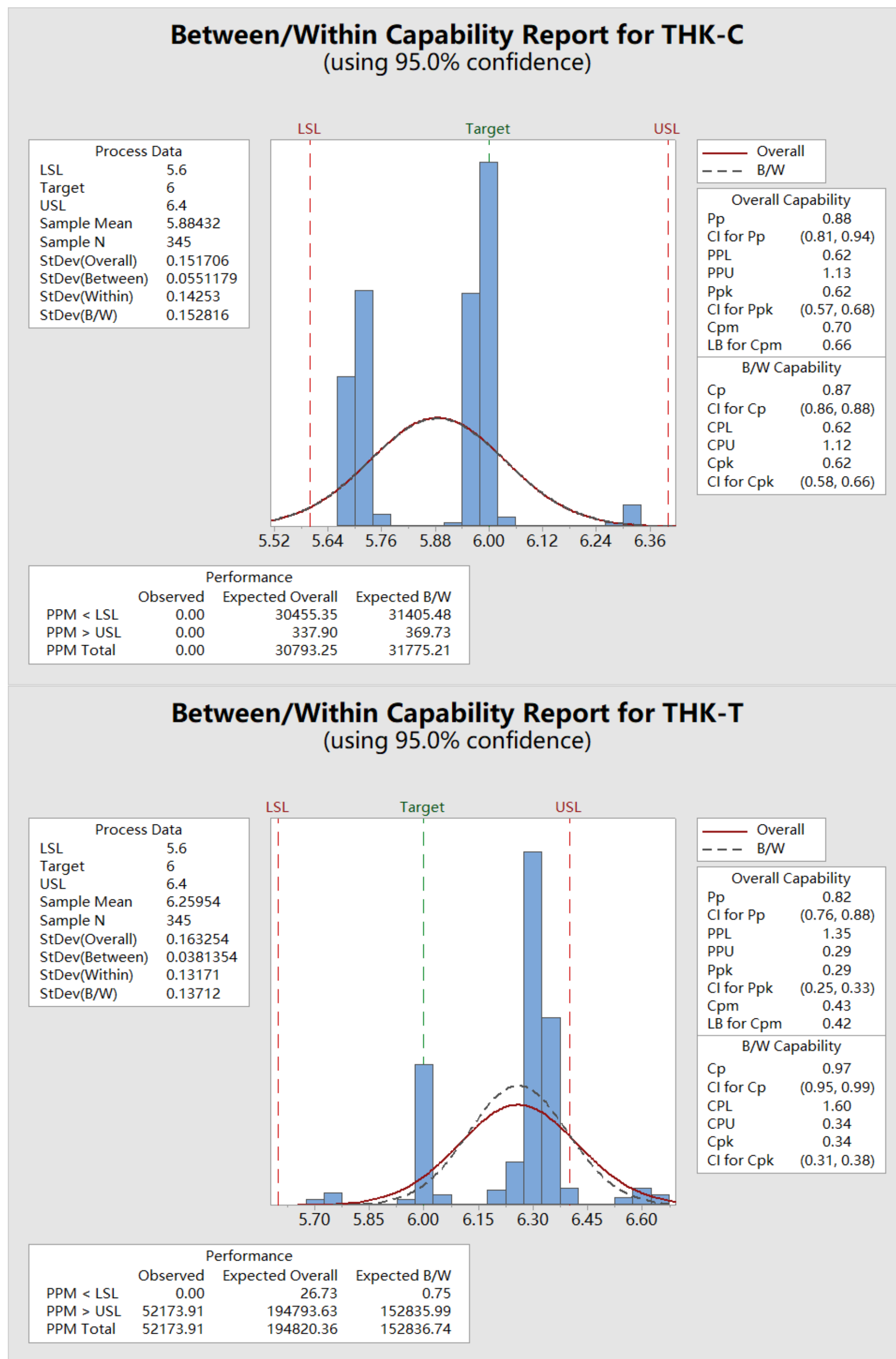

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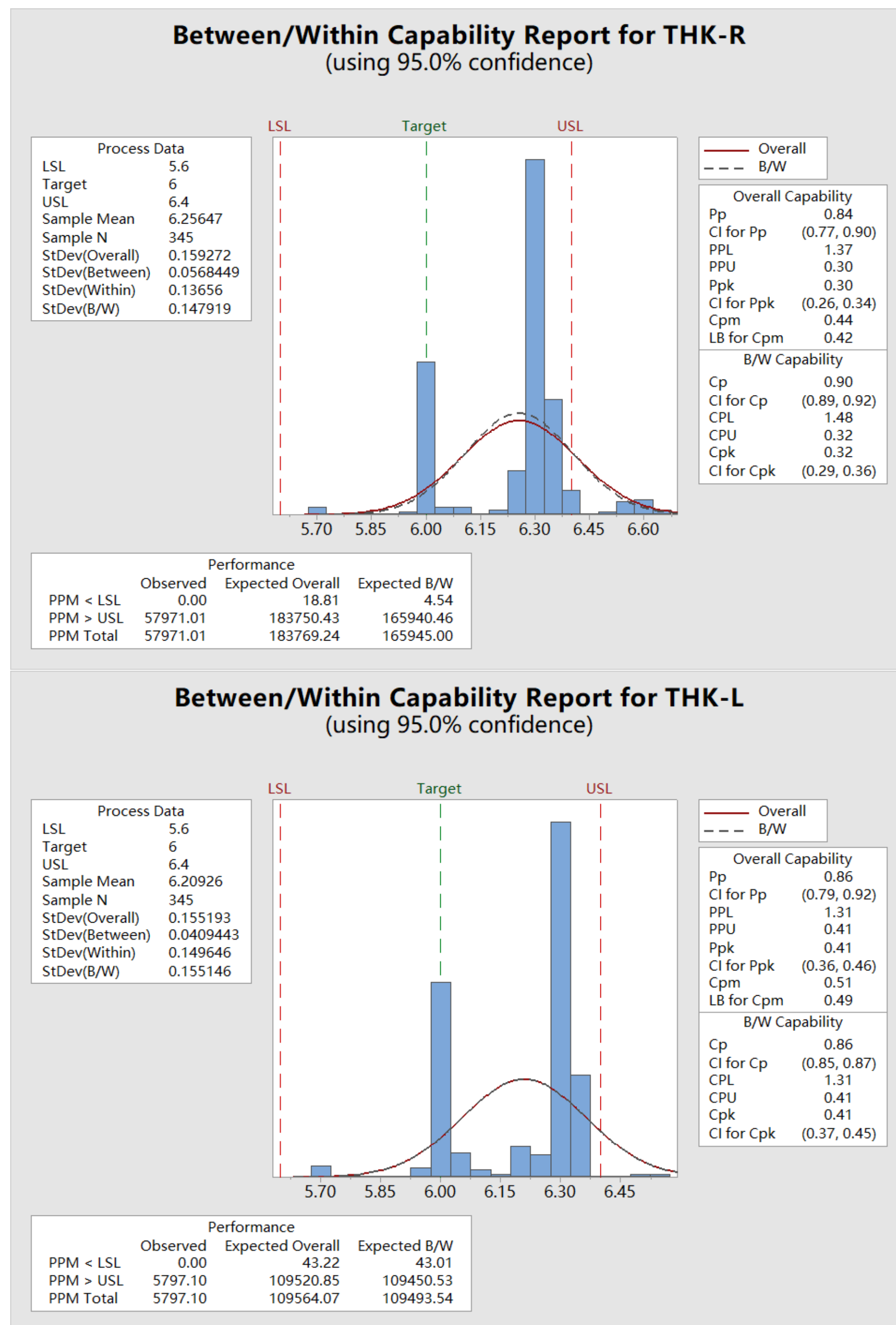

Figure 4. Thickness histograms for the 345 wafers for THK-B, THK-C, THK-T, THK-R and THK-L. LSL = 5.6 µM, USL = 6.4 µM and the target = 6.0 µM.

As shown in Figure 4, the Cp for THK-C, THK-T, THK-R and THK-L was greater than 0.83 and less than 1.00, while the Cp for THK-B was less than 0.83. According to SPC theory, when the Cp is less than 0.83, the process capability is in trouble. The thickness distribution at the five points on each wafer was not uniform, especially at point B. The reason for this was because the gas flow was not uniform.

Figure 5 shows the thickness RI between/within capability sixpack report for the 23 lots and Figure 6 shows the RI between/within capability sixpack report for the 345 wafers. For the data in Figures 5 and 6, p (the probability value test) was less than 0.05. This means that the thickness of the 23 lots or 345 wafers did not have a normal distribution because of the wafer warpage. However, the

average thickness of the silica optical film per wafer was higher than the thickness target of 6.0 µM. As shown in Figure 5, the Cp for the 23 lots exceeded 1.33, while the Cpk for the 23 lots was below 1.33. This means that the lot fabrication capability for thickness was under control, but that the mean thickness was higher than the thickness target. The gap between the electrode and the wafer needed to be adjusted. In Figure 6, the Cp/Cpk for the 345 wafers was lower than 0.83, indicating that the process needed improvement.

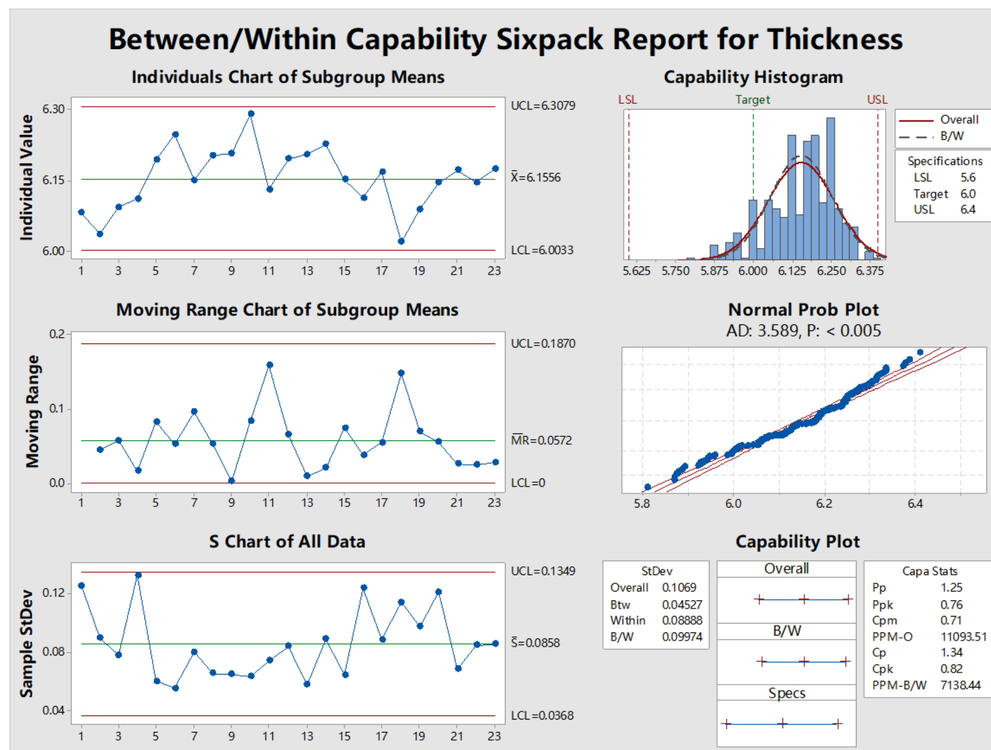

Figure 5. Thickness Between/Within Capability Sixpack for the 23 lots.

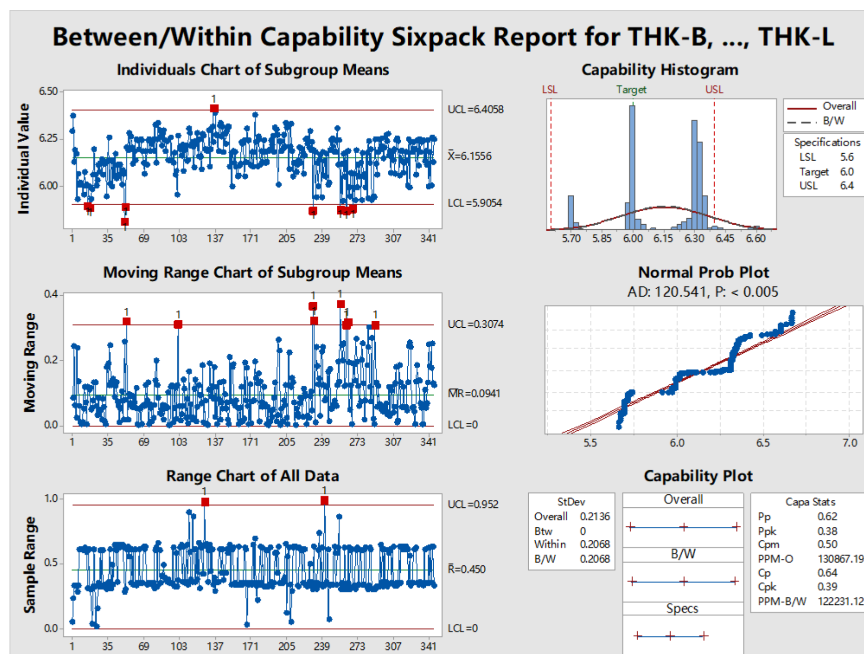

Figure 6. Thickness between/within capability sixpack report for the 345 wafers.

In this case, there was no one-to-one mapping between the PLC process capability and the thickness of the lots and of the wafers overall. According to Figures 5 and 6, the thickness at the five points on the wafer surface was uneven. In Figure 6, the tests for specific causes were set to "six points in a row, all increasing or all decreasing". When the number of wafers exceeded 256 [256 pcs /15 (pcs/lot) = 17 days], the thickness value was lower than the LCL (lower control limit). In other words, after 17 days, the gap between the electrode and the wafer needed to be adjusted.

3.3. Process Control Strategy

Lot fabrication stability is a key factor in defining the usability of various materials, environments and technologies for fabrication processes. For the PLC process capability analysis conducted in Sections 3.1 and 3.2, the optical waveguide specifications were determined according to variations in the fabrication process and, in theory, they obeyed a one-dimensional normal distribution. Unfortunately, there were many factors that were not adequately controlled. This means that the specific causes of variation had not been identified and eliminated, such as ambient temperature and relative humidity. According to Sections 3.1 and 3.2, if the process parameters of the PLC remained unchanged for a long time, the RI and thickness of the optical film wafers would move beyond their designated range. In this PLC production line, the GeH_4 (combined with 95% H_2) flow needed to be adjusted to stabilize the RI of the optical film after every 8 lots (or 8 days) and the electrode and wafer gap needed to be adjusted to stabilize the THK of the optical film every 17 lots (or 17 days).

4. Conclusions

Silica optical film specifications are determined on the basis of variations in the fabrication process. In this study, we have analyzed the mapping between the PLC process capability and the RI and thickness of lots of silica optical film wafers. In addition to internal factors, there are key external factors that need to be taken into consideration during the PLC process, such as temperature, relative humidity, process variation and machine aging. Statistical process control (SPC) can be used during the process to analyze the process capability and the lot fabrication stability, enabling real-time decisions to be made regarding whether to improve the fabrication process. Here, for instance, it was found that, on the studied PLC product line, the GeH_4 (combined with 95% H_2) flow needed to be adjusted to stabilize the RI of the optical film after every 8 lots, while the electrode and wafer gap needed to be adjusted to stabilize the THK of the optical film after every 17 Lots.

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Conflicts of Interest: The authors declare no competing financial interests.

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