applied sciences

MDPI

Article

Performance and Control Strategy of Real-Time Simulation of a Three-Phase Solid-State Transformer

Jorge Almaguer [1], Víctor Cárdenas [1,*], Jose Espinoza [2], Alejandro Aganza-Torres [3] and Marcos González [2]

[1] Centro de Investigación y Estudios de Posgrado, Facultad de Ingeniería, Autonomous University of San Luis Potosí, Av. Dr. Manuel Nava 8, Zona Universitaria, San Luis Potosí 78290, S.L.P., Mexico; jorge.almaguer@alumnos.uaslp.edu.mx

[2] Electrical Engineering Department, Universidad de Concepción, Edmundo Larenas 219, Concepción, Chile; Jose.Espinoza@udec.cl (J.E.); marcosigv@gmail.com (M.G.)

[3] Department of Electrical Power Engineering (EVS), Kassel University, Wilhelmshöher Allee 71, 34121 Kassel, Germany; alejandro.aganza@uni-kassel.de

* Correspondence: vcardena@uaslp.mx; Tel.: +52-444-826-2300 (ext. 6276)

Received: 14 January 2019; Accepted: 19 February 2019; Published: 23 February 2019

Abstract: This paper shows the real-time simulation of a three-stage three-phase solid-state transformer with an Opal OP5607 platform. The simulation model considers the complete electronic full-order circuit for the topology without the use of simplifications, such as average models or equivalent circuits for the coupling transformer and the input and output converters, which may neglect part of the dynamics of interest for the converter design. The simulation is made through an electronic hardware solver (eHS), which can achieve smaller solving times than the regular algorithms, allowing to reach the switching frequency rate for this converters. The simulation model takes the RTE-library which is used for DC-DC converters, with simple arrangements in order to operate with the topology.

Keywords: real-time simulator; solid-state transformer; LCL filter

1. Introduction

Real-Time Digital Simulation (RTS, abbreviation recommended by IEEE) has been widely used for the studies on electrical power systems with a cornerstone role on the development and planning of the electrical power system. In recent years, the increase in the computational capacity and the appearance of high-speed platforms have provided a powerful tool for the study of power electronic converters, especially in the areas of rapid prototyping, control tests, phenomena investigation, fault and protection studies, among others.

Typical offline simulations are performed to obtain a valid result regardless time, holding any subprocess in order to achieve the output calculation. Conversely RTS incorporate high-speed dedicated processing hardware to solve the system model variables, with a fixed time-step within the same time in the reality [1], also the simulation algorithm operates as the physical system would.

Because of this RTS allow a reduction in simulation times of complex systems; offline simulations can take hours to deliver a few seconds of the system dynamics, while in real-time simulators one simulation second corresponds to an operating second of the physical system.

RTS operates at a predetermined simulation time-step intervals (T_s), in which, the algorithm gets the inputs and proceeds to perform all the necessary calculations (control algorithms, model calculations) in order to write all the outputs. For industrial applications a 50 µs time-step is an accepted target to achieve an accurate representation for a physical system over a frequency range up to 3 kHz [2].

Due to the discrete computing time, two scenarios based on the fixed time T_s and the complexity of the model may occur [3]. The first one is when the real-time algorithm can find a solution in T_s meaning that the selected time-step is enough for the real-time execution mode. A second scenario happens when the given T_s is smaller than the necessary time to obtain a valid response, with the need to extend the solving time algorithm to the next time-step generating an overrun, loosing real-time synchronization with an offline simulation.

All this gives RTS the capability to recreate power electronic converter voltages and currents signals with a high-accuracy level within frequency range [2]. Making posible to do further advanced studies without the need to have a physical prototype. Adding also a security margin in the case of control strategies and fault protection schemes that will be implemented physically, bringing the possibility of having a look of critical operating points of the electronic converters without involving any risk.

One of the power electronics topologies that has received attention in many research fields for its capabilities is the solid-state transformer (SST), whose characteristics make it feasible to be applied in the modern power electric due to its capability to integrate distributed energy resources (DER), can also operate as a power management system in smart grid applications [4–6], interconnecting wind and solar PV [7–9], for locomotive traction [10,11] and as a scheme that can provides ancillary services to the distribution network like power factor correction, reactive power compensation, harmonic mitigation, among others [12,13].

SST are power electronics converters which can interface two AC voltage sources providing galvanic isolation through a high frequency DC-DC link, achieving a notorious reduction in the volume and weight of the coupling transformer. Because of this, the real-time simulation of SST requires a very small T_s for the fixed-step solvers, which in most cases is not feasible for RTS.

To overcome this issue, strategies have been reported like the use of Dynamic Average Models (DAM) [14,15], in which the fundamental system dynamic is represented through ideal voltage and current sources, neglecting all the other components. Despite the fact these components are not necessary for control design, this simplification causes the loss of realism in the use of RTS. On the other hand techniques like hardware emulation like shown in [16,17] can generate a highly accurate machine-state based model for a VSC converter, however the complexity of the implementation increases.

Real-time implementation for a full-circuit model of the SST is a good method to test in advance control schemes, soft startup strategies, transient on-state switching currents, resonance points, among others; which is of particular interest in the design of these type of higher frequency converters, due to the use of reduced coupling inductances which commonly leads to the appearance of inrush currents.

DAM models neglect the switching dynamics and preserve the fundamental signal component, considering the converter as the union of continuous current and voltage controlled sources. Nevertheless this is based on the assumption that the commutation effect has low impact on the fundamental component dynamics. In the case of higher power ratings, where low commutation switching frequency is used, these type of models reduces their accuracy. Besides, there are certain types of transient effects, resonance and other phenomena that can not be recreated through fundamental DAM models.

The aim of the paper is to show the implementation of a three stage solid-state transformer in an Opal-RT platform, using an electronic hardware solver (eHS), in order to achieve very small simulation time-steps (≈200 ns) for the electric circuit, adapting the RTE-Library of the Opal software in conjunction with SimPowerSystems library in Matlab for the topology.

The paper is organized as follows: in Sections 2 and 3 the SST topology, control strategy and the simulation parameters used for the simulation are shown; Section 4 introduces the RTS platform, the simulation scheme and the implementation of the circuit; showing the modulation schemes and its

overall operation. In Section 5 the RTS results for the topology are depicted, finally in Section 6 the concluding remarks are presented.

2. SST Topology

The Figure 1 shows the three-phase SST considered; the converter is integrated by three conversion stages (VSC_i, DAB and VSC_o). VSC_i operates as an Active Front End (AFE) and regulates the voltage across the capacitor C_i. The DAB (Dual Active Bridge) stage is a DC-DC high/medium frequency isolated converter operating in a phase shifted modulation scheme (CPS), as an effect of the higher commutation frequency the magnetic coupling transformer reduces its volume and size. Finally VSC_o operates as an inverter to achieve the power transfer to the output feeders. Due to the structure of each module, active power transfer can be transferred bidirectionally, and the VSC converters add the capabilities to develop ancillary functions as reactive power compensation, harmonics mitigation, power factor correction, among others.

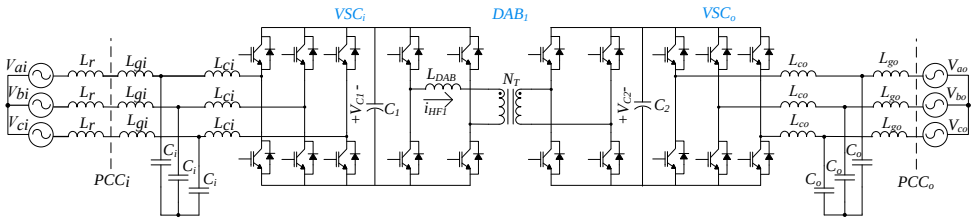

Figure 1. Three-Stage SST.

In addition, the incorporation of the SST to the AC networks is using an LCL filter. The grid side inductor is estimated from the grid short circuit power (S_{CC}), and all the inductor elements associates a series loss resistance estimated for a quality factor $Q_f \geq 20$. The values of the filter inductors are chosen to achieve the direct location of the resonance frequencies of the filter (f_1 and f_2) and achieve the proposed nominal power for the converter which is 1 MW.

3. Control Strategy

One advantage of the RTS is the capability to test control strategies in similar conditions of a physical application, incorporating effects to the control schemes like saturation, data acquisition delays, sampling process and discretization. For this reasons RTS simulations have a high acceptance level for technicians and engineers, allowing to evaluate performance and stability conditions previously to use an experimental or real system.

The Figure 2 shows the dq reference frame control strategy for the SST [18], each one of the control stages achieves its own control task independently without feedback from the other stages due to the dynamic decoupling caused by the proper selection of the capacitors C_1 and C_2. For VSC_i the control tasks are the regulation of the voltage across the capacitor C_1 (V_{C1}), the reactive compensation to the input feeders and to provide the operating VARs for the input LCL filter. The DAB converter regulates the voltage in the capacitor C_2 (V_{C2}); and the VSC_o converter provides the total active power transfer for the entire topology, the reactive compensation to the output AC source, as well as supplying the operating VARs for the output LCL filter.

For VSC_i the control scheme operates in two separate levels, one for each control component (U_i^d, U_i^q). The upper level has two interconnected loops, the outer loop regulates the voltage V_{C1} providing the inner superior loop the reference I_d^*, for the reference for the inner inferior loop Equation (1) is used. The control for VSC_o operates in a similar way and have the same structure; however, only the inner loops are required and their references are also calculated by (1). The DAB control operates as a single-loop PI voltage control, and the processing of the voltage error gives the θ angle to the modulation strategy.

For $VSC_{i,o}$ the control bandwidth response is decoupled from the filter resonance frequencies f_1 and f_2 in order to avoid resonance to the grid; the parameters used in the simulation are shown in Table 1.

$$\mathbf{I} = \begin{bmatrix} I_{i,o}^{d*} \\ I_{i,o}^{q*} \end{bmatrix} = \frac{-2}{\left(V_{i,o}^{d}\right)^2 + \left(V_{i,o}^{q}\right)^2} \begin{bmatrix} V_{i,o}^{d} & V_{i,o}^{q} \\ V_{i,o}^{q} & -V_{i,o}^{d} \end{bmatrix} \begin{bmatrix} P_{i,o}^{*} \\ Q_{i,o}^{*} \end{bmatrix} \tag{1}$$

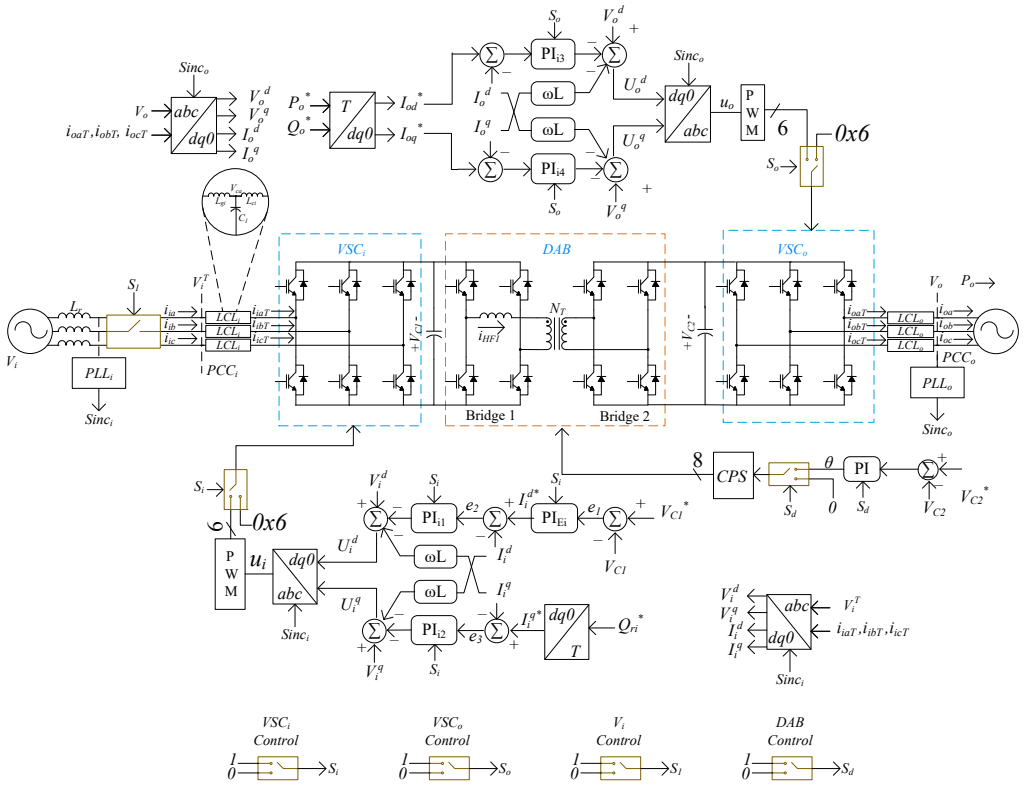

Figure 2. Control scheme.

Table 1. Simulation parameters.

	Parameter	Symbol	Value	Units
Grid	Short-circuit power	S_{CC}	10	MVA
	Grid inductance	L_r	60.4	µH
	Voltage 3ϕ	V_i	220	V_{L-L}
	Voltage 3ϕ	V_o	220	V_{L-L}
	Grid frequency	f_{grid}	50	Hz
LCL Filter	LCL converter side inductor	L_{ci}	150	µH
	Operating VARS 3ϕ for L_{ci}	$Q_{Lci3\phi}$	240	kVAR
	LCL grid side inductor	L_{gi}	15	µH
	Operating VARs 3ϕ for L_{gi}	$Q_{Lgi3\phi}$	243	kVAR
	LCL Capacitor	C_i	432	µF
	Complete LCL operating VARs	LCL_{VAR}	243.1	kVAR
Frequencies	Resonance frequency	f_1	875	Hz
	Resonance frequency	f_2	1.075	kHz
	Outer loop bandwidth	F_o	35	Hz
	Inner loop bandwidth	F_i	450	Hz
Converter	Total apparent power	S_t	1.02	MVA
	Capacitor	C_1	2600	µF
	Link inductor	L_{DAB}	0.005	mH
	Capacitor	C_2	1200	µF
	$VSC_{i,o}$ Switching frequency	f_{sw}	2.15	kHz
	DAB Switching frequency	f_{sDAB}	5	kHz
	DC voltages	$V_{C1,2}$	1000	V

4. Digital Real-Time Simulator

The RTS platform is shown in Figure 3, which incorporates two simulation modules OP5607; each one has an FPGA Virtex 7, including 256 I/O ports per module, with RJ45 and DB37 connections sockets, also integrating BNC output ports for signal monitoring. Each OP5607 has 4-core Xeon E5 processor, with an operating frequency of 3.2 GHz, 32 GB of DRAM, and 512 GB in SSD, the graphical user interface is madeRT-LAB V11.0, and the simulation model is built with in Matlab Simulink.

Figure 3. RTS simulator.

4.1. Simulation Circuit

Figure 4 shows the Simulink model and its components, which consist in two blocks created according to [19]. SM_Circuit corresponds to the master block which is loaded to the OP5607; usually this block has feedback to the graphical user interface (SC_GUI); however in this case the outputs are directly assigned with the block "To Analog Outputs" in SM_Circuit.

The SC_GUI block is used to have a real-time link to the control gains for PI_{i1}, PI_{i2}, PI_{i3}, PI_{i4}, and the setpoint references (Q^*_{ri}, V^*_{C1}, V^*_{C2}, Q^*_o, P^*_o); which in conjunction with the activation signals (S_i, S_o, S_d), brings the capability to program soft start-up techniques, trajectory planning, among others. Besides all this SC_GUI also controls the signals multiplexor to the external oscilloscope.

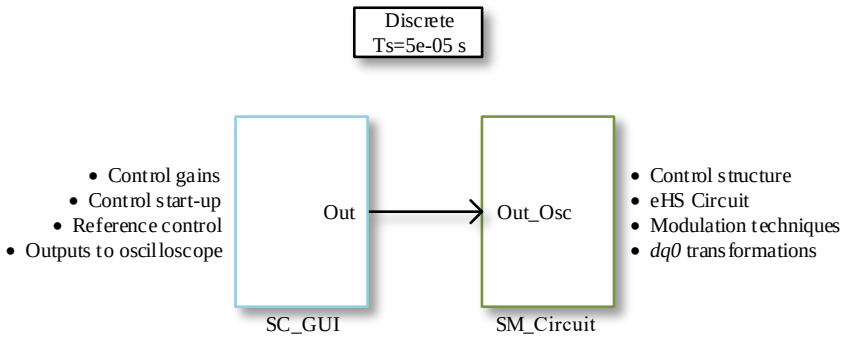

Figure 4. Circuit structure for real-time simulation.

4.2. eHS Circuit

The main challenge to simulate the SST topology is the DAB switching frequency; trough performance tests for a VSC converter operating as an AFE the simulation time-step was fixed in $T_s = 50$ µs; considering a switching frequency for the DAB $f_{sDAB} = 5$ kHz meaning that the circuit will compute four samples per-cycle for the modulation technique, which in fact meets the Nyquist criterion. Therefore, this strategy is not suitable for the simulating an SST generating overruns under transient conditions, thus a smaller time-step is needed to accurately represent electrical system dynamics.

A solution to reduce the RTS time-step is the use of an electric Hardware Solver (eHS), which allows the parallel simulation of electric circuits using the FPGA on the OP5607 with a much smaller time-step. The eHS uses the Pejovic method to solve the electric circuit in parallel with the main process [20].

This circuit is programmed in the eHSx64 block, which is located in the Opal-RT libraries and handles the writing and communications of the electric circuit between the FPGA and the main algorithm. Its simulation parameters are listed in Table 2.

Table 2. eHS Parameters.

Parameter	Value
Number of Inputs	32
Number of Outputs	32
Number of Switches	64
Maximum number of states	150
Calculation power	25.6 GFLOPS
Solving time	≈200 nS

In addition, the eHS block can operate with the Loss Compensation Algorithm (LCA), which allows the simulation to compensate the power losses that might occur by the Pejovic method. Considering all these, the eHS circuit is made in Simulink based on [21]. An advantage in the use of eHS in this configuration is the simplicity when the model is created in comparison with other FPGA programming methods as in [16], since the SimPowerSystem electrical model is automatically deployed to the FPGA using the RT-LAB.

The transformer characteristics are calculated using [22], and the fixed time-step for the eHS circuit T_{eHS} is optimized each time-step for the algorithm. Also an advantage on the eHS simulation is the use of only one OP5607 core in comparison with [14], in which the circuit is split into several subsystems to divide the computational load among all the available cores.

4.3. Modulation Schemes

Another challenge to simulate in real-time the SST is the control of the switching devices; for VSC_i and VSC_o the modulation strategy is carried out by a SPWM technique [23], in which three modulating sine-waves signals shifted $\frac{2\pi}{3}$ rad among them are compared with a triangular carrier, the result per modulating signal controls a branch of the converter. However the generation of the structure by using Simulink blocks like triangular generators and comparators causes the comparison result in being linked to the sampling time T_s; meaning that only when a T_s rising edge occurs the switching state will change, with the possible loss of commutation states as shown in Figure 5.

One possible solution is the use of the RTE library, which allows the simulation algorithm to generate transition states between computation times T_s. However the use of RTE-Comparator and RTE-Not blocks to generate the PWM signal only allows to create one transition event per time-step T_s; to solve this the RTE library incorporates the RTE-SPWM block, whose operation principle is also shown in Figure 5.

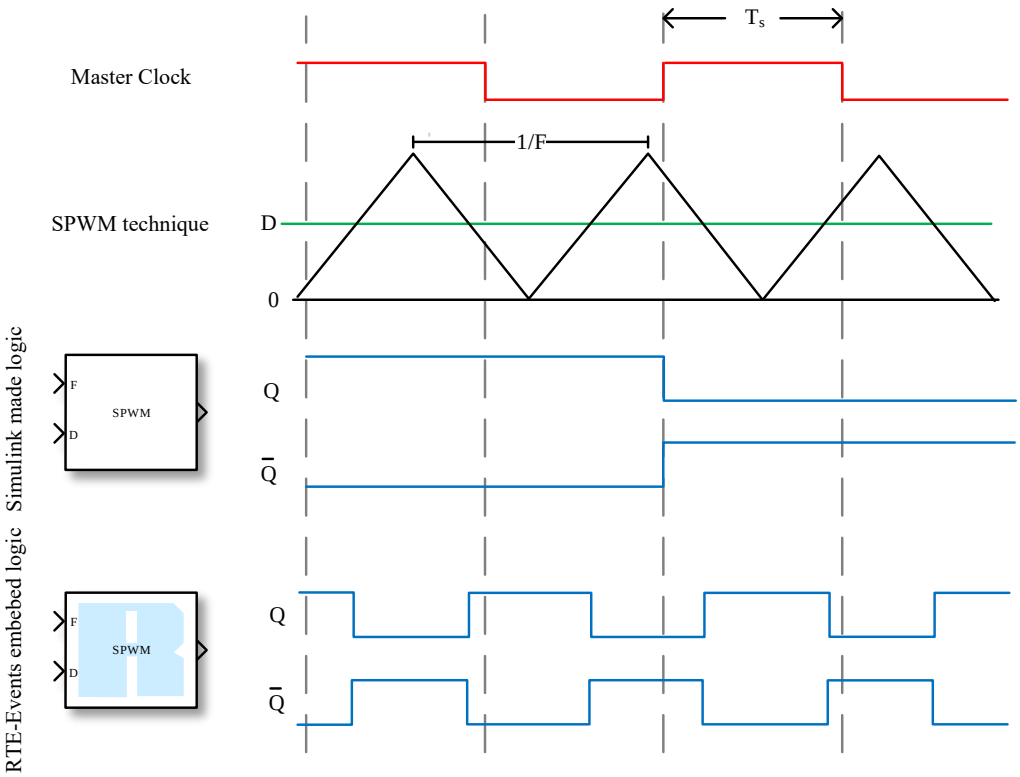

Figure 5. RTE-SPWM block and operation.

However the RTE-SPWM block is optimized for DC-DC converters, and the simulation technique operates only positive voltages for the triangular wave. Figure 6 shows an arrangement of the RTE-SPWM block in order to handle the negative half-cycle of the carrier.

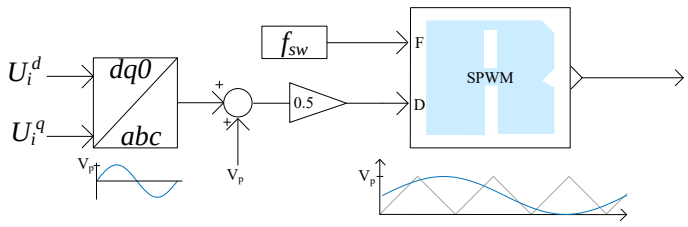

Figure 6. RTE-SPWM block and operation.

For the DAB converter the modulation scheme is based on a conventional phase-shift, consisting of two 50% fixed duty cycle square-waves signals shifted θ degrees among them; the proposed modulation scheme is shown in Figure 7. A block RTE-SPWM with a 50% ratio ($D = 0.5$) is used to generate the control signals, and the θ regulation is made through RTE-Delay buffers. However the use of these blocks only allows for positive values; for negative degree values for θ (inverted power flow) the input is saturated to zero, to solve this for $\theta \geq 0$ the switching signals are delayed on the secondary bridge and for $\theta < 0$ values the primary bridge control signals are lagged. The sign and conversion from degrees to time are solved with a gain $K = \frac{1}{2\pi f_{sDAB}}$, and all the logic functions are made through RTE-Blocks.

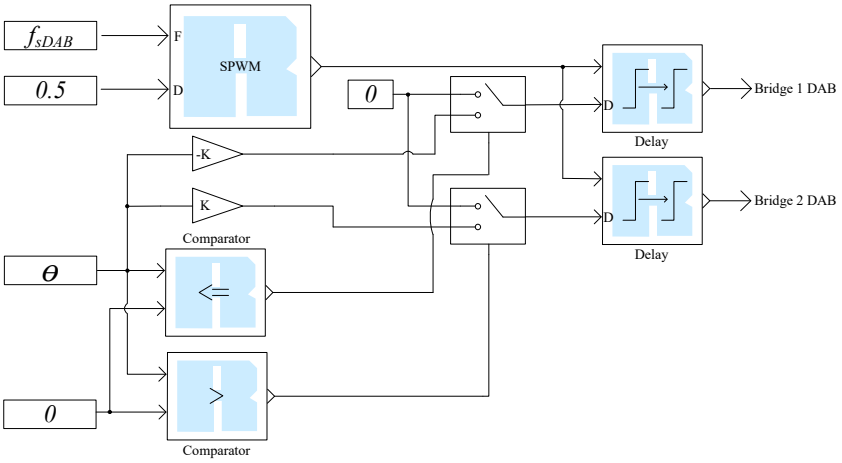

Figure 7. Proposed DAB modulation scheme.

4.4. PI Controllers

Figure 8 shows the scheme for the PI controllers used in the RTS, with an advantage in comparison with the traditional Simulink PI blocks due to the capability to modify the control gains in real-time during the simulation, being helpful during the start-up operation, also if control trajectory planning will be applied. It is worth highlighting that the control strategy is made in a $dq0$ referential frame, because of this also a PLL was used on the $PCC_{i,o}$ in order to have the signal references for the $dq0$ transformations.

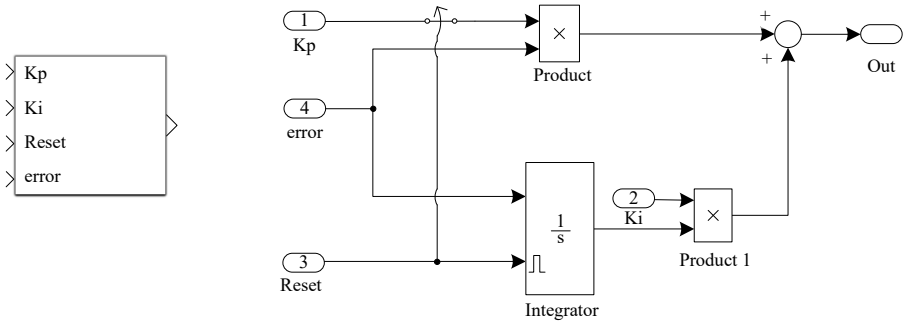

Figure 8. Proposed PI controller scheme.

5. Real-Time Operation

One of the main differences with offline simulations is that the operation should be treated as a physical system to avoid possible overruns; hence a soft-start strategy is needed in order to avoid inrush voltages and currents.

The operation begins with the VSC_i converter operating as a three-phase diode rectifier, with a voltage in C_1, the DAB converter operates with an angle $\theta = 0$, and VSC_o is needed to transfer 0 W.

Simulation Results

In order to corroborate the operation of the implemented topology, the control is asked to follow a reference from 0 W to 500 kW. The results are shown below, in all the cases currents have an output gain $K_o = \frac{1}{10}$, and the power signals are escalated by a factor $K_f = \frac{1}{1000}$.

Figure 9 shows tracking of the control scheme for the active power reference P_o^*, with a overshoot corresponding to the 12%, this value can be reduced by the use of trajectory planning if higher regulation is needed for the application on critical loads; and the reactive power is compensated at the input and output PCC, as shown achieving a power factor $P_F = 1$.

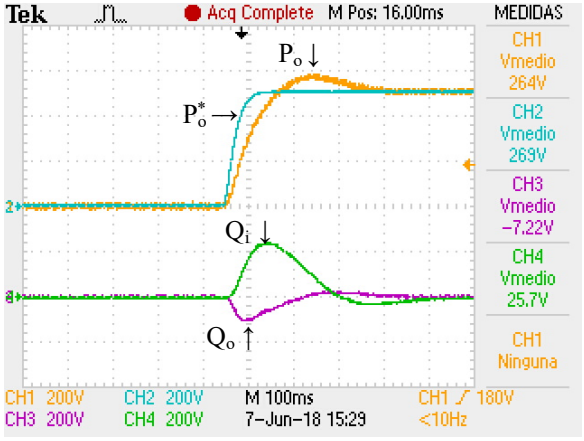

Figure 9. Total active and reactive power.

In Figure 10 the transient behavior of the input currents at the PCC_i and the voltage V_{C1} is shown. Having a smooth evolution on the current dynamics is desired for a physical application, and for the V_{C1} exists a 20% of drop in the DC value during the transition.

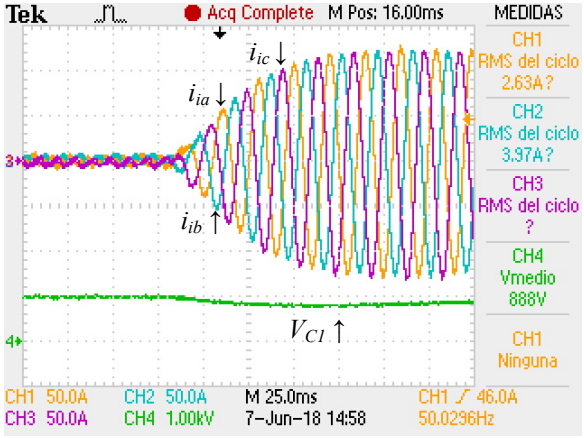

Figure 10. PCC_i currents and V_{C1}.

Figure 11 presents the current signals between the converter VSC_i and the LCL filter, with the currents without the mitigation effect of the LCL filter, showing the capability of the RTS to recreate physical signals with a high fidelity in comparison with fundamental DAM models which the signal will be the same escalated by the filter gain without any ripple, and in order to recreate switching effects there is the need to create more complex models to emulate the switching frequency impact.

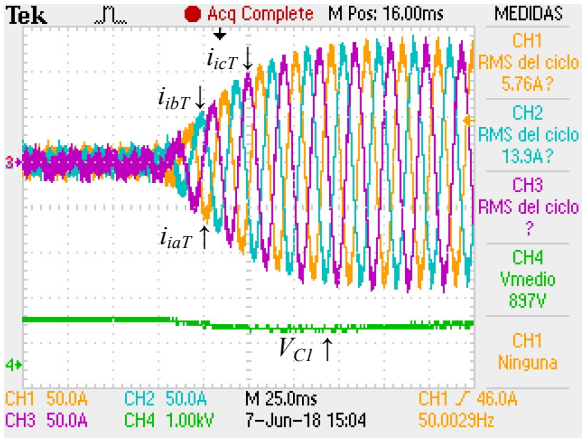

Figure 11. VSC_i input currents and V_{C1}.

In Figure 12 the input voltages at the PCC_i are shown, the signal VSC_i is used to synchronize the voltage signals with the active power step, not finding any disturbance during the transient condition.

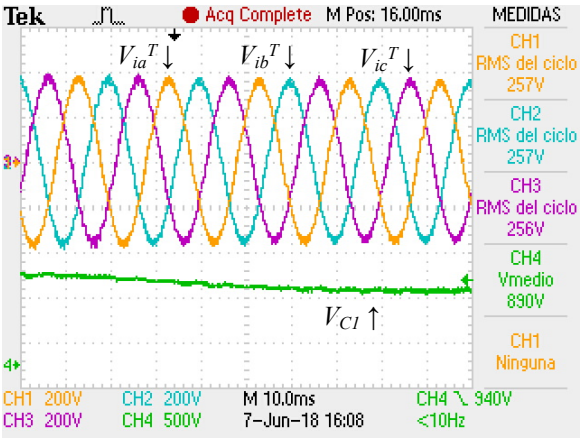

Figure 12. PCC_i voltages and V_{C1}.

In Figure 13 the VSC_i and VSC_o control signals during the transient are shown, as seen all the references reach the steady-state without saturation, with a smooth behavior.

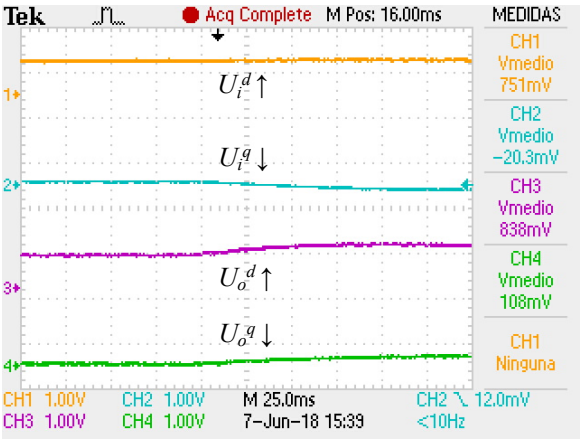

Figure 13. VSC_i and VSC_o control signals.

Figure 14 shows the DAB control signal θ also with a transition without saturation, and its effect over the voltage V_{C2} as shown in the inferior trace.

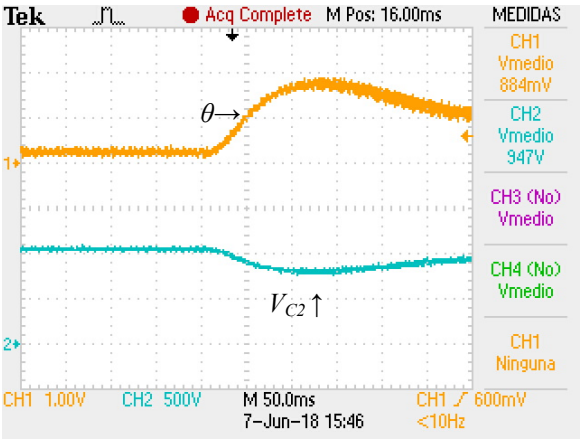

Figure 14. DAB control signal (θ) and V_{C2}.

The currents at the PCC_o are shown in Figure 15, with a desirable behavior and an output total harmonic distortion $THD = 0.98\%$ in steady state, which is adequate to achieve the interconnection with the grid.

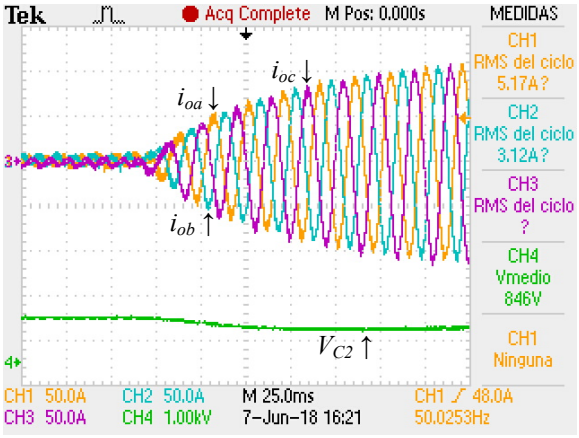

Figure 15. PCC_o currents and V_{C2}.

Figure 16 shows the output currents of the VSC_o converter, in this case is noticeable the mitigation effect of the LCL filter, in comparison with the currents after the LCL filter in Figure 15.

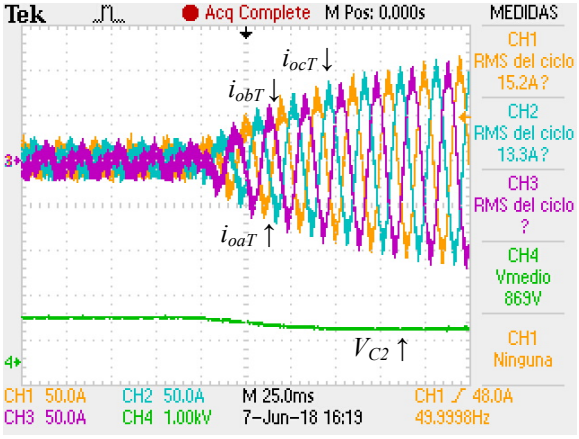

Figure 16. VSC_o currents and V_{C2}.

Figure 17 shows the voltages at the PCC_o, as in PCC_i the signal V_{C2} is used to synchronize the voltage signals with the power transient, and in the same way have a behaviour without finding any disturbance.

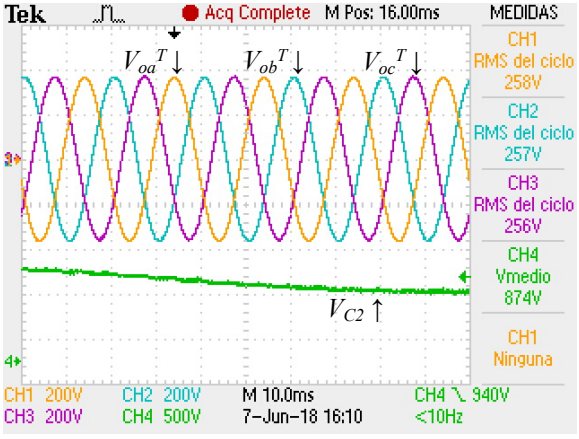

Figure 17. PCC_o voltages and V_{C2}.

In Figure 18 the control is needed to follow beforehand a reference $P_o^* = 700$ kW, and suddenly this reference is changed to $P_o^* = -700$ kW, showing how the SST is capable of inverting the power flow among the three-phase AC sources.

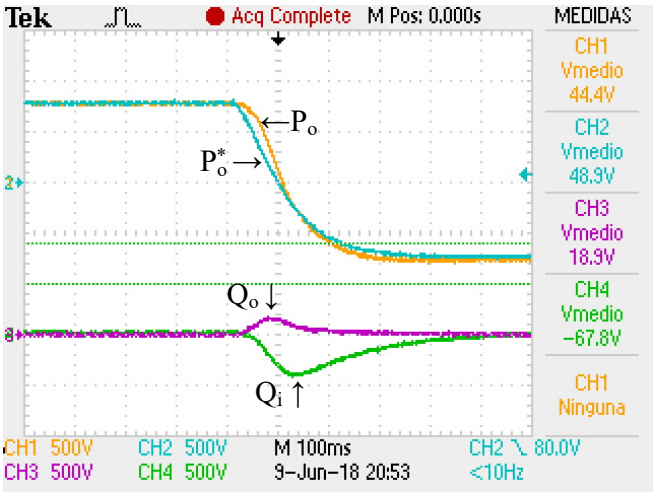

Figure 18. Power tracking and active regulation power flow inversion.

The Figure 19 presents the θ angle for the power inversion showing the sign change due to the power flow inversion, which is processed by the shifting scheme shown in Figure 7 changing the delay through the bridges, achieving the sign transition.

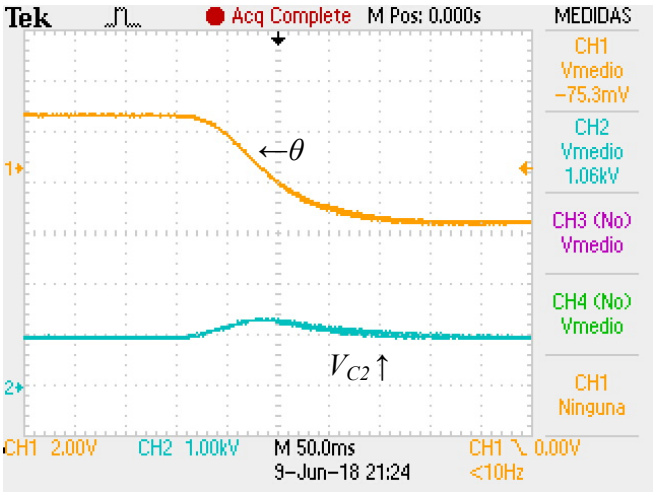

Figure 19. DAB control signal (θ) and V_{C2}.

Figures 20 and 21 shown the current before and after of the LCL filters at nominal power (1 MW) and the current at the capacitor C_1 for phase a, at nominal power shown. This type of scenario can be useful in the LCL filter design, in order to corroborate current rates for design purposes, which is feasible due to the eHS capability to reproduce commutation effects. Simulations based on DAM models neglect these components and they would only show the average value of the signal without the current ripple. This restricts the possibility to observe the performance of the LCL filter over the currents.

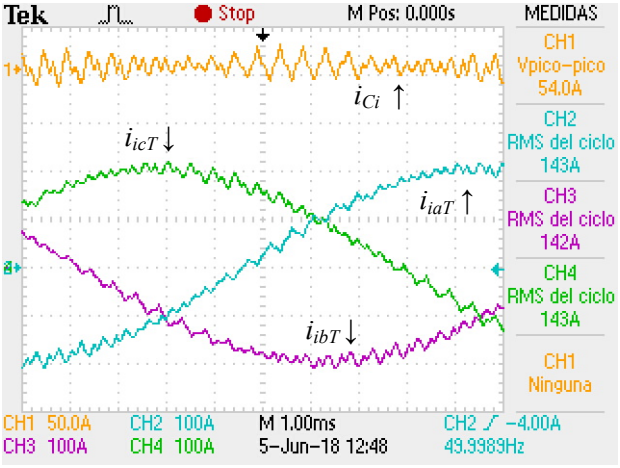

Figure 20. Input currents between LCL filter VSC_i.

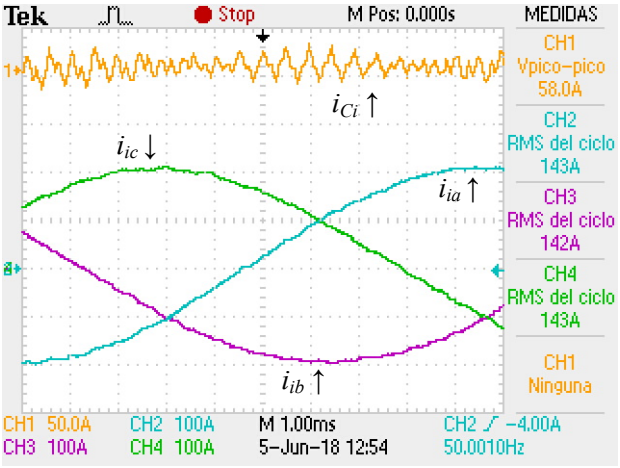

Figure 21. Input current at the PCC_i.

Finally in Figure 22 the *a* phase PWM signal showing how the RTS reproduces the commutation effect.

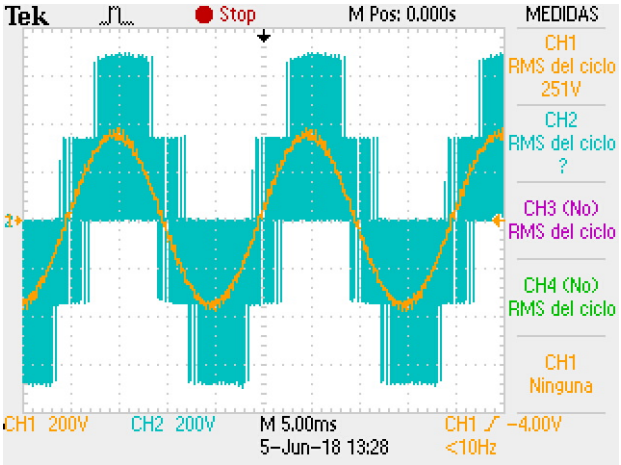

Figure 22. PWM and voltage from phase *a*.

One of the advantages of implementation of the methodology developed is the reduction of the computation time necessary to enhance the simulation, this can be measured through the graphical

user interface on the RT software. The principal subprocess are shown in Table 3 according to each time-step consumption percentage.

Table 3. Time used per T_s.

Parameter	Time [µs]	T_s [%]
Data acquisition	0.08	0.16
Major computation time	13.24	26.48
Minor computation time	0.18	0.36
Opctrl recv (EHS)	0.1	0.2
Execution cycle	14.29	28.57

* T_s = 50 µs.

6. Concluding Remarks

This paper presented the real-time digital simulation of a three-stage three-phase solid-state transformer in an OPAL-RT platform, in which the interconnection to the grid was made achieved through an LCL filter, using an eHS in order to have very small simulation steps for the circuit solving, without the need to use circuit simplifications.

The use of the RTE-Library in collaboration with the eHS solver allows the simulation to achieve higher frequencies, and the proposed structures are a simple way to operate the DC-DC RTE blocks in the SST scheme.

The use of eHS for the electric circuit shows all the frequency components involved in the operation of the topology, achieving a realistic behavior to the simulation and adding the capability to monitoring high frequency behavior in comparison with DAM models.

The implementation of the phase-shift control of the DAB converter with the proposed scheme allows the system to operate in a bidirectionally way.

The control scheme can achieve a proper performance during the entire operation and transients, incorporating also saturation effects. Operating within real physical conditions which are possible to take into account due to real-time simulation.

RTS for the SST had a proper operation not showing overruns and with a total execution time of 28.57% of the time-step, which according to [2] is appropriate for industrial applications.

Author Contributions: Formal analysis, J.A.; Investigation, J.A.; Methodology, A.A.-T. and M.G.; Project administration, V.C.; Resources, J.E.; Software, M.G.; Supervision, J.E.; Writing—original draft, J.A.; Writing—review and editing, V.C. and A.A.-T.

Funding: This research received no external funding.

Acknowledgments: The authors wish to thanks the financial support from UASLP/AG-038/18, CONICYT / FONDEQUIP / EQM140148, CONICYT / FONDAP / 15110019, and CONICYT / BASAL / FB0008.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Bélanger, J.; Venne, P.; Paquin, J.N. The what, where, and why of real-time simulation. *Planet RT* **2010**, 37–49. Available online: https://www.opal-rt.com/wp-content/themes/enfold-opal/pdf/L00161_0436.pdf (accessed on 23 February 2019).
2. Kuffel, R.; Forsyth, P.; Peters, C. The Role and Importance of Real Time Digital Simulation in the Development and Testing of Power System Control and Protection Equipment. *IFAC-PapersOnLine* **2016**, *49*, 178–182. [CrossRef]
3. Strasser, T. Real-Time Simulation Technologies for Power Systems Design, Testing, and Analysis. *IEEE Power Energy Technol. Syst. J.* **2015**, *2*, 63–73.
4. She, X.; Yu, X.; Wang, F.; Huang, A.Q. Design and Demonstration of a 3.6-kV-120-V/10-kVA Solid-State Transformer for Smart Grid Application. *IEEE Trans. Power Electron.* **2014**, *29*, 3982–3996. [CrossRef]

5. Pinto, S.F.; Mendes, P.V.; Silva, J.F. Modular Matrix Converter Based Solid State Transformer for smart grids. *Electr. Power Syst. Res.* **2016**, *136*, 189–200. [CrossRef]
6. Huang, A.Q.; Crow, M.L.; Heydt, G.T.; Zheng, J.P.; Dale, S.J. The Future Renewable Electric Energy Delivery and Management (FREEDM) System: The Energy Internet. *Proc. IEEE* **2011**, *99*, 133–148. [CrossRef]
7. Parreiras, T.; Machado, A.A.P.; Amaral, F.; Lobato, G.; Brito, J.A.S.; Cardoso, B. Forward Dual-Active-Bridge Solid State Transformer for a SiC-Based Cascaded Multilevel Converter Cell in Solar Applications. *IEEE Trans. Ind. Appl.* **2018**, *54*, 6353–6363. [CrossRef]
8. Gao, R.; She, X.; Husain, I.; Huang, A.Q. Solid-State-Transformer-Interfaced Permanent Magnet Wind Turbine Distributed Generation System with Power Management Functions. *IEEE Trans. Ind. Appl.* **2017**, *53*, 3849–3861. [CrossRef]
9. Syed, I.; Khadkikar, V. Replacing the Grid Interface Transformer in Wind Energy Conversion System with Solid-State Transformer. *IEEE Trans. Power Syst.* **2017**, *32*, 2152–2160. [CrossRef]
10. Drabek, P.; Pittermann, M.; Los, M.; Bednar, B. Traction Drive with MFT-Novel Control Strategy Based on Zero Vectors Insertion. *IFAC Proc. Vol.* **2014**, *47*, 11968–11973. [CrossRef]
11. Bednar, B.; Drabek, P.; Pittermann, M. The comparison of different variants of new traction drives with medium frequency transformer. In Proceedings of the 2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Anacapri, Italy, 22–24 June 2016; pp. 1172–1177. [CrossRef]
12. Costa, L.F.; Carne, G.D.; Buticchi, G.; Liserre, M. The Smart Transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid. *IEEE Power Electron. Mag.* **2017**, *4*, 56–67. [CrossRef]
13. Milani, A.A.; Khan, M.T.A.; Chakrabortty, A.; Husain, I. Equilibrium Point Analysis and Power Sharing Methods for Distribution Systems Driven by Solid-State Transformers. *IEEE Trans. Power Syst.* **2018**, *33*, 1473–1483. [CrossRef]
14. Martinez-Velasco, J.A.; Alepuz, S.; González-Molina, F.; Martin-Arnedo, J. Dynamic average modeling of a bidirectional solid state transformer for feasibility studies and real-time implementation. *Electr. Power Syst. Res.* **2014**, *117*, 143–153. [CrossRef]
15. Jiang, Y.; Breazeale, L.; Ayyanar, R.; Mao, X. Simplified Solid State Transformer modeling for Real Time Digital Simulator (RTDS). In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 1447–1452. [CrossRef]
16. Parma, G.G.; Dinavahi, V. Real-Time Digital Hardware Simulation of Power Electronics and Drives. *IEEE Trans. Power Deliv.* **2007**, *22*, 1235–1246. [CrossRef]
17. Jack, A.G.; Atkinson, D.J.; Slater, H.J. Real-time emulation for power equipment development. I. Real-time simulation. *IEEE Proc. Electr. Power Appl.* **1998**, *145*, 92–97. [CrossRef]
18. Peña-Alzola, R.; Blaabjerg, F. Chapter 8—Design and Control of Voltage Source Converters with LCL-Filters. In *Control of Power Electronic Converters and Systems*; Blaabjerg, F., Ed.; Academic Press: Cambridge, MA, USA, 2018; pp. 207–242. [CrossRef]
19. Opal-RT Training Services. *RT-LAB Solution for Real-Time Applications, OP101: Getting Started*; Opal-RT Technologies Inc.: Montréal, QC, Canada, 2013.
20. Pejovic, P.; Maksimovic, D. A new algorithm for simulation of power electronic systems using piecewise-linear device models. *IEEE Trans. Power Electron.* **1995**, *10*, 340–348. [CrossRef]
21. Opal-RT. *eHS User Guide*; Opal-RT Technologies Inc.: Montréal, QC, Canada, 2017.
22. McLyman, C. *Transformer and Inductor Design Handbook*; CRC Press: Boca Raton, FL, USA, 2017.
23. Vadhiraj, S.; Swamy, K.N.; Divakar, B.P. Generic SPWM technique for multilevel inverter. In Proceedings of the 2013 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), Kowloon, China, 8–11 December 2013; pp. 1–5. [CrossRef]