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SVPWM Method for Multilevel Indirect Matrix Converter with Eliminate Common Mode Voltage

Nguyen Dinh Tuyen * and Le Minh Phuong

Faculty of Electrical and Electronics Engineering, Hochiminh City University of Technology, VNU-HCM, Hochiminh City 70000, Vietnam; lmphuong@hcmut.edu.vn

* Correspondence: ndtuyen@hcmut.edu.vn; Tel.: +84-9-1914-2110

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Abstract: The multilevel indirect matrix converter (IMC) is a merit of power converter for feeding a three-phase load from three-phase power supply because it has several attractive features such as: Sinusoidal input/output currents, bidirectional power flow, long lifetime due to the absence of bulky electrolytic capacitors. As compared to the conventional IMC, the multilevel IMC provides high output performance by increasing the level of output voltage. In this paper, the novel approach topology of multilevel IMC by using the combination of the cascaded rectifier and the three-level T-Type inverter is introduced. Furthermore, the new space vector pulse width modulation (SVPWM) method for the presented multilevel IMC that eliminate the common-mode voltage is proposed in this paper. The simulation study is carried out in PSIM software to verify the proposed modulation method. Then, an experimental system is built using a three-phase RL load, a multilevel IMC, a DSP controller board and other elements to verify the effectiveness of the proposed modulation method. Some simulation and experimental results are illustrated to confirm the theory analysis.

Keywords: multilevel inverter; matrix converter; indirect matrix converter; multilevel matrix converter; SVPWM

1. Introduction

Recently, the matrix converter (MC) has received considerable attention, especially in applications requiring bi-directional power flow. The MC provides direct AC/AC conversion and it is considered a competitive alternative to the conventional back-to-back converter. Compared to the back-to-back converter, the MC has several attractive features such as the simple and compact power circuit due to the lack of bulky electrolytic capacitors, sinusoidal input and output currents, controllable input power factor with any load, bidirectional power flow capability, long lifetime and high reliability [1–3]. Due to these advantages which the MC offers, it attracts many researchers to study and consider it for specialized applications in industry, such as adjustable speed drives, wind generation system, utility supply and ground power supply unit for aircraft servicing [4–7]. However, MC still has some limitations, e.g., the voltage transfer ratio constraint with a maximum value of 0.866, and a great sensitivity to the power source distortion due to the direct connection between input and output sides. With no intermediate power storage, the ride-through capability of MC is also under consideration of many researchers. And, the complicated commutation is also a shortcoming that makes the MC research more difficult. The MC topologies are divided into two types: Direct matrix converter (DMC) and the indirect matrix converter (IMC). In recent years, the IMC has received an increased amount of interest and has been studied intensely as an alternative to the DMC [8]. The concept of the IMC is to separate the AC/AC converter into two stages, namely, the rectifier stage and inverter stage, without a bulky capacitor. The rectifier stage is comprised of six bidirectional switches while the inverter stage consists of six unidirectional switches as shown in Figure 1.

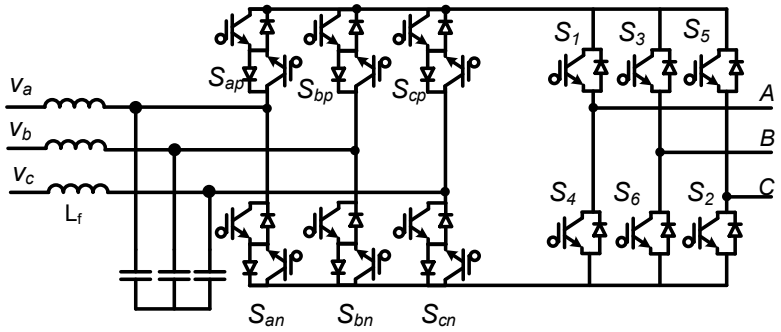

Figure 1. The conventional Indirect Matrix Converter topology.

With the limitation of voltage ratings of power switches and voltage transfer ratio, the conventional IMC is not considered for high-power applications. In last few years, there is growing interest in multilevel MC topologies to extend the application of power converters for higher voltage and power ratio. The multilevel MC can synthesize more than two-level output voltage to improve output performance in terms of reduced harmonic content. The development of multilevel MC is classified on two main topologies, i.e., multilevel direct MC (DMC) [9,10] and multilevel IMC [11,12]. The multilevel IMC provides some advantages which are not available in the DMC, e.g., simple commutation, possibility of reducing number of power switches, and possibility of reconstructing the direct AC/AC with multi three-phase output.

Over the past few years, there has been a significant effort towards addressing the technical challenges associated with the development of topology and control of the multilevel IMC. The conventional multilevel IMC topology was firstly introduced in [12], which is based on the traditional IMC, but with a rear-ends six-switch inverter replaced by a three-level neutral-point-clamped (NPC) inverter as shown in Figure 2. Then, the new multilevel IMC based on the combination of conventional NPC and cascaded-rectifier is presented in [13] in order to improve the voltage transfer ratio.

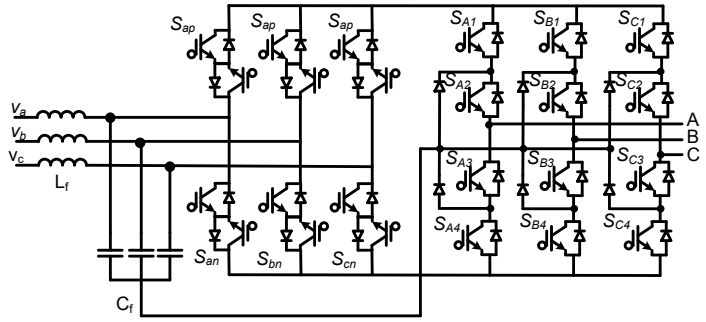

Figure 2. The conventional NPC multilevel Indirect Matrix Converter.

The common-mode voltage (CMV) is known as the main reason of the shaft voltage, leakage current, and bearing current damage, not only harms the motor lifetime, but also degrades the reliability of the electrical system. Thus, the techniques to reduce the CMV or to limit it within certain bounds are very important for the adjustable speed drive system which is fed by MC. The modulation strategies affect the CMV and several methods to reduce the CMV have been introduced in [3,14–18]. These SVPWM methods are suggested for conventional IMC and DMC to reduce the peak value of CMV by selecting the suitable zero switching states. The peak value of CMV in [14,18] is reduced to 42%. In [19,20], a new space vector modulation method to achieve zero CMV for DMC. However, the multi-step commutation and the limited of voltage transfer ratio are the advantages of the proposed method in [19,20]. Furthermore, in order to eliminate the CMV for DMC, only rotating vectors are used to synthesize the reference output voltage. Then, the output voltage performance is reduced.

Despite the multilevel IMC's outstanding advantages, the common mode voltage (CMV) generated by PWM modulation is still problematic and it has received considerable attention to eliminate. In this paper, a novel approach of multilevel IMC topology is introduced. This topology is constructed based on the comprising of cascaded rectifier and the three-level T-Type NPC inverter. Furthermore, the SVPWM strategy is presented to eliminate the CMV with zero average value of neural-point current. The SVPWM modulation method with zero CMV (ZCMV) for the multilevel NPC inverter was first presented in [21]. This method uses the six active middle vectors and one zero vector due to their ability to create zero common mode voltage. However, the average value of the neutral-point current within one sampling period still exists, and it affects the neutral-point voltage. In this paper, the new SVPWM utilizes a group of four active vectors to produce the reference output voltage. These four active vectors consist of two active vectors closest to the reference vector and its two neighbor vectors. By apply four active vectors to synthesize the reference output voltage vector, the average value of neutral-point current is zero while the voltage transfer ratio was not affected. As compared to [3,14–18], the presented topology with proposed SVPWM method in this paper can provide the zero CMV.

The rest of this paper is organized as follows. Section 2 introduces the multilevel IMC topology and the SVPWM method to eliminate the CMV with canceling the neutral-point current. In Section 3, some simulation and experimental results are provided to illustrate the efficiency of the proposed method. Finally, conclusions are included in Section 4.

2. Multilevel Indirect Matrix Converter and the Proposed SVPWM Method

2.1. The Multilevel IMC Topology

As shown in Figure 3, the multilevel IMC comprises of two stages: The rectifier stage and the three-level T-Type inverter stage. The function of the rectifier stage is to generate sinusoidal input currents as well as to maintain the maximum DC voltage at the DC-link. The expected output voltages with variable frequency are obtained by control at the inverter stage. The cascaded rectifier is built by two identical three-phase bidirectional front-end current source rectifier (CSR) modules connected in series [12]. Each CSR includes six bidirectional as shown in Figure 3 (S_{ap1}, S_{an1}, S_{bp1}, S_{bn1}, S_{cp1}, S_{cn1} for upper rectifier; and S_{ap2}, S_{an2}, S_{bp2}, S_{bn2}, S_{cp2}, S_{cn2} for lower rectifier), and they are connected at neutral-point "O". The upper and lower rectifier stages generated the DC-link voltage: V_{PO} and V_{ON}, respectively. The switching states at the rectifier stage and the DC-link voltage are shown in Table 1, where v_{ab}, v_{ac}, v_{bc}, v_{ba}, v_{ca}, v_{cb} are the line-to-line input voltage.

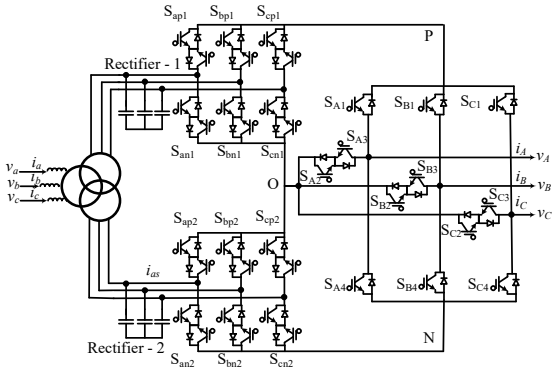

Figure 3. The Three-level T-Type Indirect Matrix Converter Topology.

Table 1. The switching states at rectifier stage and the DC-link voltage.

Switching State						DC-Link Voltage	
S_{ap1} S_{ap2}	S_{bp1} S_{bp2}	S_{cp1} S_{cp2}	S_{an1} S_{an2}	S_{bn1} S_{bn2}	S_{cn1} S_{cn2}	V_{PO}	V_{ON}
1	0	0	0	1	0	v_{ab}	v_{ab}
1	0	0	0	0	1	v_{ac}	v_{ac}
0	1	0	0	0	1	v_{bc}	v_{bc}
0	1	0	1	0	0	v_{ba}	v_{ba}
0	0	1	1	0	0	v_{ca}	v_{ca}
0	0	1	0	1	0	v_{cb}	v_{cb}
1	0	0	1	0	0	0	0
0	1	0	0	1	0	0	0
0	0	1	0	0	1	0	0

The three-level T-Type NPC inverter is the extension configuration of a traditional two-level three-phase inverter, by adding three bidirectional power switches that connect three-load output to the neutral point. Comparison with the traditional three-level NPC, the three-level T-Type NPC inverter have many advantages, e.g., less losses, less semiconductor components due to the absence of clamping diode [22,23]. From Figure 3, the switching state and load voltage of inverter stage are given in Table 2.

Table 2. The state of inverter stage and the output voltage according to the switching state.

Inverter Stage's State	Switching State of Power Switches $X = (A, B, C)$				Output-Phase Voltage V_{XO} $X = (A, B, C)$
	S_{X1}	S_{X2}	S_{X3}	S_{X4}	
1	1	1	0	0	V_{PO}
0	0	1	1	0	0
−1	0	0	1	1	$-V_{ON}$

2.2. The SVPWM Method for Elimination the CMV

SVPWM techniques have been widely used for the power converter as a common industrial practice due to it has flexibility. The SVPWM is the general solution to the modulation problem of the IMC drive. This modulation can provide the possibility to obtain the highest voltage transfer ratio and to optimize the switching pattern by coordinate the switching state in the rectifier and inverter stages. The space vector approach for the multilevel IMC is based on the instantaneous space vector representation input current vector and output voltage vectors. The SVM produces a combination of vectors to synthesize the input current and output voltage vectors in the rectifier and inverter stages, respectively. Once the vectors and their duty cycles of each stage are determined, the switching pattern of the converter is obtained by combining the switching states from two stages in order to keep balance input and output currents. In this section, the novel SVPWM method is proposed to eliminate the CMV and to cancel the neutral-point current within the sampling period control.

2.2.1. Rectifier Stage Control

It is assumed that three-phase supply voltages v_a, v_b, v_c are given by:

$$\begin{aligned} v_a &= V_{in}\cos(\omega_{in}t) \\ v_b &= V_{in}\cos(\omega_{in}t - 2\pi/3) \\ v_c &= V_{in}\cos(\omega_{in}t + 2\pi/3) \end{aligned} \tag{1}$$

where V_{in} is the amplitude of input phase voltage and ω_{in} is the angular frequency of the input side.

The current space vectors of the rectifier are illustrated in Figure 4. There are six active vectors with fixed direction and three zero vectors. Each active vector represents the connection of the input phase voltage to the positive, neutral or negative point of DC-link bus. In each sector, the reference current space vector is synthesized by two neighbor active vectors.

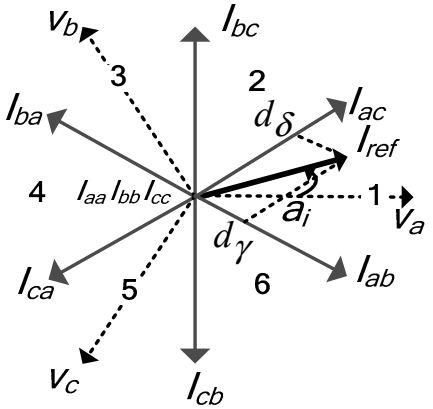

Figure 4. The space vector diagram of the rectifier stage.

We assume that the reference current vector is located in sector 1 as shown in Figure 4. The duty cycles d_γ, d_δ of two active vectors I_{ab}, I_{ac} are given below:

$$d_\gamma = m_i \sin(\pi/6 - \alpha_i); d_\delta = m_i \sin(\pi/6 + \alpha_i) \tag{2}$$

where m_i is the modulation index in the rectifier stage and α_i is the phase angular of the reference input current.

Due to the elimination of zero vectors in the modulation of the rectifier stage to obtain the highest of DC-link voltage, the duty cycles of two active vectors is modified as following:

$$d_x = \frac{d_\gamma}{d_\delta + d_\gamma}; d_y = \frac{d_\delta}{d_\delta + d_\gamma} \tag{3}$$

The local average value of DC-link voltage in one sampling period which is generated by the upper and lower rectifier can be written as:

$$V_{PO} = V_{ON} = d_x v_{ab} + d_y v_{ac} = \frac{3V_{in}^2}{2v_a} \tag{4}$$

Therefore, the average DC-link voltage is

$$V_{DC} = V_{PO} + V_{ON} = 3V_{in}^2/v_a \tag{5}$$

Similarly, Table 3 summarizes the average of DC-link voltage, duty cycles of active vectors according to the input current sector.

Table 3. Switching state and average DC link voltage according to the input current sector.

Input Voltage Phase $\omega_{in}t$	Sector	ON Switch	Modulated Switches	Duty Ratios	Instantaneous Split DC-Link Voltages	Average DC-Link Voltage v_{PN}
		Upper Rectifier Lower Rectifier		(d_x, d_y) (d_x, d_y)	V_{PO} V_{ON}	
$-\pi/6\ \pi/6$	I	S_{ap1} S_{ap2}	(S_{bn1}, S_{cn1}) (S_{bn2}, S_{cn2})	$(-v_b/v_a, -v_c/v_a)$	v_{ab} v_{ac}	$3V_{in}^2/v_a$
$\pi/6\ \pi/2$	II	S_{cn1} S_{cn2}	(S_{bp1}, S_{ap1}) (S_{bp2}, S_{ap2})	$(-v_b/v_c, -v_a/v_c)$	v_{bc} v_{ac}	$-3V_{in}^2/v_c$
$\pi/2.5\pi/6$	III	S_{bp1} S_{bp2}	(S_{cn1}, S_{an1}) (S_{cn2}, S_{an2})	$(-v_c/v_b, -v_a/v_b)$	v_{bc} v_{ba}	$3V_{in}^2/v_b$
$5\pi/6.7\pi/6$	IV	S_{an1} S_{an2}	(S_{cp1}, S_{bp1}) (S_{cp2}, S_{bp2})	$(-v_c/v_a, -v_b/v_a)$	v_{ca} v_{ba}	$-3V_{in}^2/v_a$
$7\pi/6.9\pi/6$	V	S_{cp1} S_{cp2}	(S_{an1}, S_{bn1}) (S_{an2}, S_{bn2})	$(-v_b/v_c, -v_b/v_a)$	v_{cb} v_{ca}	$3V_{in}^2/v_c$
$9\pi/6.11\pi/6$	VI	S_{bn1} S_{bn2}	(S_{cp1}, S_{ap1}) (S_{cp2}, S_{ap2})	$(-v_c/v_b, -v_a/v_b)$ $(-v_c/v_b, -v_a/v_b)$	v_{ab} v_{cb}	$-3V_{in}^2/v_b$

2.2.2. Inverter Stage Control

Once the switching states of the rectifier stage have been decided, the SVPWM is applied to control the three-level T-Type NPC inverter. With the three-phase load, the system variables (voltages or currents) in *abc* coordinates can be transformed to $\alpha\beta$ coordinates by using the transformation defined in (5).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{6}$$

where V_A, V_B, V_C are three-phase output voltage and V_α, V_β are corresponding voltage sequence in $\alpha\beta$ plane given by Clark transform.

From (5), the size of each vector can be calculated and given in Table 4. The space vector diagram of the three-level T-type NPC inverter includes of 27 vectors which can be split into three categories: Zero, large, medium and small vectors. There are 6 large vectors, 6 medium vectors, 12 small vectors and 3 additional zero vectors as shown in Figure 5. On the plane vectors as shown in Figure 5, each vector indicates the connection of the output phase to the DC-link bus. For example, vector $V_{13\ (1\text{-}1\text{-}1)}$ represents the connection of the output phase "*A*" to the positive pole "*P*", output phase "*B*" and "*C*" to the negative pole "*N*" of DC-link bus.

There are three kinds of modulation strategies for three-level NPC inverter, i.e., carrier-based PWM, SVPWM and Selected Harmonics Elimination. Among three methods, the SVPWM has been a very popular PWM technique. In the space vector approach, over one PWM cycle, a specific number of voltage vectors are selected and used in a specific time length and sequence. The SVPWM with zero CMV was firstly presented in [21], but the neutral-point voltage imbalance stills exist due to the neutral-point current. In this paper, the novel SVPWM method is presented to obtain the zero CMV and to cancel the neutral-point current.

Table 4. Space vectors, switching states and type of vectors.

Space Vectors	Switching States	V_α	V_β	Type of Vector	Vector Magnitude
	(−1,−1,−1)	0	0		
$\vec{V_0}$	(0,0,0)	0	0	Zero vector	0
	(1,1,1)	0	0		
$\vec{V_1}$	(1,0,0)	$V_{DC}/3$	0		
	(0,−1,−1)	$V_{DC}/3$	0		
$\vec{V_2}$	(1,1,0)	$V_{DC}/6$	$\sqrt{3}V_{DC}/6$		
	(0,0,−1)	$V_{DC}/6$	$\sqrt{3}V_{DC}/6$		
$\vec{V_3}$	(0,1,0)	$-V_{DC}/6$	$\sqrt{3}V_{DC}/6$		
	(−1,0,−1)	$-V_{DC}/6$	$\sqrt{3}V_{DC}/6$	Small vector	$\frac{1}{3}$V$_{DC}$
$\vec{V_4}$	(0,1,1)	$-V_{DC}/3$	0		
	(−1,0,0)	$-V_{DC}/3$	0		
$\vec{V_5}$	(0,0,1)	$-V_{DC}/6$	$-\sqrt{3}V_{DC}/6$		
	(−1,−1,0)	$-V_{DC}/6$	$-\sqrt{3}V_{DC}/6$		
$\vec{V_6}$	(1,0,1)	$V_{DC}/6$	$-\sqrt{3}V_{DC}/6$		
	(0,−1,0)	$V_{DC}/6$	$-\sqrt{3}V_{DC}/6$		
$\vec{V_7}$	(1,0,−1)	$V_{DC}/2$	$\sqrt{3}V_{DC}/6$		
$\vec{V_8}$	(0,1,−1)	0	$\sqrt{3}V_{DC}/3$		
$\vec{V_9}$	(−1,1,0)	$-V_{DC}/2$	$\sqrt{3}V_{DC}/6$	Medium Vector	$\frac{\sqrt{3}}{3}$V$_{DC}$
$\vec{V_{10}}$	(−1,0,1)	$-V_{DC}/2$	$-\sqrt{3}V_{DC}/6$		
$\vec{V_{11}}$	(0,−1,1)	0	$-\sqrt{3}V_{DC}/3$		
$\vec{V_{12}}$	(1,−1,0)	$V_{DC}/2$	$-\sqrt{3}V_{DC}/6$		
$\vec{V_{13}}$	(1,−1,−1)	$2V_{DC}/3$	0		
$\vec{V_{14}}$	(1,1,−1)	$V_{DC}/3$	$\sqrt{3}V_{DC}/3$		
$\vec{V_{15}}$	(−1,1,−1)	$-V_{DC}/3$	$\sqrt{3}V_{DC}/3$	Large vector	$\frac{2}{3}$V$_{DC}$
$\vec{V_{16}}$	(−1,1,1)	$-2V_{DC}/3$	0		
$\vec{V_{17}}$	(−1,−1,1)	$-V_{DC}/3$	$-\sqrt{3}V_{DC}/3$		
$\vec{V_{18}}$	(1,−1,1)	$V_{DC}/3$	$-\sqrt{3}V_{DC}/3$		

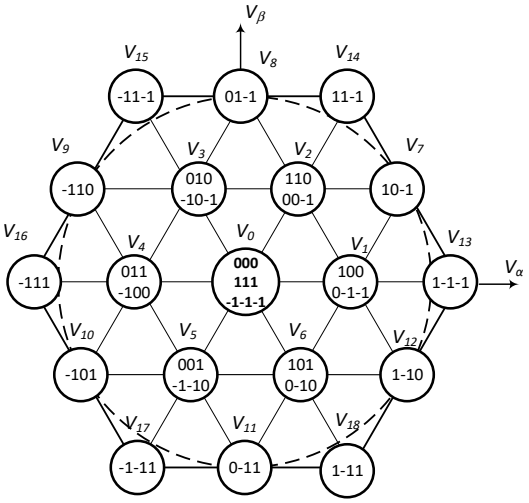

Figure 5. The space vector diagram of the 3-level T-Type NPC inverter stage.

In the three-phase load, the CMV can be defined as a voltage between motor neutral point and ground point of power supply. The CMV can be described as follows:

$$\begin{aligned} v_A - v_{CM} &= Ri_A + L(di_A/dt) \\ v_B - v_{CM} &= Ri_B + L(di_B/dt) \\ v_C - v_{CM} &= Ri_C + L(di_C/dt) \end{aligned} \tag{7}$$

where v_{CM} is the common mode voltage; i_A, i_B, i_C are three-phase output currents; R L are resistor and inductor of the load.

Under the assumption that the sum of output currents is equal to zero, $i_A + i_B + i_C = 0$. The CMV can be obtained as follows:

$$v_{CM} = \frac{v_A + v_B + v_C}{3} \tag{8}$$

From (7), Table 5 shows the CMV according to the state of the inverter stage.

Table 5. The CMV of the 3-level T-Type NPC inverter.

Inverter Stage's Switching State	Common Mode Voltage
(0,0,0)	*0*
(−1,−1,−1)	$-V_{DC}/2$
(1,1,1)	$V_{DC}/2$
(1,0,0); (0,1,0); (0,0,1); (−1,1,1); (1,−1,1); (1,1,−1)	$V_{DC}/6$
(0,0,−1); (−1,0,0); (0,−1,0); (1,−1,−1); (−1,1,−1); (−1,−1,1)	$-V_{DC}/6$
(1,0,−1); (0,1,−1); (−1,1,0); (−1,0,1); (0,−1,1); (1,−1,0)	*0*
(1,1,0); (1,0,1); (0,1,1)	$V_{DC}/3$
(0,−1,−1); (−1,0,−1); (−1,−1,0)	$-V_{DC}/3$

From Table 5, it can be easily seen that the magnitude of CMV has seven values: 0, $\pm V_{DC}/6$, $\pm V_{DC}/3$, $\pm V_{DC}/2$. In these 27 vectors, one zero and six medium vectors produce the ZCMV. The implementation of ZCMV modulation using an SVPWM approach is shown in Figure 6. It is assumed that the reference output voltage vector is in sector 1.

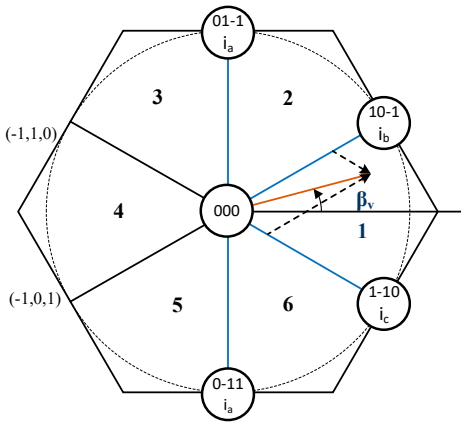

Figure 6. Space vector diagram and the selected vectors for zero common voltage.

The reference voltage vector V_{ref} can be obtained as:

$$V_{ref} = d_{01-1}V_{01-1} + d_{10-1}V_{10-1} + d_{1-10}V_{1-10} + d_{0-11}V_{0-11} \tag{9}$$

where $d_{01\text{-}1}$, $d_{01\text{-}1}$, $d_{1\text{-}10}$ and $d_{0\text{-}11}$ are duty cycles of four active vectors $V_{01\text{-}1}$, $V_{10\text{-}1}$, $V_{1\text{-}10}$ and $V_{0\text{-}11}$, respectively.

When one phase leg is clamped to the neutral-point, its output current is injected to this point. Therefore, the average neutral-point current within sampling period is determined as:

$$I_O = d_{01-1} i_A + d_{10-1} i_B + d_{1-10} i_C + d_{0-11} i_A \tag{10}$$

The neutral-point current can be rewritten as:

$$I_O = d_{01-1} i_A + d'_{10-1} i_B + d'_{1-10} i_C + d''_{10-1} i_B + d''_{1-10} i_C + d_{01-1} i_A \tag{11}$$

where

$$d_{10-1} = d'_{10-1} + d''_{10-1} \tag{12}$$

$$d_{1-10} = d'_{1-10} + d''_{1-10} \tag{13}$$

To find the duty cycles of active vectors for obtaining the zero-average value of neutral-point current, the following two equations are used:

$$d_{01-1} = d'_{10-1} = d'_{1-10} \tag{14}$$

$$d''_{10-1} = d''_{1-10} = d_{01-1} \tag{15}$$

Substitute the (12), (13) to (8), we have:

$$V_{ref} = d_{01-1} V_{01-1} + d_{10-1} V_{10-1} + d_{1-10} V_{1-10} + d_{01-1} V_{01-1} \tag{16}$$

From (10)–(14), the duty cycles of the active and zero vectors is calculated as following:

$$d_{1-10} = d'_{1-10} + d''_{1-10} \tag{17}$$

$$d_{10-1} = d'_{10-1} + d''_{10-1} \tag{18}$$

$$d_{0-11} = \frac{V_{ref}}{V_{dc}} \sin\left(\frac{\pi}{6} - \beta_v\right) \tag{19}$$

$$d_{01-1} = \frac{V_{ref}}{V_{dc}} \sin\left(\frac{\pi}{6} + \beta_v\right) \tag{20}$$

$$d_{1-10} = d_{10-1} = \frac{V_{ref}}{V_{dc}} \sin\left(\frac{\pi}{6} + \beta_v\right) + \frac{V_{ref}}{V_{dc}} \sin\left(\frac{\pi}{6} - \beta_v\right) \tag{21}$$

To complete one sampling period, the zero vector V_{000} is inserted and its duty cycle is calculated as:

$$d_{000} = 1 - d_{1-10} - d_{10-1} - d_{0-11} - d_{01-1} = 1 - \frac{2V_{ref}}{V_{dc}} \cos \beta_v \tag{22}$$

where β_v is a phase angle of reference output voltage vector ($-\pi/6 \leq \beta_v \leq \pi/6$) and d_{000} are duty cycle of zero vector $V_{000.}$

2.3. Maximum Voltage Transfer Ratio

If we define m as the voltage transfer ratio, which is the ratio between the output and input voltages, then:

$$m = \frac{V_{ref}}{V_{in}} \tag{23}$$

From (4), the minimum values of the average DC-link voltage are:

All duty cycles must be positive and lower than unity, from (22) and (24), the maximum of reference output voltage is

$$V_{ref} < \frac{V_{DC}}{2} \tag{24}$$

From (8) and (20), the maximum voltage transfer ratio of the three-level T-Type NPC IMC is

$$m_{\max} = 1.5 \tag{25}$$

2.4. Switching Sequence

To obtain a balanced output currents and input currents, the PWM pattern of the multilevel IMC should produce all combinations between the switching states of the rectifier and the inverter stages. Figure 7 shows the switching sequence of the T-Type multilevel IMC in case of the reference input current and reference output voltage are located in sector 1 as shown in Figure 4; Figure 6, respectively. It is noted that the switching state of the rectifier and inverter stages are arranged to guarantee the zero DC-link current commutation at the rectifier stage, therefore the multi-step commutation is avoided.

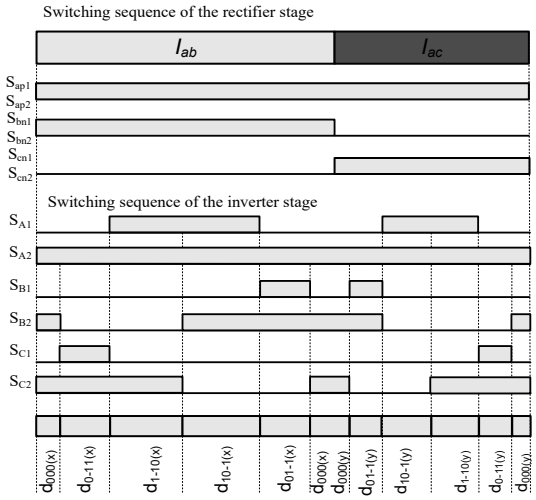

Figure 7. The switching pattern of the multilevel IMC with the proposed SVPWM method.

The duty cycles for each voltage vector of the inverter stage can be determined using equations:

$$d_{0-11(x)} = d_{0-11}d_x; d_{1-10(x)} = d_{1-10}d_x; d_{10-1(x)} = d_{10-1}d_x; d_{01-1(x)} = d_{01-1}d_x \tag{26}$$

$$d_{0-11(y)} = d_{0-11}d_y; d_{1-10(y)} = d_{1-10}d_y; d_{10-1(y)} = d_{10-1}d_y; d_{01-1(y)} = d_{01-1}d_y \tag{27}$$

3. Simulation Results and Experimental Results

Simulations and experiments are carried out in order to verify the proposed method for multilevel IMC control. The simulation process is performed by using PSIM 9.1 software. The parameters of the system including power supply, load, sampling period control for simulation are given in Table 6.

Table 6. The parameter for simulation and experimental.

Input voltage (V_{in})	100 V
Input frequency (f_{in})	50 Hz
R load	20 Ω
L load	20 mH
Output frequency (f_{out})	40 Hz
Sampling period (T_s)	100 kHz
Voltage transfer ratio (m)	1.2

In Figure 8, the input phase voltage (v_a) and input phase current (i_a) are shown. At the input side, the LC input filter is used to filter the switching frequency harmonic, therefore, the sinusoidal input current waveform is obtained. The input current and input voltage waveforms are almost in-phase. The dc-link voltage which is generated by the upper and lower rectifier stages is shown in Figure 9. It can be seen that the DC-link voltage does not consist of the zero voltage and it is modulated between the maximum and medium line-to-line input voltages. The shape of DC-link voltage is formed by the line-to-line input voltage and two dc-link voltages are the same value. The line-to-line output voltage (V_{AB}), the phase output voltage (V_A) and output current are shown in Figure 10; it is evident that output current is sinusoidal waveforms. In order to see the performance of the converter, the total harmonic distortion (THD) of the input current and the output voltage are shown in Table 7.

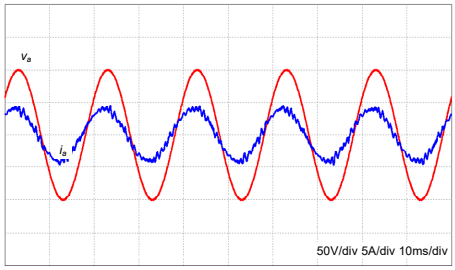

Figure 8. The simulation results of input current and input voltage.

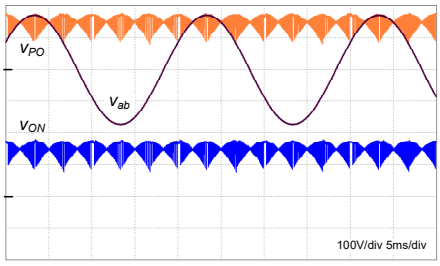

Figure 9. The simulation results of DC-link voltage V_{PO} and V_{ON}, which are generated by the upper and lower rectifiers, respectively.

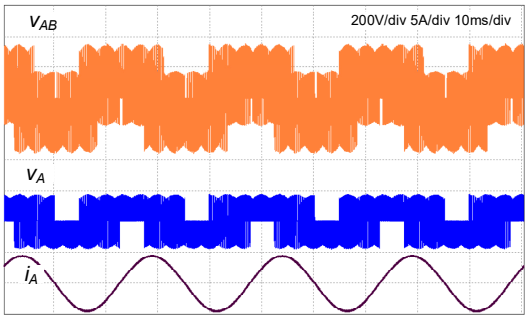

Figure 10. The simulation results of line-to-line output voltage, phase output voltage and output current.

Table 7. The THD of input current and output voltage according to the voltage transfer ratio.

Voltage Transfer Ratio (m)	THD of Input Current (%)	THD of Output Voltage
0.2	0.42	6.48
0.4	1.52	4.57
0.6	2.62	3.48
0.8	3.80	2.76
1.0	4.55	2.30
1.2	6.20	1.94
1.4	6.82	1.60

In order to confirm the propriety of the proposed topology, theory analysis and simulated results, an experiment for the proposed SVPWM method was built. The experimental parameters are identical to the simulation parameters. Figure 11 shows the block diagram of a multilevel IMC and Figure 12 indicates the photograph of the experimental setup. The system consists of a controller board, power board, sensor board and driver board. The controller board is developed with a high-performance DSP TMS320F28377S, which executes the A/D converter, the generating PWM signals for driver circuit. The sensor board uses the LV-25P of LEM. The power board was implemented by using IGBT SK 60GM123 for bidirectional switches and IGBT FMG2G50U60 for dual switch in the inverter stage. Table 8 lists the model name, manufacturer and the ratings of the power switches used in the power converter.

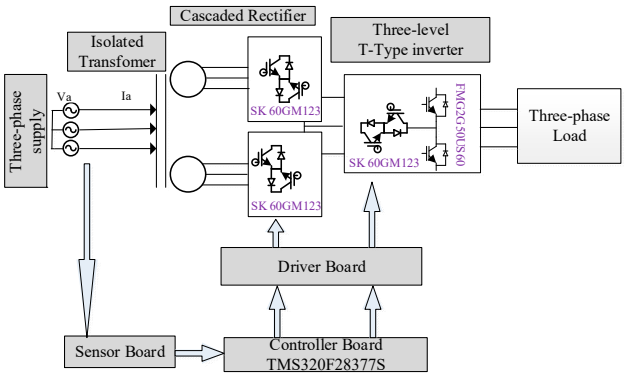

Figure 11. Block diagram of the multilevel IMC hardware experiment.

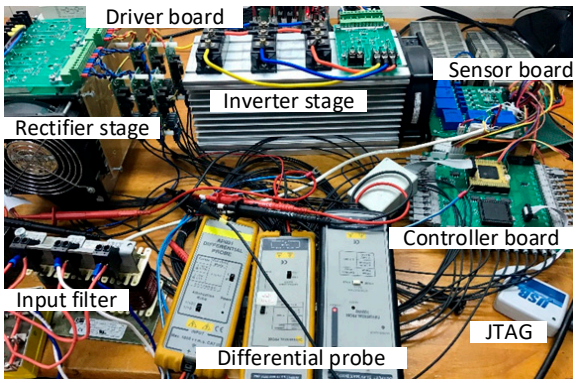

Figure 12. Experimental setup.

Table 8. Summary of IGBT Module for the converter.

Model Name	Manufacturer	Rated Voltage	Rated Current	Power Switches in Figure 3
SK 60GM123	Semikron	1200 V	50 A	S_{ap1}, S_{an1}, S_{bp1}, S_{bn1}, $S_{cp1,}$ S_{cn1} S_{ap2}, S_{an2}, S_{bp2}, S_{bn2}, $S_{cp2,}$ S_{cn2}
FMG 2G 50US60	Fairchild Semiconductor	600 V	50 A	S_{A2}, S_{A3}, S_{B2}, S_{B3}, S_{C2}, S_{C3} S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_{C1}, S_{C4}

The pulse signals for the rectifier stage according to the input sector are shown in Figure 13. It can be seen that, the switch S_{ap1}, S_{ap2} are always at ON state in sector 1, they are modulated in sector 2 and 6 and at OFF state in all remain sectors. Figure 14 shows the PWM signals for the rectifier and inverter stages, and the zoom in of these waveforms is shown in Figure 15. From Figure 15, the switch S_{ap1} of the rectifier stage changes the status from ON to OFF or OFF to ON during the time when the zero vector is applied in the inverter stage (S_{A1} is OFF state and S_{A2} is ON state). It means that the soft-switching is achieved in the rectifier stage.

The experimental results of input side, DC-link voltage and output side are shown in Figures 16–18, respectively. It can be seen that both of the input current and output current are sinusoidal waveforms. However, the input current contains some ripple due to the limitation of input LC filter. Furthermore, the level of output voltages of the multilevel IMC is higher than that of conventional two-level IMC. Figure 19 shows the phase-to-neutral point voltage and the common mode voltage. The zero common mode voltage is obtained with the proposed method.

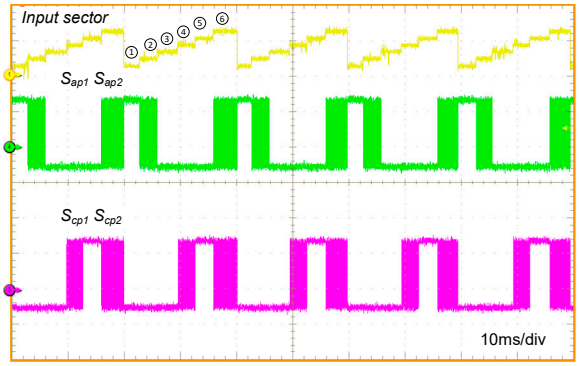

Figure 13. Input sector and the PWM signals of rectifier stages.

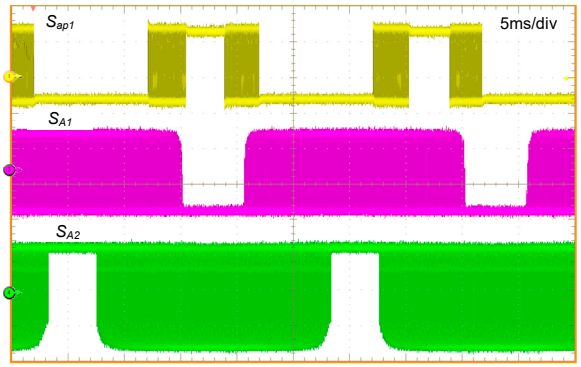

Figure 14. The PWM signals of rectifier and inverter stages.

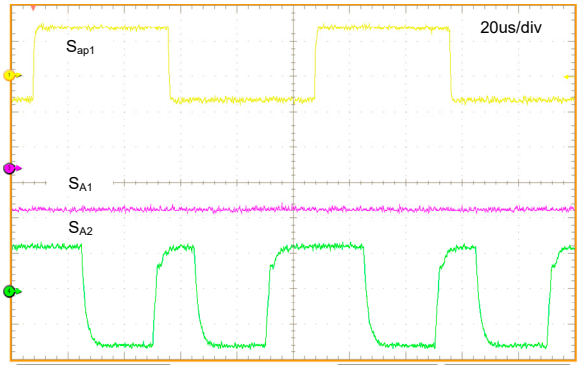

Figure 15. The zoom-in of PWM signals of rectifier and inverter stages.

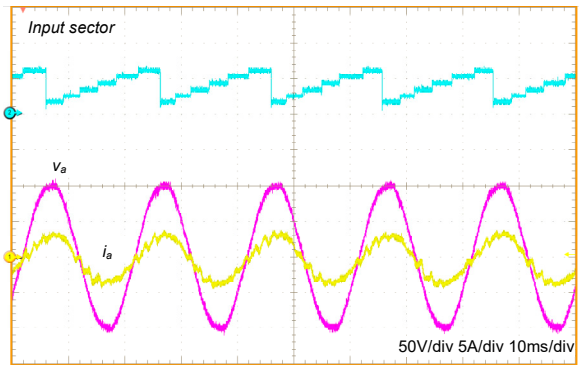

Figure 16. Experimental results of input side.

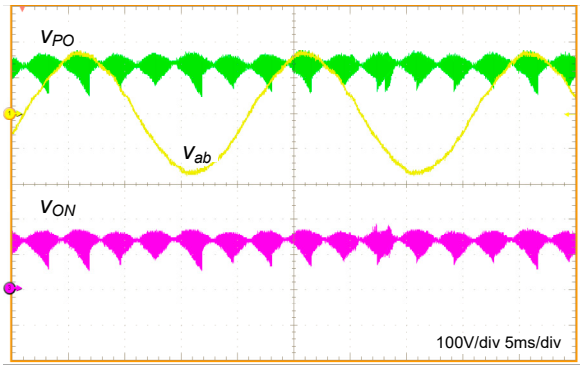

Figure 17. Experimental results of DC-link voltage.

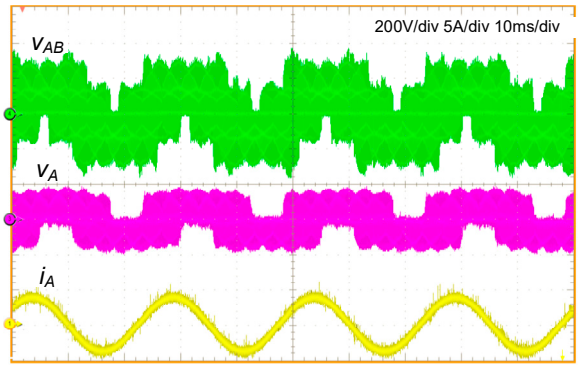

Figure 18. Experimental results of load side: line-to-line output voltage, phase output voltage and output current.

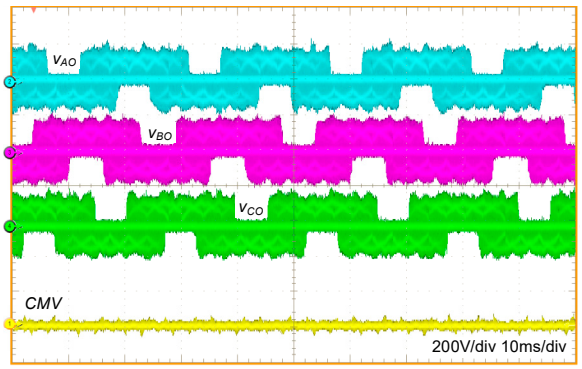

Figure 19. The phase to neutral voltage and the common mode voltage.

4. Conclusions

We have introduced the novel approach of multilevel IMC and proposed SVPWM method with zero common mode voltage. The explanation of multilevel IMC operating and duty cycles calculating are provided. Both simulation and experimental results are shown to demonstrate the effectiveness of the proposed method. Besides the advantageous features of the conventional MC, i.e., compact design, sinusoidal input/output current, bidirectional power flow, we have figured out other features to compensate for the drawbacks of the IMC, i.e., used two cascaded-rectifier to improve the voltage transfer ratio, proposed new SVPWM method to obtain zero CMV with neutral-point voltage balancing.

Author Contributions: N.D.T. developed the idea of this paper, implemented the main research and validated in the real system. L.M.P. performed the analysis and simulation. All authors contributed to the writing of the manuscript, revised and approved the final manuscript.

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