Article

Combinational Circuits Testing Based on Hsiao Codes with Self-Dual Check Functions

Dmitry V. Efanov [1,2,3,*], Tatiana S. Pogodina [1], Nazirjan M. Aripov [2], Sunnatillo T. Boltayev [2], Asadulla R. Azizov [2], Elnara K. Ametova [2] and Feruza F. Shakirova [2]

[1] Higher School of Transport, Institute of Machinery, Materials and Transport, Peter the Great St. Petersburg Polytechnic University, St. Petersburg 195251, Russia; pogodina-ts@mail.ru
[2] «Automation and Remote Control» Department, Tashkent State Transport University, Tashkent 100167, Uzbekistan; aripov_n@tstu.uz (N.M.A.); boltaev_s@tstu.uz (S.T.B.); azizov_a@tstu.uz (A.R.A.); elnara_84@tstu.uz (E.K.A.); shakirova_ff@tstu.uz (F.F.S.)
[3] "Automation, Remote Control and Communication on Railway Transport" Department, Russian University of Transport, Moscow 127994, Russia
* Correspondence: efanov_dv@spbstu.ru

Abstract: This paper investigates the features of using modified Hamming codes, which are also known as Hsiao codes. Self-checking digital devices are proposed to be implemented with calculations testing using two diagnostic signs. These signs indicate that the functions (there are functions that describe check bits) belong to the class of self-dual Boolean functions and also belong to the codewords of Hsiao codes (these are codes with an odd column of weights). The authors have established that all check functions can be self-dual for a certain number of the Hsiao codes' data symbols. Such codes can be used in the synthesis of concurrent error-detection circuits by two diagnostic signs. The paper describes the structure of an organization for a concurrent error-detection circuit based on Hsiao codes with self-dual check functions. Some experimental results are presented on the synthesis of self-checking devices using the proposed methodology. The controllability of the structure and the number of test combinations both increased. Hsiao codes can be effectively used with self-dual check functions in the synthesis of self-checking digital devices.

Keywords: self-checking digital devices; Hamming codes; Hsiao codes; error detection in digital devices; concurrent error-detection circuit; calculations testing by two diagnostic signs; testing the self-duality of signals

Academic Editor: Demos T. Tsahalis

Received: 5 December 2024
Revised: 31 December 2024
Accepted: 11 January 2025
Published: 13 January 2025

Citation: Efanov, D.V.; Pogodina, T.S.; Aripov, N.M.; Boltayev, S.T.; Azizov, A.R.; Ametova, E.K.; Shakirova, F.F. Combinational Circuits Testing Based on Hsiao Codes with Self-Dual Check Functions. *Computation* **2025**, *13*, 15. https://doi.org/10.3390/computation13010015

Copyright: © 2025 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

The methods of redundancy and technical diagnostics are widely applied in the construction of highly reliable safety devices and operation systems [1–6]. Time redundancy is one of the ways to add redundancy. The time redundancy implies the availability of a time resource to perform procedures for checking and performance restoration of the original object [7]. Self-testing and self-checking digital devices are created when using a time redundancy along with a special representation of signals [8,9]. Calculations testing is convenient to use in this case when functions belonged to special classes of Boolean functions such as monotonous, linear and/or self–dual functions [10–14]. Let us focus on the combination of linearity and self-duality of generated functions when performing calculations testing using time redundancy and the pulse mode of operation. Linear redundant codes can be used for this [15,16]. Such double calculations testing makes it possible to enhance the controllability of a final self-checking device and to ensure the

testing of faults and errors in calculations over a much larger number of input combinations. This will not be effective when using a single diagnostic sign.

It should be noted that the calculations testing by two signs has already been considered in several papers. The authors of [17,18] report the features of the organization of calculations testing using the control of monotonicity and self-duality of calculated functions. The first property relates to the functions that generate the values for the codewords bits in the «r-out-of-2r» constant-weight codes, where r is the codeword weight. The second property relies on the use of a method for logical signals correction, or logical complement [19–21], in a concurrent error-detection circuit (CED). Additionally, the values are generated by each input set of codewords and must be such that each function describes the digits of a self-dual codeword. The authors of [15,16] report that classical and modified Hamming codes [22] can also be used for calculations testing by two diagnostic signs. These codes have the property of self-dual functions (which describe the check bits) for certain data symbols values. An example is also given for the synthesis of a device with the calculations testing by two signs for a four-output device.

The author of [23] reports that one of the well-known modifications of Hamming codes is the odd-weight-column codes. These codes are called by the name of their discoverer, Hsiao. They are often used in the implementation of devices with error detection and correction [24,25]. They are linear and have self-dual functions, which describe the check bits under certain conditions.

A large number of works are devoted to the use of Hsiao codes for the organization of CED circuits. Papers [26–28] report that these codes are used to calculate the testing and correct errors at the cache level of the memory hierarchy to increase reliability. However, in all papers, only the sign of control is used, which relates to the codewords of Hsiao codes. These papers focus on the application of Hsiao codes for the organization of CED circuits. The authors of this paper conducted an analysis and discovered that the Hsiao codes also have another "natural" property in which their check symbols are described by self-dual Boolean functions under certain conditions. In this paper, we propose a way to organize CED circuits. There is another diagnostic sign in the Hsiao code that is embedded within the Hsiao code at certain values of the number of data symbols and conditions for code construction. In the paper, the CED circuit is developed based on two diagnostic signs. It has improved performance indicators compared to well-known structures, for example, from [13,14], as well as traditional ones [29,30].

2. The Hsiao Codes

The Hsiao codes are generated in accordance with the following rules [31]:

1. The value of the number of data symbols m is the selected item.
2. All columns are assigned to check symbols in the check matrix with weight $r = 1$ (their number is $\binom{k}{1}$, where k is the number of check symbols and the number of rows in the matrix).
3. All columns are selected sequentially with an odd weight value $r = 3, 5, 7, \ldots$ corresponding to data symbols $\binom{k}{3}$ columns with an odd weight $r = 3$; then, $\binom{k}{5}$ columns are selected with an odd of weight $r = 5$, and so on, until m columns have been selected with an odd weight.

Table 1 reports the values of m for various k. $m_{\max}$ is the maximum value of the number m for a particular k, and N_r is the total number of columns with an odd weight r: $\binom{k}{3} + \binom{k}{5} + \ldots + \binom{k}{l}$, $l = m$, if m is an odd, $l = m$–1, if m is an even.

Table 1. Parameters of the Hsiao codes.

k	N_r	$m_{\max}$
4	$\binom{4}{3}$	4
5	$\binom{5}{3} + \binom{5}{5}$	11
6	$\binom{6}{3} + \binom{6}{5}$	26
7	$\binom{7}{3} + \binom{7}{5} + \binom{7}{7}$	57
8	$\binom{8}{3} + \binom{8}{5} + \binom{8}{7}$	120
9	$\binom{9}{3} + \binom{9}{5} + \binom{9}{7} + \binom{9}{9}$	247
10	$\binom{10}{3} + \binom{10}{5} + \binom{10}{7} + \binom{10}{9}$	502

The Hsiao codes can be generated by using a check matrix. The columns are removed with a weight of r = 1 in this matrix (these columns correspond to check symbols), and all other columns remain (these columns correspond to data symbols). The value of the y_i, $i = \overline{1,k}$ bit is calculated as the sum modulo M = 2 data symbols, for which 1 is present in the intersection of the i-th row and all columns that have a weight $r \geq 3$. A check matrix is given for the Hsiao codes with the value k = 5:

$$H_5 = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{pmatrix}. \quad (1)$$

The maximum number of data symbols in the Hsiao code for a given value k is determined by

$$m_{\max} = \sum_{r=1+2j} \binom{k}{r},\ j = 1,\ 2,\ \ldots,\ \left\lfloor \frac{k}{2} \right\rfloor. \quad (2)$$

It follows from the last formula that the number of ways to build a code with the value $m \leq m_{\max}$ is determined by

$$N_{k,m} = \binom{m_{\max}}{m}. \quad (3)$$

The permutation of columns in check matrices allows for the construction of Hsiao codes by selecting m columns from a max with various arguments used in formulas to determine the check symbols. For example, for m = 7, we have $N_{5,7} = \begin{pmatrix} 11 \\ 7 \end{pmatrix} = 330$.

Research has shown that the Hsiao codes possess the property of detecting errors with multiplicities $d \leq 3$. Specifically, these codes are endowed with corrective properties. These are the features of the Hsiao codes that can be considered when designing self-checking combinational circuits. Therefore, this paper will focus on the detecting abilities of these codes. We will consider the codewords' bits on the outputs of diagnostic objects belonging to the calculated Hsiao codes in the CED as a diagnostic sign. Additionally, another feature of these codes can serve as a second diagnostic sign. Some methods for constructing generating matrices produce Hsiao codes, whose check symbols are determined by self-dual Boolean functions. The authors of [15–18] have shown that using two diagnostic signs can increase the number of test combinations in which one or another fault of the diagnostic object is manifested.

The author of [16] reports that a linear Boolean function is self-dual if it has an odd number of arguments on which it significantly depends. Therefore, among the Hsiao codes, those can be selected for which all the check symbols will have the property of self-duality of Boolean functions. Analysis of the check matrix (1) showed that codes with k = 5 can be constructed for the cases where the number of data symbols is m = 5, 7 and 11. Next, we will demonstrate how to select Hsiao codes that use self-dual Boolean functions to describe the check symbols.

3. Structure of the Concurrent Error-Detection Circuit

From (1), we derive the following system of functions describing the check symbols (check functions):

$$H_5 = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 0 \end{pmatrix}. \tag{4}$$

From (4), we derive the following system of functions describing the check symbols:

$$\begin{cases} g_1 = f_1 \oplus f_2 \oplus f_3 \oplus f_5 \oplus f_6; \\ g_2 = f_1 \oplus f_2 \oplus f_4 \oplus f_5 \oplus f_7; \\ g_3 = f_1 \oplus f_3 \oplus f_4 \oplus f_6 \oplus f_7; \\ g_4 = f_2 \oplus f_3 \oplus f_4; \\ g_5 = f_5 \oplus f_6 \oplus f_7. \end{cases} \tag{5}$$

In Formula (5), all five functions (which describe the check symbols) have an odd number of arguments. The authors of [15,16] state that any linear Boolean function is *self-dual* with an odd number of arguments. Since all five functions are self-dual, the Hsiao code encoder is a *self-dual digital device* implemented by Formula (5).

The authors of [15,16] report the method for using classical and modified Hamming codes in the synthesis of the CED according to two diagnostic signs. We implement a structure of CED using the Hsiao code, which is describing check symbols by the system (5). Figure 1 illustrates this. Block $G(f)$ is implemented by Formula (5) and is a encoder of the

Hsiao code. The cascade connection of the diagnostic object $F(x)$ and the encoder $G(f)$ result in the formation of block $G(x)$, which is then optimized further. Both devices, $G(f)$ and $G(x)$, perform identical functions, and their eponymous outputs are compared at the inputs of the comparator 5*TRC*1. This is implemented using four modules of two-rail checkers *TRC* (check pair A). The comparator operates in two-rail logic; therefore, the signals from block G(x) are previously inverted. On the other hand, the outputs of the encoder $G(f)$ are controlled by the device 5*SSC*1 (check pair B). A self-dual self-checking checker (*SSC*) has been installed on each output, and the control outputs from each self-dual checker are connected to the inputs of the 5*TRC*1 two-rail signal comparator. The outputs from two comparators (subcircuits for the testing belonging to the Hsiao codes and subcircuits for the testing the self-duality of check functions) are connected to the inputs of one module of the two-rail checker *TRC* (check pair C). The outputs of the last are the check outputs of the CED.

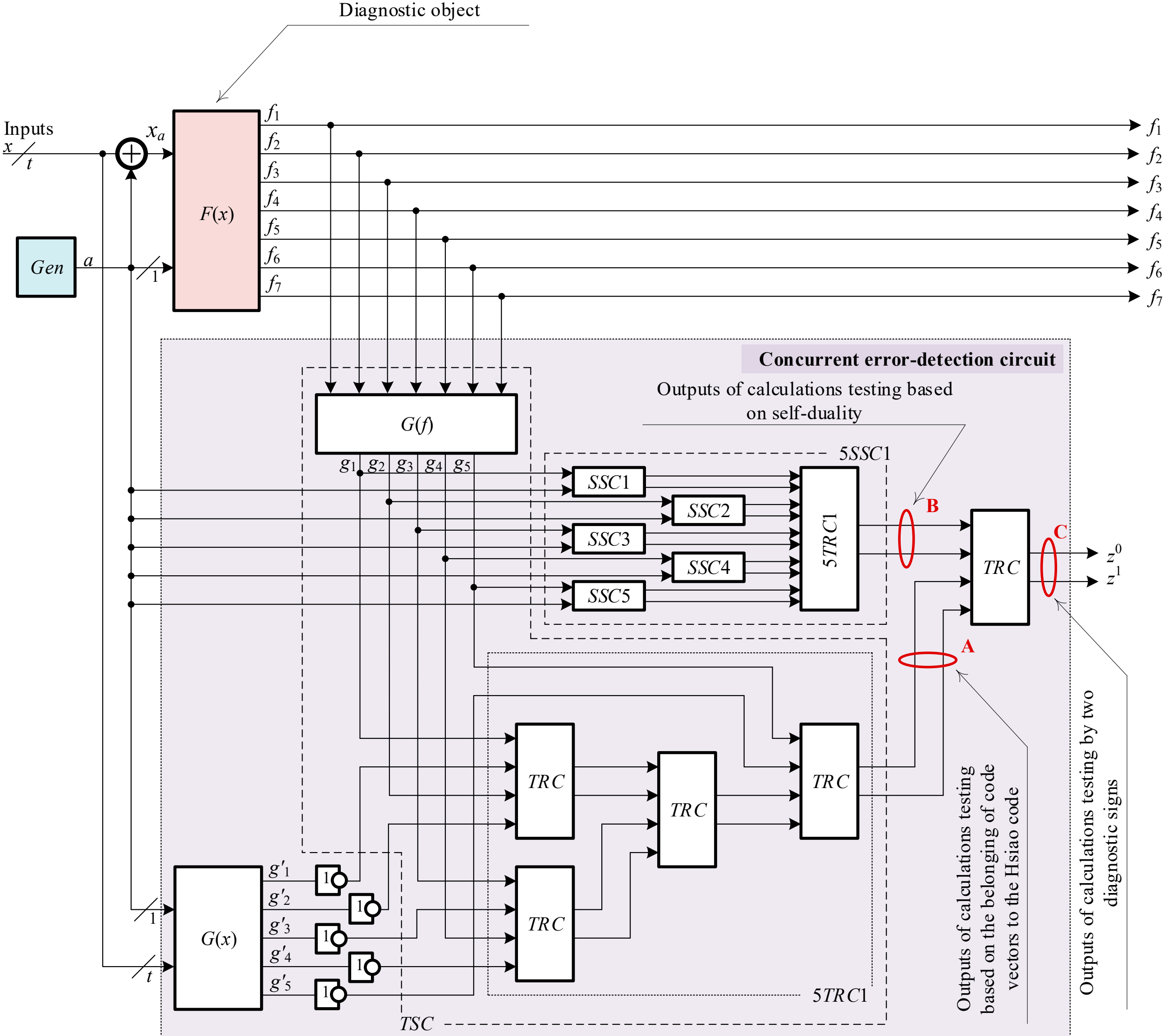

Figure 1. The structure of the organization of the CED circuit for a group of 7 outputs.

Figure 1 illustrates the basic structure, which is implemented for a group of seven outputs. The devices with $m(\text{mod}7) \neq 0$ outputs are controlled by allocating several groups of outputs. At the same time, they can be divided into groups of seven outputs

each, allowing for intersection. Individual outputs can only be controlled on the sign of self-duality.

4. Experiments with Benchmarks

We considered a non-self-dual test combination circuit (benchmark). This was implemented in the bases of *NOR* (*OR-NOT*) gates. Any Boolean function can be converted into a self-dual function with only one additional (alternative) variable a [8] required. For example, the following expression is used to convert the function $f_{NOR2} = x_1 \downarrow x_2$ [32]:

$$f^{SD}_{NOR2} = \overline{a}(\overline{x_1} \vee \overline{x_2})x_1x_2. \quad (6)$$

Therefore, a self-dual analogue can be realized by introducing structural redundancy into the source object.

Figure 2 demonstrates that by replacing each logic gate in the source circuit with a self-dual analogue, a self-dual circuit is generated.

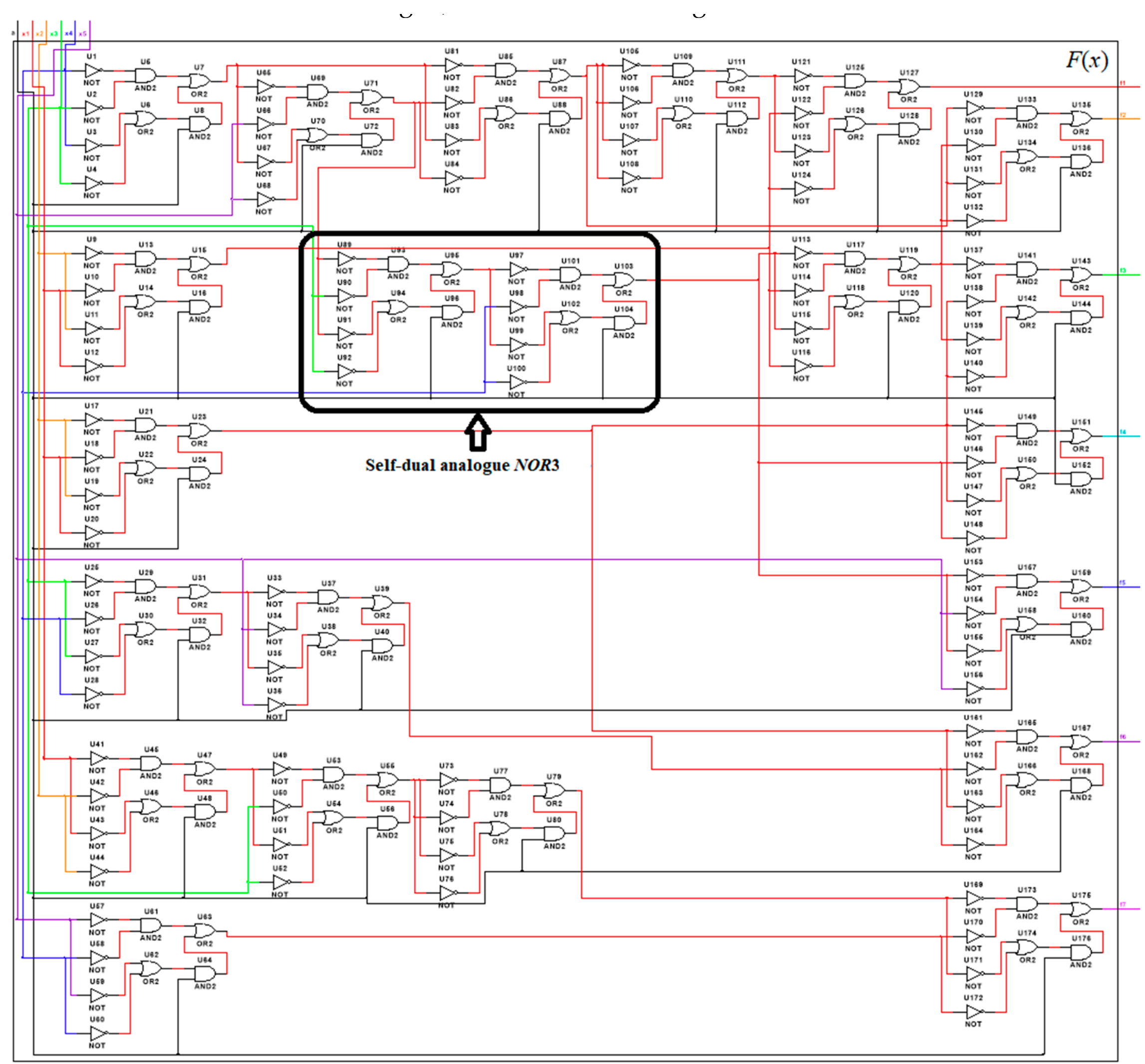

Figure 2. Self-dual combinational circuit.

Next, the CED (not provided due to cumbersomeness) was implemented according to a given structure with the testing by two diagnostic signs. Figure 1 illustrates these signs, such as testing calculations using the Hsiao codes and each checking function belonging to the class of self-dual Boolean functions. The operation of the final device was simulated

in a pulsed mode of operation, in which the input was sent pairs of $ax_1x_2x_3x_4x_5$ input combinations orthogonal by all variables to the inputs: (000000, 111111), (000001, 111110), . . ., (011111, 100000). At the same time, both regular operation and operation under the influence of a single stuck-at fault were simulated at the outputs of the self-dual analogues of the functional gates of the source circuit (total of 24 faults). We have reported the features of modeling self-dual circuits in [15,16].

Figure 3 illustrates time diagrams of the circuit operation when introducing stuck-at-0 and stuck-at-1 faults at the output of the selected cascade in Figure 2. It also shows diagrams for devices *SSC*1. . .*SSC*5 and *TRC*7. . .*TRC*9. The first five devices are self-dual checkers controlling the checking functions $g_1 \ldots g_5$. The *TRC*7 gate is a check gate of a check subcircuit regarding the self-duality of signals from gates *SSC*1. . .*SSC*5. The *TRC*8 gate is the check gate of the calculation testing subcircuit belonging to the checking functions joined with digits of the Hsiao code. The *TRC*9 gate is the check output of the CED. The outputs of the *TRC*7. . .*TRC*9 gates are of interest, as check signals can be observed on them. If a two-rail signal is violated, it indicates that an error has occurred.

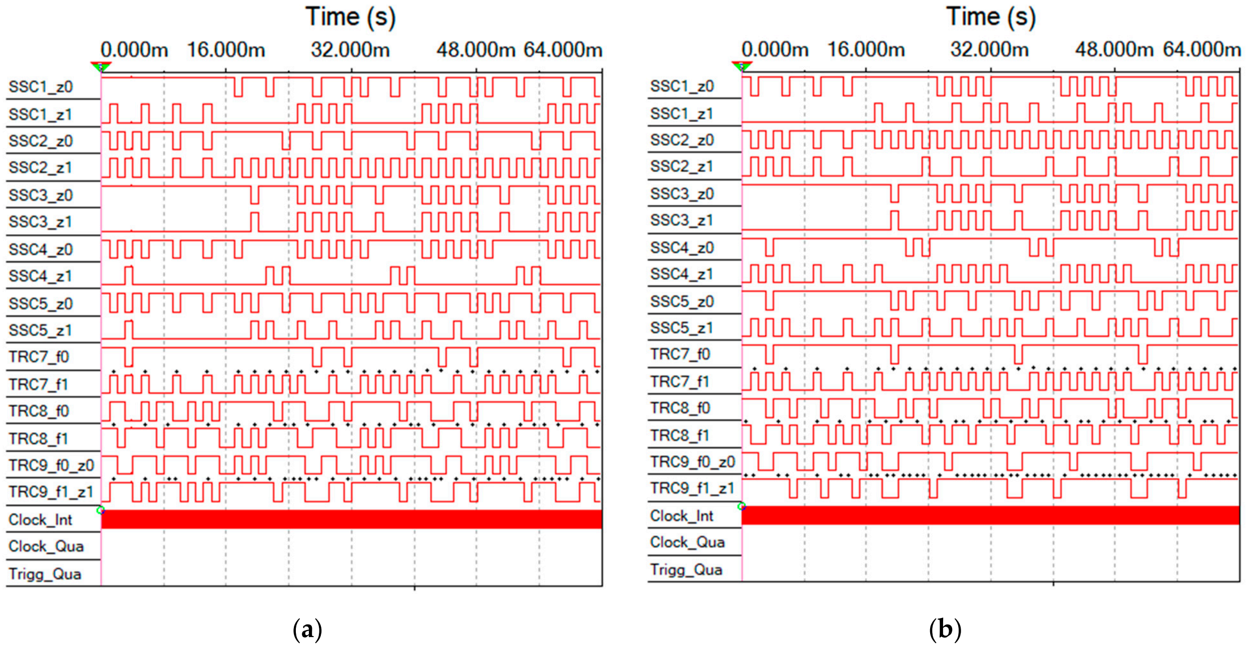

Figure 3. Time diagrams at the outputs of control devices when introducing faults into the benchmark: (**a**) stuck-at-0 at the output of the cascade selected in Figure 2; (**b**) stuck-at-1 at the output of the cascade selected in Figure 2.

Figure 3 illustrates the operation of the structure shown in Figure 1 for the given benchmark, focusing only on its control outputs. Pairs of control and check combinations are supplied to the inputs of device with a CED circuit. These combinations are presented in Tables 2 and 3. Each *SSC*1. . .*SSC*5 tester converts a serial two-rail signal into a parallel signal at outputs z0 and z1. If a two-rail signal is disrupted when a pair of combinations is applied, then a non-two-rail signal is also generated at outputs z0 and z1. This indicates an error in the calculations. The first ten signals demonstrate the operation of self-dual signal checkers on each of the diagrams. The signals from the outputs *SSC*1. . .*SSC*5 are compressed using elementary two-rail signal compression modules into a single signal. This is demonstrated in the diagrams in lines *TRC*7_f0 and *TRC*7_f1 (point B in Figure 1). The conclusion can be made based on the violation of a two-rail signal regarding the presence of an error in the calculations. We have highlighted the violation of a two-rail signal using black dots in order to facilitate the analysis of the diagrams. In parallel, the

calculations are monitored by whether the codewords belong to the Hsiao code. The signals are shown in lines *TRC*8_f0 and *TRC*8_f1 (point A in Figure 1) from the control outputs of this monitoring subcircuit. Here, too, moments of two-rail signal violation are highlighted with black dots. Moments do not always coincide with fixing errors in calculations by different subcircuits. This is what makes it possible to improve the observability of errors at the control outputs of the CED circuit. Lines *TRC*9_f0_z0 and *TRC*9_f1_z1 represent the signals at the control outputs of the entire CED circuit (point C in Figure 1). There are a total of 32 pairs of combinations on which the circuit can operate. If the calculations were based on only one diagnostic sign, for example as assumed in [26–30], the error rate would be much lower.

Table 2. Tables should be placed in the main text near to the first time they are cited.

Pair Number	$ax_1x_2x_3x_4x_5$	*TRC7* 0/1 *B*	*TRC7* 0/1 *A*	*TRC7* 0/1 *C*	Pair Number	$ax_1x_2x_3x_4x_5$	*TRC7* 0/1 *B*	*TRC7* 0/1 *A*	*TRC7* 0/1 *C*
1	000000	1/0	0/1	1/0	17	010000	1/0	1/0	0/1
	111111	1/1	1/1	1/1		101111	1/1	1/1	1/1
2	000001	1/0	1/0	0/1	18	010001	1/0	1/0	0/1
	111110	0/1	0/1	0/1		101110	1/1	1/1	1/1
3	000010	1/0	0/1	1/0	19	010010	1/0	1/0	0/1
	111101	1/1	1/1	1/1		101101	1/1	1/1	1/1
4	000011	1/0	0/1	1/0	20	010011	1/0	0/1	1/0
	111100	1/0	1/0	0/1		101100	1/1	1/1	1/1
5	000100	1/0	1/1	1/1	21	010100	1/0	1/1	1/1
	111011	1/1	0/1	1/1		101011	1/1	1/0	1/1
6	000101	1/0	0/1	1/0	22	010101	1/0	0/0	0/0
	111010	1/0	1/0	0/1		101010	0/0	0/1	0/0
7	000110	1/0	0/1	1/0	23	010110	1/0	0/1	1/0
	111001	1/1	1/1	1/1		101001	1/1	1/1	1/1
8	000111	1/0	0/1	1/0	24	010111	1/0	1/0	0/1
	111000	1/0	1/0	0/1		101000	0/0	0/0	0/0
9	001000	1/0	1/0	0/1	25	011000	1/0	1/0	0/1
	110111	1/1	1/1	1/1		100111	1/1	1/1	1/1
10	001001	1/0	1/0	0/1	26	011001	1/0	1/0	0/1
	110110	1/1	1/1	1/1		100110	1/1	1/1	1/1
11	001010	1/0	1/0	0/1	27	011010	1/0	1/0	0/1
	110101	1/1	1/1	1/1		100101	1/1	1/1	1/1
12	001011	1/0	0/1	1/0	28	011011	1/0	0/1	1/0
	110100	1/1	1/1	1/1		100100	1/1	1/1	1/1
13	001100	1/0	1/1	1/1	29	011100	1/0	1/1	1/1
	110011	1/1	1/0	1/1		100011	1/1	1/0	1/1
14	001101	1/0	0/0	0/0	30	011101	1/0	0/0	0/0
	110010	0/0	0/1	0/0		100010	0/0	0/1	0/0
15	001110	1/0	0/1	1/0	31	011110	1/0	0/1	1/0
	110001	1/1	1/1	1/1		100001	1/1	1/1	1/1
16	001111	1/0	1/0	0/1	32	011111	1/0	1/0	0/1
	110000	0/0	0/0	0/0		100000	0/0	0/0	0/0

Table 3. The results of testing the introduced fault type stuck-at-1.

Pair Number	$ax_1x_2x_3x_4x_5$	*TRC7 0/1 B*	*TRC7 0/1 A*	*TRC7 0/1 C*	Pair Number	$ax_1x_2x_3x_4x_5$	*TRC7 0/1 B*	*TRC7 0/1 A*	*TRC7 0/1 C*
1	000000	1/0	1/1	1/1	17	010000	1/0	1/1	1/1
	111111	1/1	1/0	1/1		101111	1/1	0/1	1/1
2	000001	1/0	1/0	0/1	18	010001	1/0	0/0	0/0
	111110	0/1	0/1	0/1		101110	0/0	0/1	0/0
3	000010	1/0	1/1	1/1	19	010010	1/0	1/1	1/1
	111101	1/1	1/0	1/1		101101	1/1	0/1	1/1
4	000011	1/0	0/1	1/0	20	010011	1/0	1/1	1/1
	111100	1/0	1/0	0/1		101100	1/1	1/0	1/1
5	000100	1/0	1/0	0/1	21	010100	1/0	0/1	1/0
	111011	1/1	1/1	1/1		101011	1/1	1/1	1/1
6	000101	1/0	0/1	1/0	22	010101	1/0	1/0	0/1
	111010	1/0	1/0	0/1		101010	1/1	1/1	1/1
7	000110	1/0	1/1	1/1	23	010110	1/0	1/1	1/1
	111001	1/1	1/0	1/1		101001	1/1	1/0	1/1
8	000111	1/0	0/1	1/0	24	010111	1/0	1/1	1/1
	111000	1/0	1/0	0/1		101000	1/1	0/1	1/1
9	001000	1/0	1/1	1/1	25	011000	1/0	1/1	1/1
	110111	1/1	0/1	1/1		100111	1/1	0/1	1/1
10	001001	1/0	0/0	0/0	26	011001	1/0	0/0	0/0
	110110	0/0	0/1	0/0		100110	0/0	0/1	0/0
11	001010	1/0	1/1	1/1	27	011010	1/0	1/1	1/1
	110101	1/1	0/1	1/1		100101	1/1	0/1	1/1
12	001011	1/0	1/1	1/1	28	011011	1/0	1/1	1/1
	110100	1/1	1/0	1/1		100100	1/1	1/0	1/1
13	001100	1/0	0/1	1/0	29	011100	1/0	0/1	1/0
	110011	1/1	1/1	1/1		100011	1/1	1/1	1/1
14	001101	1/0	1/0	0/1	30	011101	1/0	1/0	0/1
	110010	1/1	1/1	1/1		100010	1/1	1/1	1/1
15	001110	1/0	1/1	1/1	31	011110	1/0	1/1	1/1
	110001	1/1	1/0	1/1		100001	1/1	1/0	1/1
16	001111	1/0	1/1	1/1	32	011111	1/0	1/1	1/1
	110000	1/1	0/1	1/1		100000	1/1	0/1	1/1

In addition to Figure 3, Tables 2 and 3 list all pairs of combinations supplied to the device inputs. The background color indicates which input combinations are used for testing the corresponding faults. These combinations are tested (the output signals on the corresponding check device are the same on such input combinations). The corresponding combinations are also shown in Figures 3 and 4 as dots on the corresponding clock cycle. When the circuit is operating with a stuck-at-0 fault at the output of the designated cascade in Figure 2, 28 input combinations are checked using one of two diagnostic signs (43.75% of the total number of combinations). Checking by two signs allows for increasing the number of test combinations to 35 (54.69% of the total number of combinations). When the circuit is operating with a stuck-at-1 fault at the output of the cascade designated in Figure 2, 28 input combinations are also checked using each of the signs (43.75% of the total number of combinations). Checking by two signs increases this number to 49 (76.56% of the total number of combinations). For the stuck-at-0 fault, an improvement of about 11% was achieved; for the stuck-at-1 fault, an improvement of about 33% was achieved.

The calculations testing with two diagnostic signs makes it possible in all cases to increase the controllability of circuits. This allows for a higher probability of detecting emerging faults when using a subset of the full input combinations set. This indicates the

potential applicability of the described approach for calculations testing in devices with inputs that rarely change, which is common for many safety-critical systems [33,34].

Figure 4 shows a histogram that allows us to judge the increase in the controllability of the circuit due to the organization of calculations testing by two diagnostic signs and not by one of them. On average, 40.104% of the input combinations are also tested when testing by one sign of all faults. This number increase to 60.156% when the calculations are testing by two signs. Thus, the number of test combinations on average increased by 1.5 times. The columns (highlighted in blue) correspond to the operation of the CED circuit only according to whether the generated codewords belong to the Hsiao codes. Thus, the observability of errors at the outputs is significantly increased in contrast to traditional structures of computing control organization [26–30] due to the monitoring of several diagnostic signs at once. This demonstrates the effectiveness of the technical solution proposed by the authors of this paper. At the same time, it should be noted that we do not use any modifications of the Hsiao code but apply its natural properties. These properties consist of the fact that under certain conditions, the check symbols can be described by self-dual Boolean functions.

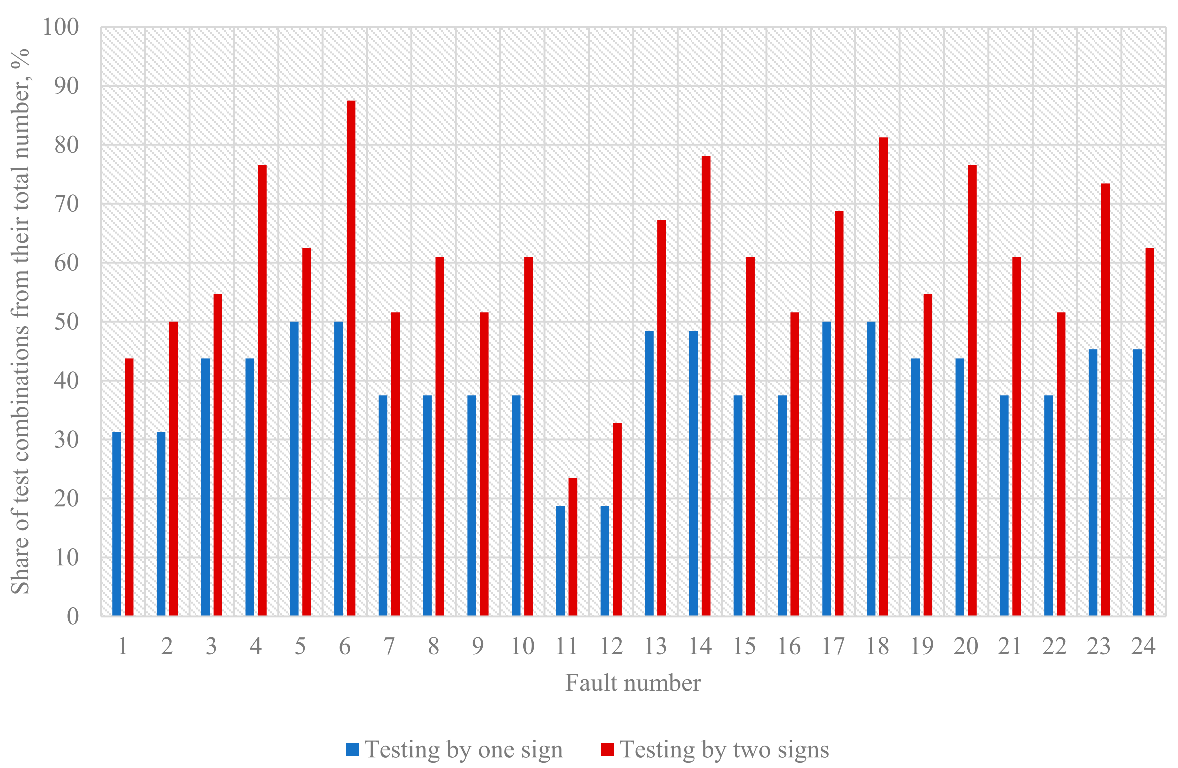

Figure 4. Histogram of the distribution of the shares of test combinations from their total number when calculations testing by one and two diagnostic signs.

5. Discussion

Hsiao codes are commonly employed in the construction of structures with error detection and correction [24–28]. Nevertheless, all applications of these codes are limited to the properties of the code itself for detecting and correcting errors in data symbols. The authors of this paper point out that Hsiao codes possess another diagnostic property that can be effectively used in the design of CED circuits. The research conducted by the authors has demonstrated that Hsiao codes can be effective for use in the synthesis of CED circuits for self-dual digital devices. It has also been found that calculations testing is highly effective when based on two diagnostic signs. The check functions belong to the class of self-dual Boolean functions, and the code vector belongs to the Hsiao code that is generated in a CED circuit. This is supported by numerous experiments, one example of

which is provided in Section 4 of the paper. Figure 4 shows that the calculations testing increases the detection abilities of the CED circuit by simultaneously using two diagnostic signs. For various circuits, the improvement is between 20% and 25%. In addition, control indicators have been significantly increased in terms of fault detection. This indicates possible prospects for applying the developed method of circuit synthesis based on two diagnostic signs in the design of highly reliable devices for critical systems.

It is important to note the following feature of Hsiao codes: they have a lower coding rate compared to classic Hamming codes, which affects the hardware cost of designing a CED circuit. Figure 1 illustrates the structure of a CED circuit, where a group of seven diagnostic object outputs is controlled by compressing signals into five using a Hsiao code encoder. Structures for larger numbers of discrete device outputs can be proposed, and the structural redundancy can be reduced of the self-testing device. There will be a significant difference between the values of m and k in this case. The author of [14] reports that the self-dual signal compression circuit can be used along with a single self-dual signal checker instead of a group of self-dual signal checker in the structure illustrated in Figure 1. This would simplify the structure of the CED circuit.

Note also that the structure depicted in Figure 1 is a special type of structure and is designed for a group of seven outputs from the diagnostic object. Using other Hsiao codes would allow for the creation of similar structures with more outputs and different lengths of data vectors. Table 4 present the ratio of the number of ways to construct Hsiao codes for the case $k = 5$, which has self-dual encoder properties. Researchers have shown that such Hsiao codes can only be generated for cases $m = 5, 7$ and 11. Row $N_{k,m}^{SD}$ shows the number of Hsiao codes with self-dual encoders. Row $N_{k,m}$ shows the total number of Hsiao codes. Row ω calculates the relative indicator of the number of Hsiao codes with self-dual encoders compared to the total number of Hsiao codes: $\omega = N_{k,m}^{SD}/N_{k,m} \cdot 100$ %. The last column of the table shows the total values of $\sum_{m=5}^{11} N_{k,m}^{SD}$, $\sum_{m=5}^{11} N_{k,m}$ and $\overline{\omega} = \sum_{m=5}^{11} N_{k,m}^{SD} / \sum_{m=5}^{11} N_{k,m} \cdot 100$ %. There are only 52 ways to construct Hsiao codes using self-dual encoders from a total of 1486 Hsiao codes with $k = 5$. This number of ways to construct Hsiao codes using self-dual encoders is relatively small compared to the total number. Nevertheless, this provides 52 ways of synthesizing a CED circuit based on two diagnostic signs. Hsiao codes with large $k > 5$ values can also be considered. Furthermore, as the k value increases, there are increasing numbers of Hsiao codes available. Among these, codes can be implemented with self-dual functions describing check symbols.

Table 4. Hsiao codes with self-dual encoders at $k = 5$.

Indicator	m							Total with $k = 5$
	5	6	7	8	9	10	11	
$N_{k,m}^{SD}$	27	0	24	0	0	0	1	52
$N_{k,m}$	462	462	330	165	55	11	1	1486
ω, %	5.844	0	7.273	0	0	0	100	3.499

It is also worth noting the error-detecting properties of the Hsiao codes. These codes are able to identify any errors that occur in codewords bits with multiplicities $d < 4$. Hsiao codes have a much higher effectiveness at detecting errors in the area with small multiplicities compared to classical Hamming codes. This allows for the synthesis of CED circuits with high efficiency indicators of errors detection efficiency at the outputs of diagnostic objects. However, the Hsiao codes are inferior to the Hamming codes in terms of the code rate. They always have one more check symbol than the classic Hamming

codes. However, this may be seen as a consequence of the high level of error detection efficiency in the CED circuit. At the same time, there is a slight increase in the additional cost associated with synthesis and the structural redundancy in the CED circuit (a larger number of self-dual checkers, two-rail checker modules, as well as a slightly more complex control logic block are required).

Additionally, it is important to discuss the disadvantages of employing the method described in the paper. This method involves pulsed operation, which necessitates a specific representation of signals. This task can be solved by simply installing a square-wave generator and configuring the circuit operation. The combinations are supplied in pairs with every first clock cycle representing data and every second clock cycle performing a check. This reduces the performance of the devices with CED circuits by half compared to the traditional way of organizing CED circuits. Additionally, we would like to stress a point that in order to organize the CED circuit according to the proposed method, it will be necessary to transform the structure of a non-dual diagnosis object into a self-dual structure. This, of course, is a relatively simple process, but it can lead to an increased device redundancy [14]. The Boolean correction of signals can also be applied to check non-dual structures of diagnostic objects [16]. Another disadvantage of the proposed method is that it may introduce complexity. These is commensurate with or exceeds that of the widely used duplication approach. And it may prove to be ineffective in terms of structural redundancy when used for modeling and evaluating efficiency indicators of CED circuits.

In future research, the authors intend to analyze other features of the Hsiao codes. These features can be considered when designing highly reliable devices. Additionally, we also intend to develop a methodology for the synthesis of real control devices for the implementation of critical technological processes using parallel CED circuits based on two diagnostic signs.

6. Conclusions

The Hsiao codes possess the ability to detect any one-, two- and three- fold errors in the bits of codewords. These codes are characterized by the property of self-dual functions (which describe check symbols) under certain conditions. Therefore, the Hsiao codes can be used in the design of CEDs with calculations testing by two diagnostic signs. This increases the structural redundancy indicators of the CED, but the number of test combinations increases significantly. These combinations are both operating for the device.

The structural redundancy does not significantly increase. A self-duality check device for Boolean functions is included in the CED in addition to the Hsiao code checker. This device has the simplest typical implementation. The authors of [15,16] describe the principle of operation and structure of the self-duality checker. The complexity indicators for the technical implementation of the standard part of the CED increase linearly as the number of outputs from the diagnostic object (source device) increases. Controllability indicators also increase with various faults in different ways and can reach an increase of 1.5–1.8 times when faults are observed at the device's outputs.

The Hsiao codes are of interest with self-dual check functions in the development of self-checking digital computing devices and systems, and, importantly, critical application systems, for which the input data rarely change.

Author Contributions: Conceptualization, D.V.E.; methodology, D.V.E.; validation, D.V.E.; formal analysis, T.S.P. and D.V.E.; investigation, N.M.A. and D.V.E.; writing—original draft preparation, T.S.P. and D.V.E.; writing—review and editing, D.V.E., A.R.A. and S.T.B.; visualization, E.K.A. and F.F.S.; supervision, D.V.E.; project administration, E.K.A. and F.F.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Gavzov, D.V.; Sapozhnikov, V.V.; Sapozhnikov, V.V. Methods for Providing Safety in Discrete Systems. *Autom. Remote Control* **1994**, *55*, 1085–1122.
2. Ubar, R.; Raik, J.; Vierhaus, H.-T. *Design and Test Technology for Dependable Systems-on-Chip (Premier Reference Source)*; Information Science Reference; IGI Global: Hershey, PA, USA; New York, NY, USA, 2011; p. 578.
3. Dubrova, E. *Fault-Tolerant Design*; Springer Science+Business Media: New York, NY, USA, 2013; p. XV+185. [CrossRef]
4. Hahanov, V. *Cyber Physical Computing for IoT-driven Services*; Springer International Publishing AG: New York, NY, USA, 2018; p. 279.
5. Bestemyanov, P.F. Methods of Providing Hardware Safety for Microprocessor Train Control Systems. *Russ. Electr. Eng.* **2020**, *91*, 531–536. [CrossRef]
6. Drozd, O.; Romankevich, V.; Kuznietsov, M.; Drozd, M.; Martynyuk, O. Using Natural Version Redundancy of FPGA Projects in Area of Critical Applications. In Proceedings of the IEEE 11th International Conference on Dependable Systems, Services and Technologies, Kyiv, Ukraine, 14–18 May 2020; pp. 58–64. [CrossRef]
7. Reynolds, D.A.; Meize, G. Fault Detection Capabilities of Alternating Logic. *IEEE Trans. Comput.* 1978; C-27, 1093–1098.
8. Aksjonova, G.P. Restoration in Duplicated Units by the Method of Data Inversion. *Autom. Remote Control* **1987**, 144–153.
9. Goessel, M.; Dmitriev, A.V.; Sapozhnikov, V.V.; Sapozhnikov, V.V. A Functional Fault-Detection Self-Test for Combinational Circuits. *Autom. Remote Control* **1999**, *60*, 1653–1663.
10. Sogomonyan, E.S.; Gössel, M. Design of Self-Testing and On-Line Fault Detection Combinational Circuits with Weakly Independent Outputs. *J. Electron. Test. Theory Appl.* **1993**, *4*, 267–281. [CrossRef]
11. Saposhnikov, V.V.; Morosov, A.; Saposhnikov, V.V.; Göessel, M. A New Design Method for Self-Checking Unidirectional Combinational Circuits. *J. Electron. Test. Theory Appl.* **1998**, *12*, 41–53. [CrossRef]
12. Matrosova, A.Y.; Levin, I.; Ostanin, S.A. Self-Checking Synchronous FSM Network Design with Low Overhead. *VLSI Des.* **2000**, *11*, 47–58. [CrossRef]
13. Saposhnikov, V.V.; Moshanin, V.; Saposhnikov, V.V.; Goessel, M. Experimental Results for Self-Dual Multi-Output Combinational Circuits. *J. Electron. Test. Theory Appl.* **1999**, *14*, 295–300. [CrossRef]
14. Dmitriev, A.; Saposhnikov, V.; Sapozhnikov, V.; Goessel, M.; Moshanin, V.; Morosov, A. New Self-Dual Circuits for Error Detection and Testing. *VLSI Des.* **2000**, *11*, 1–21. [CrossRef]
15. Efanov, D.V.; Pogodina, T.S. Self-Dual Digital Devices with Calculations Testing by Modified Hamming Code. In Proceedings of the 2023 Conference of Russian Young Researchers in Electrical and Electronic Engineering (ElConRus), St. Petersburg, Russia, 24–27 January 2023; pp. 72–77.
16. Efanov, D.; Pogodina, T. Properties Investigation of Self-Dual Combinational Devices with Calculation Control Based on Hamming Codes. *Inform. Autom.* **2023**, *22*, 349–392. [CrossRef]
17. Efanov, D.; Sapozhnikov, V.; Sapozhnikov, V.; Osadchy, G.; Pivovarov, D. Self-Dual Complement Method up to Constant-Weight Codes for Arrangement of Combinational Logical Circuits Concurrent Error-Detection Systems. In Proceedings of the 17th IEEE East-West Design & Test Symposium (EWDTS'2019), Batumi, Georgia, 13–16 September 2019; pp. 136–143. [CrossRef]
18. Efanov, D.V.; Pivovarov, D.V. The Hybrid Structure of a Self-Dual Built-In Control Circuit for Combinational Devices with Pre-Compression of Signals and Checking of Calculations by Two Diagnostic Parameters. In Proceedings of the 19th IEEE East-West Design & Test Symposium (EWDTS'2021), Batumi, Georgia, 10–13 September 2021; pp. 200–206. [CrossRef]
19. Goessel, M.; Morozov, A.V.; Sapozhnikov, V.V.; Sapozhnikov, V.V. Logic Complement, a New Method of Checking the Combinational Circuits. *Autom. Remote Control* **2003**, *1*, 153–161. [CrossRef]
20. Goessel, M.; Morozov, A.V.; Sapozhnikov, V.V.; Sapozhnikov, V.V. Checking Combinational Circuits by the Method of Logic Complement. *Autom. Remote Control* **2005**, *66*, 1336–1346. [CrossRef]
21. Göessel, M.; Ocheretny, V.; Sogomonyan, E.; Marienfeld, D. *New Methods of Concurrent Checking*, 1st ed.; Springer Science+Business Media B.V.: Dordrecht, The Netherlands, 2008; p. 184.
22. Hamming, R.W. Error Detecting and Correcting Codes. *Bell Syst. Tech. J.* **1950**, *29*, 147–160. [CrossRef]
23. Hsiao, M.Y. A Class of Optimal Minimum Odd-Weight-Column SEC-DED Codes. *IBM J. Res. Dev.* **1970**, *14*, 395–401. [CrossRef]

24. Tshagharyan, G.; Harutyunyan, G.; Shoukourian, S.; Zorian, Y. Experimental Study on Hamming and Hsiao Codes in the Context of Embedded Applications. In Proceedings of the 15th IEEE East-West Design & Test Symposium, Novi Sad, Serbia, 29 September–2 October 2017; pp. 25–28. [CrossRef]
25. Sim, M.T.; Zhuang, Y. Design of Two Interleaved Error Detection and Corrections Using Hsiao Code and CRC. In Proceedings of the IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, Singapore, 18–21 October 2020. [CrossRef]
26. Aymen, F.; Belgacem, H.; Chiraz, K.A. New Efficient Self-Checking Hsiao SEC-DED Memory Error Correcting Code. In Proceedings of the ICM 2011 Proceeding, Hammamet, Tunisia, 19–22 December 2011; pp. 1–5. [CrossRef]
27. Novac, O.; Vari-Kakas, S.; Hathazi, F.; Curila, M.; Curila, S. Aspects Regarding the Implementation of Hsiao Code to the Cache Level of a Memory Hierarchy with FPGA Xilinx Circuits. In *Advanced Techniques in Computing Sciences and Software Engineering*; Elleithy, K., Ed.; Springer: Dordrecht, The Netherlands, 2010; pp. 539–543. [CrossRef]
28. Novac, O.C.; Sztrik, J.; Vari-Kakas, S.; Kim, C.-S. Reliability Increasing Method Using a SEC-DED Hsiao Code to Cache Memories, Implemented with FPGA Circuits. *J. Comput. Sci. Control. Syst.* **2011**, *4*, 59–62.
29. Sahana, A.R.; Chiraag, V.; Suresh, G.; Thejaswini, P.; Nandi, S. Application of Error Detection and Correction Techniques to Self-Checking VLSI Systems: An Overview. In Proceedings of the 2023 IEEE Guwahati Subsection Conference (GCON), Guwahati, India, 23–25 June 2023. [CrossRef]
30. Chioktour, V.; Kakarountas, A. Adaptive BIST for Concurrent On-Line Testing on Combinational Circuits. *Electronics* **2022**, *19*, 3193. [CrossRef]
31. Fujiwara, E. *Code Design for Dependable Systems: Theory and Practical Applications*; J. Wiley & Sons: Hoboken, NJ, USA, 2006; p. 720.
32. Moshanin, V.; Saposhnikov, V.V.; Saposhnikov, V.V.; Gossel, M. Synthesis of Self-Dual Multi-Output Combinational Circuits for On-Line Testing. In Proceedings of the 2nd IEEE International On-Line Testing Workshop, Biarritz, France, 8–10 July 1996.
33. Drozd, A.; Kharchenko, V.; Antoshchuk, S.; Sulima, J.; Drozd, M. Checkability of the Digital Components in Safety-Critical Systems: Problems and Solutions. In Proceedings of the 9th IEEE East-West Design & Test Symposium, Sevastopol, Ukraine, 9–12 September 2011; pp. 411–416. [CrossRef]
34. Sapozhnikov, V.V. *Synthesis of Train Traffic Control Systems at Railway Stations with the Exception of Dangerous Failures*; Publishing House «Nauka»: Moscow, Russia, 2021; p. 229.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.