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Field Programmable Gate Array Applications—A Scientometric Review

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Abstract: Field Programmable Gate Array (FPGA) is a general purpose programmable logic device that can be configured by a customer after manufacturing to perform from a simple logic gate operations to complex systems on chip or even artificial intelligence systems. Scientific publications related to FPGA started in 1992 and, up to now, we found more than 70,000 documents in the two leading scientific databases (Scopus and Clarivative Web of Science). These publications show the vast range of applications based on FPGAs, from the new mechanism that enables the magnetic suspension system for the kilogram redefinition, to the Mars rovers' navigation systems. This paper reviews the top FPGAs' applications by a scientometric analysis in ScientoPy, covering publications related to FPGAs from 1992 to 2018. Here we found the top 150 applications that we divided into the following categories: digital control, communication interfaces, networking, computer security, cryptography techniques, machine learning, digital signal processing, image and video processing, big data, computer algorithms and other applications. Also, we present an evolution and trend analysis of the related applications.

Keywords: FPGA; Field Programmable Gate Array; applications; digital control; networking; security; machine learning; big data; image processing; ScientoPy

1. Introduction

A Field Programmable Gate Array (FPGA) is a general purpose programmable logic device that contains logic blocks whose interconnection and functionality can be configured by a customer or a designer after manufacturing [1]. In this way, we can build inside an FPGA from a simple logic gate to a complex systems on chip or even a artificial intelligence system. As a result, FPGAs have been used for many different application such as digital signal processing [2–4], image processing [5–7], cryptography [8–10], parallel processing [11,12], fault tolerance systems [13–15], low power systems [16,17], simulation [18–20], digital control [21–23], artificial intelligence [24–26], networking [27,28], big data [29–32], among others.

Nowadays, we found several literature reviews and survey papers for different FPGAs applications like industry [33–35], power Electronics [36], fault tolerance [14,37–39], partial reconfiguration [40], photovoltaic systems [41], Sensors system based [42,43], network infrastructure security [44], LDPC (low-density parity-check) decoders [45], CORDIC algorithms [46], cryptography [8,47], deep learning [48–51], digital modulation techniques [52], low power design [53], robotic controllers [54], automotive safety [55], digital filters [56,57], Unmanned Aerial Vehicles (UAV) [58,59] and random number generators [60]. Similarly, we found books that summarize FPGAs' applications for scientific research [61,62]. These previous studies found in the related papers show the review of specific topics inside FPGA applications and the related books review some FPGAs'

applications with practical examples but do not include the top applications like image processing and machine learning.

Thus, the propose of this study is to provide an extensive overview of the top FPGAs' applications by a scientometric review, covering publications related to FPGA from 1992 to 2018. Correspondingly, in this paper, the main FPGAs' applications are divided into eleven main categories and five subcategories. Figure 1 shows an overview of this paper. Section 2 presents the materials and methods used to extract the bibliographic dataset, preprocessing steps and type of analysis performed. Sections 3–13 show the eleven FPGAs' applications categories, Section 14 illustrates the relationship between the main FPGA-based applications and implementations and Section 15 discusses the main findings of this study.

Paper organization

- 2. Materials and Methods
- 3. Digital Control
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Figure 1. Organization of the paper.

2. Materials and Methods

In this section, we describe the dataset collection, including the preprocessing steps and the review methodology that we used to analyze the dataset collected for this review.

2.1. Dataset Collection

We built the dataset using two bibliographic databases: Clarivate Web of Science (WoS) and Scopus. The search string for this analysis was: "Field-programmable gate array*" OR "Field programmable gate array*" OR "FPGA*". We applied this string to the topic search in WoS and Scopus, which includes title, abstract, author's keywords and KeyWords Plus® (for WoS). With this search criteria, we downloaded the data set within a day on 19th March 2019. Then, we preprocessed it in ScientoPy. Figure 2 shows the preprocess brief graph that presents the entire loaded documents for each database and the removed duplicated documents, respectively. Since the ScientoPy preprocessing script keeps WoS documents over Scopus documents, after the duplication removal, we see more documents from WoS than Scopus databases.

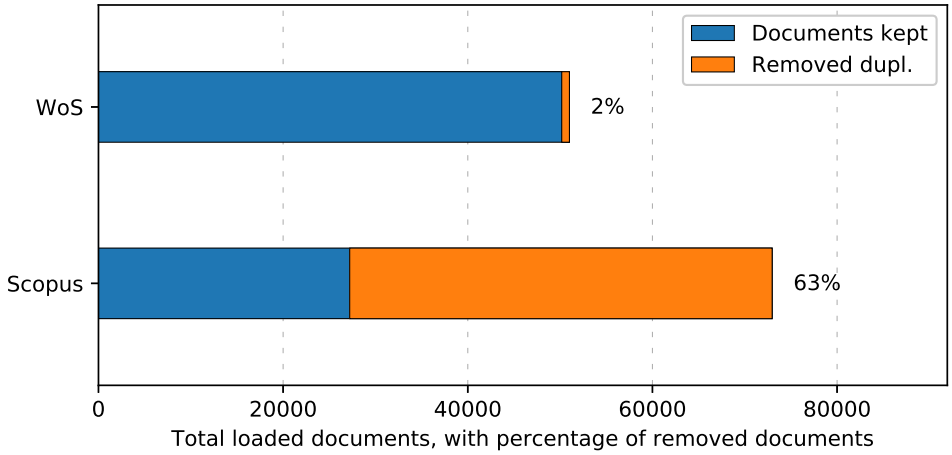

Figure 2. Field Programmable Gate Array (FPGA) total loaded documents from Clarivate Web of Science (WoS) and Scopus databases, with the percentage of removed documents after duplication removal filter.

Table 1 shows the brief preprocessing table generated by ScientoPy. This table describes the input dataset including in the second column (*Number*) the number of publications after and before the duplication removal filter per database, and the third column (*Percentage*) the relative percentages (see table description for detailed information about these percentages). *Loaded papers* represents the total number of documents loaded from both databases. *Omitted papers by document type* are the number of documents outside the default documents type filter (only including conference papers, articles, reviews, proceedings papers and articles in press). *Papers after omitted papers removed* are the number of documents inside the default documents type filter. *Loaded papers from WoS/Scopus* are the number of documents from each database after the omitted papers had been removed. *Duplicated papers found* are the duplicated total number of documents that have been found and removed. *Removed duplicated papers from WoS/Scopus* are the number of documents removed from each database after the duplication removal. *Total number of papers after rem. dupl.* are the number of documents after duplication removal by the preprocessing. Finally, *Papers from WoS/Scopus* are the whole number of documents from WoS and Scopus, respectively, after the duplication removal. The duplication removal filter used by ScientoPy is based on the DOI match or if the DOI is not present in the documents' title and documents' first author last name match.

Table 1. FPGA dataset preprocess brief table. *Omitted papers by document type*, *Loaded papers from WoS/Scopus* and *Duplicated papers found* percentage relative to *Loaded papers*. *Removed duplicated papers from WoS/Scopus* percentages relative to *Loaded papers from WoS/Scopus* respectively. *Papers from WoS/Scopus* percentage relative to *Total number of papers after rem. dupl.*

Information	Number	Percentage
Loaded papers	127,597	
Omitted papers by document type	3621	2.8%
Papers after omitted papers removed	123,976	
Loaded papers from WoS	51,010	41.1%
Loaded papers from Scopus	72,966	58.9%
Duplicated removal results:		
Duplicated papers found	46,592	37.6%
Removed duplicated papers from WoS	836	1.6%
Removed duplicated papers from Scopus	45,756	62.7%
Total number of papers after rem. dupl.	77,384	
Papers from WoS	50,174	64.8%
Papers from Scopus	27,210	35.2%

2.2. Review Methodology

Manual scientific reviews such as systematic and literature reviews have limitations to cover a vast research area such as FPGAs based applications completely. For this reason, we used a scientometric review methodology. Using ScientoPy, we extracted and analyzed the top applications and implementations based in FPGAs [63]. We took the total 77,384 papers' bibliographic information to perform a scientometric analysis with ScientoPy to extract the first 5000 top author's keywords. Then, we extracted the author's keywords related to FPGAs' applications from this list to arrange them into eleven different categories (digital control, communication interface, networking, computer security, machine learning, digital signal processing, image and video processing, computer algorithms, other implementations and other applications).

Then, we analyze in depth each category by extracting with ScientoPy the statistical graph corresponding to the most used author's keywords for each topic. In that way, for instance, in the Machine learning section, we got the ScientoPy statistical graph for the top author's keywords related to machine learning techniques developed in FPGAs. The author's keywords that we present in the graphs represent the group of similar author keywords that belong to the same topic, such as abbreviations, plural/singular words or dashes between words. For example, in machine learning, we got the "support vector machine" phrase (enclosing: support vector machine, SVM, support vector machines) or in Computer security/Cryptography we got RSA (enclosing: RSA, Rivest-Shamir-Adleman (RSA), Rivest-Shamir-Adleman, Rivest Shamir Adleman).

For the topic trending analysis, we use here two indicators. The Average Documents per Year (ADY) that is the average number of documents published in each specific topic in the last three years (2016–2018). This indicator represents the topic absolute-number of publications growth and generally is high when we have a high positioned topic. Unfortunately, this is not a good indicator of a new trending topic, in which absolute growth is generally low but its relative growth is high. For these cases, we have the second indicator called Percentage of Documents in the Last Years (PDLY) that represents the percentage of documents published in the last three years (2016–2018) for a specific topic relative to the total number of documents published for this topic. Therefore, we extracted the statistical graphs from ScientoPy using these indicators, with graphs divided into two categories:

- **Parametric evolution graph:** this graph has two parts. The first part (left side) presents the accumulative number of documents (or papers) versus the publication year of each topic (in this case author's keywords). With this graph, we can observe the starting year at the line's start and the total number of documents at the line's end. In some graphs, we put the Y-axes on a logarithmic scale to note the starting year of each topic easily. On the right side, we get the parametric plot. Here, we present the ADY and PDLY of each topic, to show the growth of the total number of documents (ADY) and the relative growth (PDLY) in the last years.
- **Trending bar graph:** if we need to analyze many topics in a specific section (usually more than ten topics), we use this kind of graph. Here we present the different topics in the Y-axis related to the total number of documents per topic in the X-axis with bars. Also, here we highlight in orange in the bar the documents published in the last three years (in this case 2016 to 2018), including the PDLY value.

Finally, for the analysis of the topics, we include the definition of each topic, the specific implementations or applications with FPGAs related to the topics and the citation of the papers that includes the related implementation or application. Here, we cited the most relevant to the application, the ones with more citations and the newest papers for each specific application.

3. Digital Control

Digital control uses digital systems to act as system controllers to control a system in an optimum manner without delay or overshot and ensuring stability [64]. Implementation of this kind of controllers in FPGAs allows highly parallel, high-speed processing and shorter delays. Most of

the documents listed here are related to fuzzy control and Proportional Integral Derivative (PID) control. Nevertheless, sensorless control has the highest PDLY and model predictive control has the highest ADY (see Figure 3). Fuzzy control has been implemented in FPGAs to comply with the requirements of high-sampling-frequency control systems such as permanent-magnet synchronous motor drives [65], vehicle semi-active suspension system [66] or Continuous Variable Camshaft Timing (CVCT) system [67]. PID implementations in FPGAs allows high-speed and high-precision systems developed for DC-DC voltage converters [68,69], nuclear fast reactors [70] and even for the controller of the magnetic suspension mass comparator system (MSMC) used for the redefinition of the kilogram at the National Institute of Standards and Technology [71].

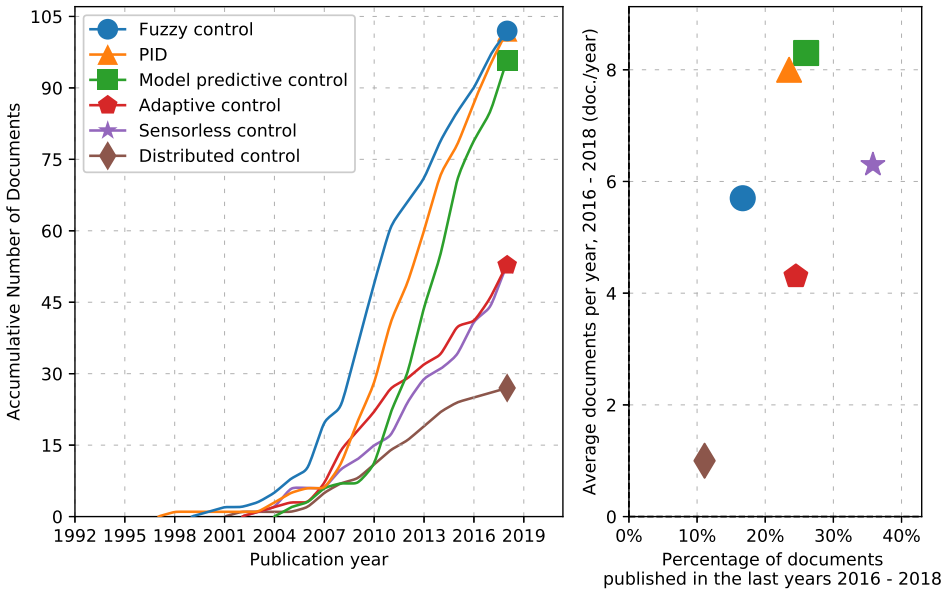

Figure 3. Digital control top implementations in FPGA research.

The Model Predictive Control (MPC) uses a model to predict the process output at future time instants to calculate a control sequence for minimizing an objective function [72]. MPC is a quadratic programming (QP) problem, where two critical factors determine the success of MPC applications: the availability of a suitable plant model and the ability to solve the quadratic programming problem within the prescribed sampling period [73]. The QP implementation in FPGAs provides an accurate real-time closed-loop simulation that meets the control deadlines [74]. This kind of implementations includes torque control at very low and zero speed [75], three-phase inverters [76,77] or spacecraft rendezvous in elliptical orbits [78].

In the adaptive control, the controller adapts to a controlled system with parameters that can vary or are uncertain, such as an airplane where its mass change as a result of the fuel consumption [79]. These control systems have been implemented using FPGAs in robotics applications [80–83], tunnel lighting systems [84], microgrids [85] and chaotic systems [86,87]. Sensorless control publications involve, for example, electrical motor speed and position control techniques that do not need a physical sensor. These techniques estimate the rotor position and speed by using algorithmic estimator techniques divided into two—the high-frequency injection method and the estimation-based techniques [88]. The estimation-based techniques use the Extended Kalman Filter (EKF) for position estimation due to its ability to extract the needed data from a random-noisy environment [89]. Real-time system based on FPGAs are used to implement the EKF matrix operations [89], vector controller [90,91] and FPGA's oversampling technique for a flux observer [92–94].

Distributed control techniques are designed to process decentralized systems for distributed cells, where each cell processes different types of information. Each cell has autonomy in local optimization and also all integrate a large complex system [95]. FPGA-based distributed control techniques

have been used for applications like micro-electromechanical systems arrays for air-flow planar micro-manipulation [96], music playing robots [97–99], telescopes control [100] and for reconfigurable FPGA-based systems [101–103].

4. Communication Interfaces

The communication interfaces allow the data transmission and reception between the FPGA-based systems and its peripherals or storage devices. For this review, we have divided these interfaces into two (parallel and serial interfaces).

4.1. Parallel

Parallel communication interfaces in FPGAs are used for high speed data acquisition, communication protocols and memory interfaces. As seen in Figure 4, the most used case are the image and video capture interfaces. First, the Charge-Coupled Device (CCD) is an image sensor used for different kind of applications (image [104], video [105], X-rays [106] and astronomical [107]). FPGAs' implementations has involved the CCD interface for high speed data acquisition [108–110], noise reduction [111,112], ultra-high resolution [113,114], among others. CMOS image Sensors interface are also widely implemented in FPGA for high frame rate processing [115,116], exposure control [117–119] and dynamic range [120,121].

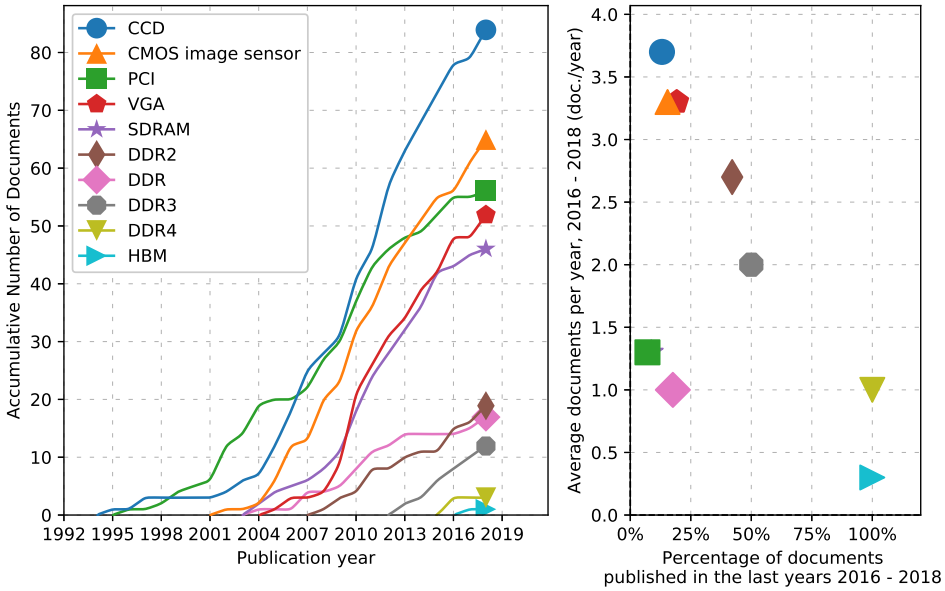

Figure 4. Parallel communication interfaces top implementations in FPGA research.

PCI (Peripheral Component Interconnect) is one of the older interfaces used for FPGA communications. According to Figure 4, publications related to this topic started in 1996 [122] and finished in 2016, due to this interface being replaced by the PCI Express. The VGA (Video Graphics Array) implementations include video and color scaling [123,124], video capturing [125] and real-time display [126,127].

The memory interfaces for FPGAs have grown in a similar time that these interfaces have emerged. For instance, in 2004, the FPGAs were used for monitoring the SDRAM (Single Data Rate Synchronous Dynamic Random-Access Memory) data retention under electromagnetic irradiation environments [128,129]. The DDR (Double Data Rate) implementation also started in 2004 with the design of a memory scheduler [130]. DDR2 implementations started in 2008 with the design of a high-speed camera system, capable of capturing 500 frames per second [131]. DDR3 documents started in 2013 with the design of a 3D volumetric display system, which uses the DDR3 memory as a high-capacity high-bandwidth video frame buffer [132]. DDR4 implementations started in

2016, with the study of thermal and energy-efficient in the memory interface design for 28 nm FPGAs [133,134]. Finally, in 2017, Gandhi et al. show the integration challenges for FPGA and HBM (High Bandwidth Memory) via an interposer interface [135]. These last two implementations (DDR4 and HBM) have 100% of PDLY for the last three years, which indicates that they are trending topics for the last three years.

4.2. Serial

Drive to higher bandwidth interfaces in computing devices has resulted in a major adoption of the serial communication interfaces [136]. That also has been reflected in FPGAs' research. Figure 5 shows a high increase in publication related to serial communication interfaces. Implementations for Ethernet physical layer in FPGAs are popular nowadays in next-generation Gigabit Ethernet implementations [137,138]. Also, precision delay measurement techniques have been developed to support the IEEE 1588 Precision Time Protocol [139–143]. Similarly, a security network processor was developed using FPGA for high-performance online security protocols processing [144,145].

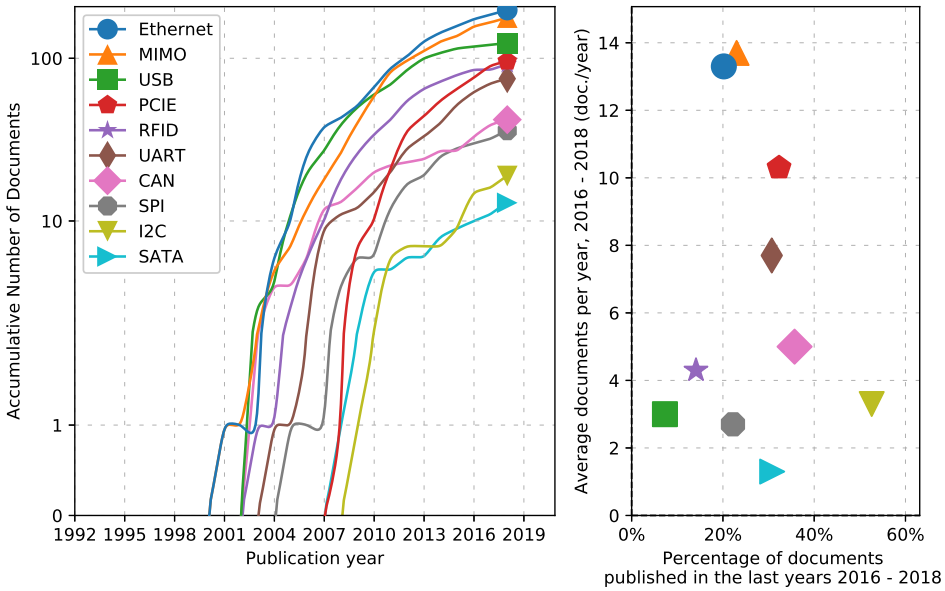

Figure 5. Serial communication interfaces top implementations in FPGA research.

The multiple-input and multiple-output (MIMO) is the communication method implemented in FPGAs' research with the highest ADY. FPGAs allows real-time MIMO-OFDM (MIMO Orthogonal frequency-division multiplexing) transceivers implementations for multiple streams [146–148]. Also, channel estimation for MIMO uses FPGAs for efficient hardware resource utilization [149] and fast prototyping algorithms [150,151]. The USB (Universal Serial Bus) interface has been widely used for FPGAs' boards to a host computer communications [152–156]. In the same way, some authors have built FPGA security systems for monitoring and detecting USB cable attacks [157] and also for building cryptography systems to add security to USB devices [158].

PCI Express (PCI-E) is nowadays the most used interface for high-performance communication between FPGAs and host-CPU (host-Central Processing Unit) [159,160], GPUs (Graphic Processing Units) [161,162] or other FPGAs [163,164]. On the other hand, other researchers have worked with FPGAs and RFID (Radio Frequency Identification) for security analysis and RFID new implementations [165–167], hardware UART (Universal Asynchronous Receiver/Transmitter) implementation and simulation [168–170], CAN (Controller Area Network) bus routers [171] and gateways [172]. SPI (Serial Peripheral Interface) and I2C (Inter-Integrated Circuit) communications are mostly used for FPGA to MEMS (Microelectromechanical systems) communications [173,174].

Finally, SATA (Serial Advanced Technology Attachment) interface has been implemented in FPGAs for high-speed data storage [175–177].

5. Networking

According to our dataset, the FPGAs have been used for networking applications since 1994. Figure 6 shows the top FPGA-based applications for networking. In Software Defined Radio (SDR), the components that have been traditionally implemented in hardware (such as mixers, filters and modulators) are instead implemented in software (computers or embedded systems) [178]. The SDN (Software-Defined Networking) implementations based on FPGA includes OFDM modulators [179–183], BPSK (Binary Phase Shift Keying) modulators [184,185], QPSK (Quadrature Phase Shift Keying) modulators [184,186], GNSS (Global Navigation Satellite System) and GPS (Global Positioning System) receivers [187–190], CDMA (Code-Division Multiple Access) [191] and QAM (Quadrature Amplitude Modulation) modulators [192,193].

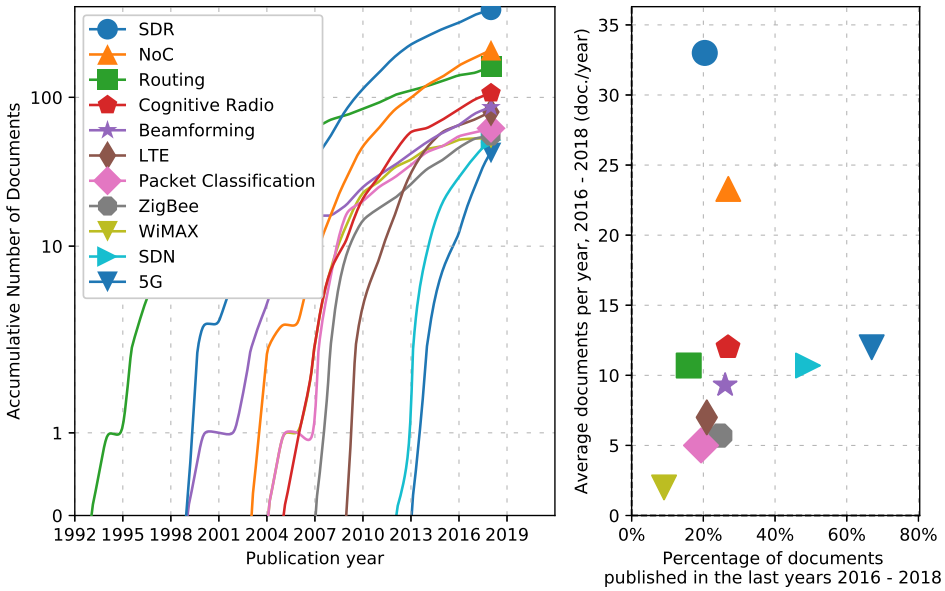

Figure 6. Networking top implementations in FPGA research.

Network on chip (NoC) is a paradigm which aims to solve the communication issues between the CPU units of the next generation of many core System on Chip (SoC). Some FPGA-based implementations to solve NoC problems include network switches typologies [194–199], buffer handling [200,201], router implementations [196,202–207] and NoC simulators [208–210].

Routing applications are the first that have been implemented in FPGAs for networking, starting in 1994 [211]. These includes packet processing [212,213], NetFPGA platform to prototyping networking devices (switches and routers) [214–216] and parallel routing [217–222]. Cognitive radio tries to solve the spectral congestion by using the best wireless channels in its vicinity to avoid user interference and congestion [223]. In this area, FPGAs have been using for spectrum sensing [224–237], reconfigurable antennas [238,239] and adaptive codec [240]. Beamforming is a signal processing technique for directional signal transmission or reception in sensor arrays [241]. This keyword is correlated for FPGAs applications to beamforming in radio communications systems and beamforming in ultrasound imaging. In this section, we are analyzing the first one. For radio communications systems, beamforming applications with FPGAs consist of band Infinite Impulse Response (IIR) beam filters [242,243] and beamforming Direction Of Arrival (DOA) estimation [244].

Long-Term Evolution (LTE) applications related with FPGAs started in 2010 [245,246] and these include the implementation of the Physical Downlink Shared Channel (PDSCH) [247,248], Physical Downlink Control Channel (PDCCH) [249,250], efficient implementation of a parallel-pipelined

configurable FFT/IFFT (Fast Fourier Transform / Inverse Fast Fourier Transform) processor [251–254]. FPGAs play a crucial role in networking packet classification, because, due to the scalable and parallel models than can be built inside these systems, efficient and high-speed packet classification systems have been designed [255–259]. These systems have been applied to firewalls [260,261] and OpenFlow capable switches [262]. ZigBee is a high-level communication protocol based on the IEEE 802.15.4 standard used in personal area networks such as home automation, smart farming and other low power and low bandwidth applications [263]. FPGA applications in this protocol includes more efficient ZigBee transceivers and MAC (Medium Access Control) protocol implementations [264–268] and data encryption in security improvement for ZigBee networks [269–271]. 5G (5th Generation) is the latest generation of cellular mobile communications that aims at the high data rate, improve the latency and the energy-saving [272]. WiMAX (Worldwide Interoperability for Microwave Access) is a wireless technology to provide last mile Internet broadband access [273] and it was a candidate for 4G communications, in competition with LTE. FPGA implementations for this technology includes OFDM transceiver [274,275], SDR [276–278] and Viterbi decoders [279–281]. Nevertheless, WiMAX lost the competition for 4G. As a result, we see it as the lowest ADY on this list. Software-Defined Networking (SDN) is a network management approach that enables programmatically efficient network configuration to improve network performance and monitoring [282]. For SDN we can find implementations in FPGA related to ultra low latency data center services [283], Software Defined Hardware Counters (SDHC) for dynamic network statics [284], high speed network (10Gbps) performance evaluation [285], packet arrival time measurement [286] and anomaly-based intrusion detection [287]. Similarly, as for SDR, in SDN we found several implementation based on NetFPGA platform [215,285,286,288–293]. FPGAs' applications for 5G have the highest PDLY (see Figure 6). These applications have helped to enable this new technology from 2014 with implementations like the antenna testbed for massive MIMO [294,295], transceiver modulator/demodulator enablers [296–299], time delay and latency estimation [300,301] and beam direction of arrival estimation [302]

6. Computer Security

Computer security or cybersecurity aims to protect confidentiality, integrity and availability of data and assets used in cyberspace [303]. Figure 7 shows the top FPGAs' applications for computer security with their number of documents and the PDLY. The first one is fault tolerance with near to 400 documents. This is a feature that enables a system to continue operating properly in the event of a failure [304] and it is widely used for space [305–310], automotive [311,312] and robot controllers applications [313,314]. NASA defines Single Event Upset (SEU) as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs". Then SEUs are random software errors of a transient nature in integrated circuits but are not generally non-destructive to hardware [315]. FPGAs have been used to built fault tolerance systems against the SEU [316–319]. Another security topic is fault injection, which involves inserting faults into a particular target at a determined time in the process and monitoring the results to determine its behavior in response to this generated fault [320]. Implementations of this kind in FPGAs help to efficiently analyze the performance of fault tolerance systems [320–324].

Side-channel attacks (SCA) refers to any attack based on information leaked for a cryptographic module that performs encryption or decryption of secret parameters via power dissipation, electromagnetic radiation or operating times as side-channel information [325]. FPGAs' research in this area covers FPGAs' vulnerabilities to SCA [326–328], security resistant designs against SCA [329–334] and hardware Trojan detection [335–337]. Physically Unclonable Function (PUF) is a noisy function that when queried with a challenge x, it generates a response y that depends on both x and the unique device-specific intrinsic physical properties of the object that contains the PUF [338]. In that way, the PUF is used as a digital fingerprint to identify a semiconductor device. FPGAs' applications for PUF

have the highest PDLY (62% of the documents published in the last three years) and these includes Ring Oscillator (RO) based physical unclonable function [339–343] and PUF strong evaluation [344–347].

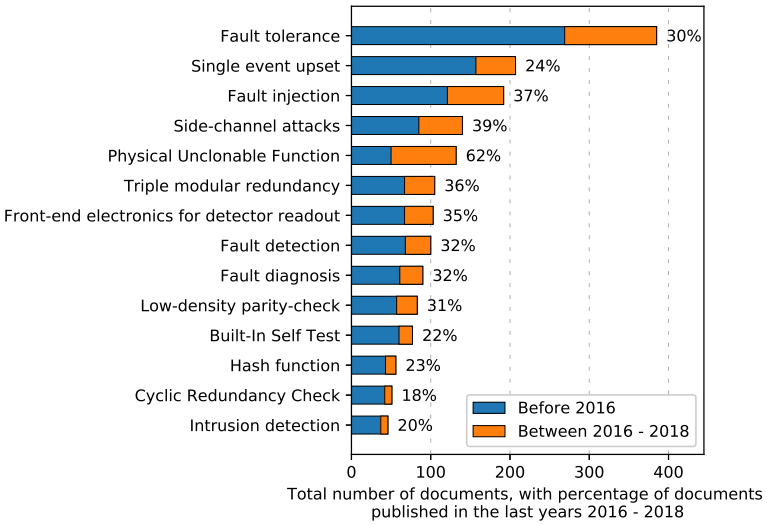

Figure 7. Security top applications in FPGA research.

Triple Modular Redundancy (TMR) is a fault-tolerance method, in which at least three systems perform a process and the result is processed by a majority voting system to produce a single output [348]. FPGAs are the perfect system to implement TMR due to its parallel design architecture. Applications of TMR in FPGAs covers novel design techniques of TMR [349–352] and TRM SRAM based systems [353–355], among others. FPGAs' systems can capture and process information at a very high speed compared with conventional systems. For this reason, FPGAs' systems have been widely used as front-end Electronics for detector readout calorimeters [356–358], neutrino detectors [359,360] and even particle tracking systems for the Large Hadron Collider (LHC) [361–365].

Other applications in our top list related to FPGAs are fault detection systems [366–371], fault diagnosis [372–377], Low-Density Parity-Check (LDPC) implementations for error correcting code in transmission [378–381], magnetic storage systems [382,383], Built-In Self Test (BIST) [344,384–388], hash function implementations [389–394], parallel and high speed Cyclic Redundancy Check (CRC) implementations [395–398] and efficient intrusion detection systems [399–404].

Cryptography Techniques

Cryptography techniques are created for securing digital information, transactions and distributed computations from third parties or the public that attempt to read private messages [405]. Figure 8 shows the top FPGAs' cryptography techniques implementations. Advanced Encryption Standard (AES), also know as Rijndael, is the most popular encryption technique that researches have implemented in FPGAs, with 510 documents. These implementations have been made to increase the encryption speed [406–410], generate small footprint and cheap designs [167,411,412], test the encryption against fault injections/attacks [413,414] and to improve the fault detection/tolerance systems [366,415,416]. Elliptic Curve Cryptography (ECC) is increasingly used in practice to instantiate public-key cryptography protocols, based on the algebraic structure of elliptic curves over finite fields [417]. In FPGAs' cryptography applications, it has the second ADY, with an average of 27 documents per year (2016 to 2018). FPGAs' implementations of these cryptography techniques includes efficient ECC processors [418–420], side-channel attack resistant implementations [329,331] and high speed implementations [421,422].

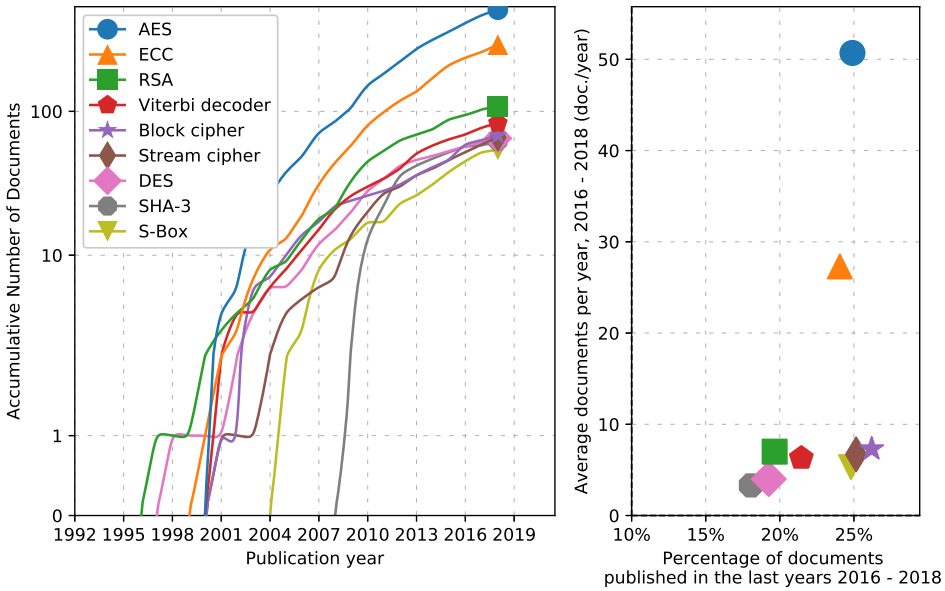

Figure 8. Cryptography top implementations in FPGA research.

RSA (Rivest–Shamir–Adleman) is one of the first public-key cryptography algorithm and it is based on the practical difficulty of the factorization of the product of two large prime numbers [423]. For RSA we found different FPGAs' implementations such as efficient or accelerated architectures [424–426], side-channel attacks resistant [427,428], tiny footprint [429] and Vedic mathematics based implementation [430]. Other cryptography techniques implemented in FPGAs are the Viterbi decoder with reconfigurable capabilities [279], high speed Viterbi decoders [431,432], steam cipher chaos-based techniques [433–436] and lightweight block cipher [437–439].

The Data Encryption Standard (DES) is an old encryption standard that is insecure for modern applications but has influenced in the advancement of modern cryptography [440]. FPGAs have been used to built cryptanalysis to crack a DES key [440–442], for DES pipelined implementations [443] and speed/power efficient implementations [444–446]. In 2008, the NIST (National Institute of Standards and Technology) started the competition for the new cryptographic Secure Hash Algorithm (SHA-3) [447]. Figure 8 shows that the implementations in FPGAs for SHA-3 started in 2009 with test and comparatives for SHA-3 candidates [448–453]. On October 2012, the Keccak cryptographic function was selected as the winner of the competition [454] and then implementations for the Keccak SHA-3 started in FPGAs [455], such as high throughput/performance [456–459], IoT focused applications [457] and compact implementations [460]. Finally, S-Box (Substitution-Box) is a substitution transformation used to obscure the relationship between the key and a encrypted text [461]. S-Box technique has been implemented in FPGAs for high throughput processing [462–464], memory efficient [465–468], low latency [469] and low power implementations [470–472].

7. Machine Learning

Machine learning is one of the top FPGA-based applications. Figure 9 shows the most implemented machine learning techniques for this architecture, where the neural network is the top one. These neural network implementations have been applied to pattern recognition [473–476], photovoltaic optimizations [25], modeling [477,478], controllers [479] and diagnostics [372]; power quality [480,481]; robotics control [482], robotics object detection and manipulation [483] and finally robotics object seeking [484]. Secondly, genetic algorithm applications include image processing [485–488], task scheduling [489–491], frequency estimation for digital relaying in power electrical systems [492–495] and mobile robots path planning [496–499].

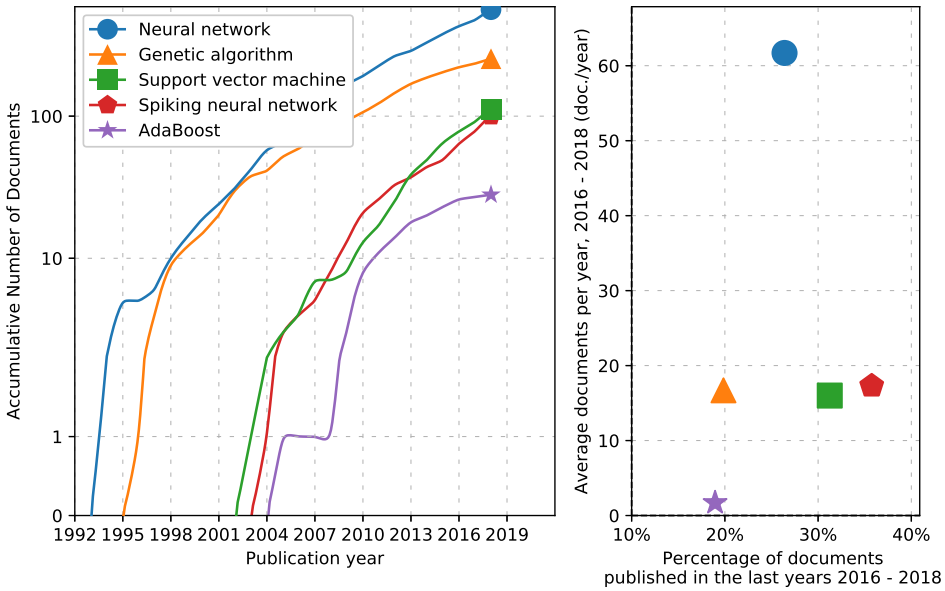

Figure 9. Machine learning top implementations in FPGA research.

Support Vector Machine (SVM) are widely used for classification and regression analysis [500]. The implementation of this technique in FPGAs is one of the newest, starting in 2002 (see Figure 9). The SVM has been used in FPGAs alongside the Histogram of Oriented Gradients (HOG) for object classifications in image processing [501–505]. Other SVM applications include facial expression recognition [506–508], network traffic classification [509], melanoma detection [510–512], arrhythmias detection [513,514], epilepsy detection [515] and stress detection [516].

The spiking Neural Netw. are a more biologically realistic model, with spiking neurons that transfer the information in the precise timing of spikes or a sequence of them [517]. For FPGAs, this machine learning technology has the highest PDLY (51% in the last three years). Some applications of this technique in FPGAs include character recognition [518,519], sound recognition [520,521] and other patterns/object recognition [522,523]. The AdaBoost technique (short for Adaptive Boosting) improves the performance of a weak learning and classifier algorithm into a strong one. This machine learning technique is the newest that has been implemented with FPGAs in our list (starting in 2005). It has been widely applied for image processing in face detection [524–528] and also for human detection [501,529].

8. Digital Signal Processing

Digital Signal Processing (DSP) is the performing of signal processing using digital techniques by a computing device [530]. Figure 10 shows the top DSP techniques implemented in FPGAs without covering digital filters, which are covered in the next sub section. Fast Fourier Transform (FFT) is the most implemented DSP technique in FPGAs, with near to 677 documents related to it. Here, we found CORDIC-based FFT [531–536], double-precision floating-point FFT [537], OFDM systems based in FFT [538–542], radix-2 FFT [543,544] and radix-4 FFT [533,545–547] implementations. The Discrete Wavelet Transform (DWT) is a wavelet transform by a certain orthonormal series generated by a discrete wavelet to capture both frequency and location information [548]. The DWT have been implemented in FPGAs for image and video compression [549–553], digital watermarking [554,555], EEG (Electroencephalography) signal processing [556–558] and general image processing [559–561].

Time-to-digital converters (TDC) are designed to measure a time interval and convert it into digital output [562]. FPGAs' implementations of TDCs offer high accuracy in time measurement. These technique has been used for Positron Emission Tomography (PET) [563–566], Light Detection And Ranging (LIDAR) [567,568] and high speed ADC (Analog-to-digital converter) [569,570]. Discrete Cosine Transform (DCT) implementations in FPGAs have been applied to MPEG-based

video encoders [571–573], JPEG encoders [574,575], for the Pierre Auger cosmic rays observatory front end detectors [576–579] and recently to image mosaicing systems [580]. Total Harmonic Distortion (THD) is a measure of the effective value of the harmonic components of a distorted waveform and it is commonly used for a quick measure of distortion [581]. THD implementations in FPGA have the highest PDLY in this category (43% of documents in the last three years) and these have been implemented in FPGAs for multilevel inverters [582–585], AC (Alternating Current) LED (Light-Emitting Diode) drivers [586–589].

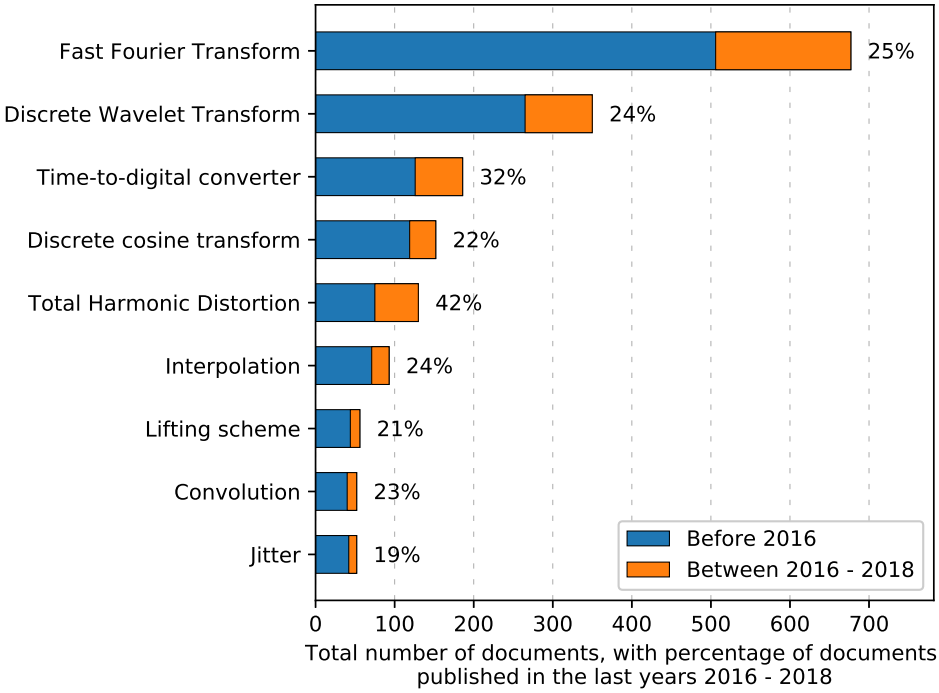

Figure 10. Digital signal processing top implementations in FPGA research.

Interpolation with FPGAs have been used for video scaling [590–592] and motion estimator for High Efficient Video Coding (HEVC) encoder [593–595]. Other digital signal processing implementations in FPGAs includes lifting scheme for efficient and modular DWT [596–599], efficient convolution techniques [600–602] and 3D convolution [603]. Finally, in our list is the jitter detection (deviation from true periodicity of a presumably periodic signal) using FPGAs [604], which includes jitter studies for 5G communications [301], Multi-Gigabit FPGA-Embedded Serial Transceivers [605], clock oscillators [606] and random number generators based on clocks signal jitter [607–609].

Digital Filters

A digital filter is a filter that operates on digital signals to perform mathematical operations to reduce or enhance certain aspects of that signal [610]. Figure 11 shows the top digital filters techniques implemented in FPGAs. Finite Impulse Response (FIR) filter is a filter where the output is computed as a weighted, finite term sum of past, present and perhaps future values of the filter input [611]. FPGAs have been used for efficient implementation of FIR filters using distributed arithmetic [612–615] and for high speed/low power implementations [616–618]. The Kalman filter uses a series of measurements observed over time, which include statistical noise and other inaccuracies, to produce an estimate of unknown variables [619]. FPGAs were used for high performance/efficiency implementation of Kalman filters [620–622], IMU (Inertial Measurement Unit) Sensors fusion [623–625] and real-time filtering [626–628].

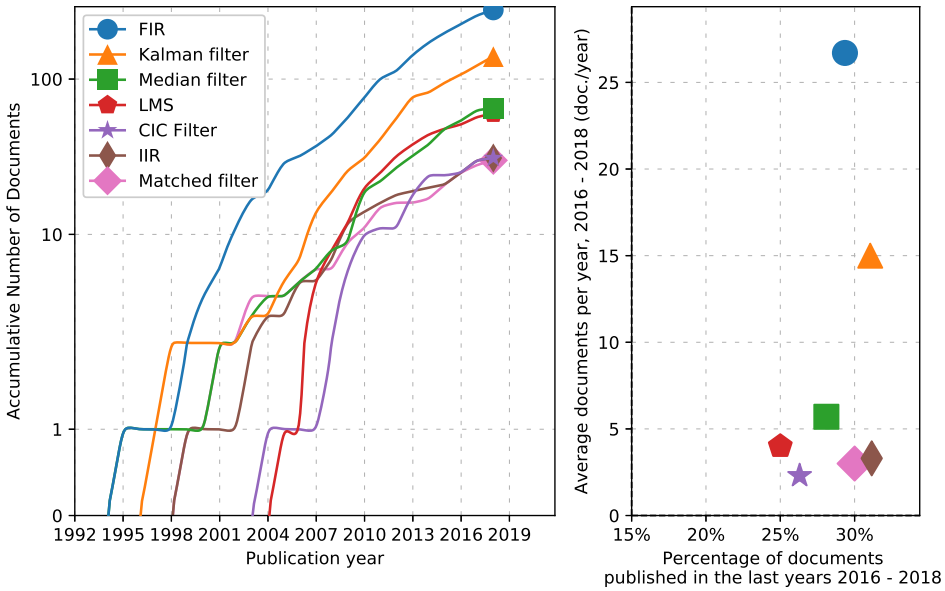

Figure 11. Digital filters top implementations in FPGA research.

Median filters implementation in FPGAs includes application for image processing [629–632], low power median filters [633,634] and high speed/real-time applications [635–637]. The Least Mean Squares (LMS) filter is an adaptive filter that finds the adequate filter coefficients to produce the least mean square error of the difference between the desired and the actual signal [638]. The LMS filters have been used in FPGAs for active noise cancellation in headphones [639], echo cancellation [640–642] and non invasive fetal ECG (Electrocardiogram) [643,644]. Other digital filters implementations in FPGAs include Cascaded integrator–comb (CIC) filter [645–649], Infinite Impulse Response (IIR) filters [650–653] and matched filter [654–658].

9. Image and Video Processing

Image and video processing techniques comprise the use of computer algorithms to perform video/image acquisition, compression, preprocessing, segmentation, representation, extraction, recognition and interpretation [659]. These techniques involve one of the most important applications in FPGAs. Figure 12 shows the top image and video processing techniques implemented in FPGAs, without including image and video/image compression standards that we include in the following subsection. First, stereo vision tries to infer the scene geometry from two or more images taken simultaneously from slightly different viewpoints [660]. This is the top image/video processing technique in FPGAs with 161 documents and includes real-time stereo vision implementations [661–664], Census transform [665,666], 3D reconstruction systems [667,668] and even the use of this technique with FPGAs for the Mars rovers navigation systems [669,670]. Face detection and recognition is the second topic in this list. Applications related to this topic in FPGAs include face detection with Haar classifiers [671–674], real-time/high speed face detection/recognition [675–680], AdaBoost based face detection [524,527,681] and Viola-Jones based face detection algorithm [682–684].

Edge detection aims to identify points in an image at which the brightens or other image characteristics changes sharply. FPGAs' implementations for edge detection cover implementations based in Sobel operator [685–689], Canny algorithm [690–692], applications for real time processing [693–697], image segmentation [698,699], DNA (Desoxyribonucleic Acid) microarray image processing [700,701] and object detection [702–704].

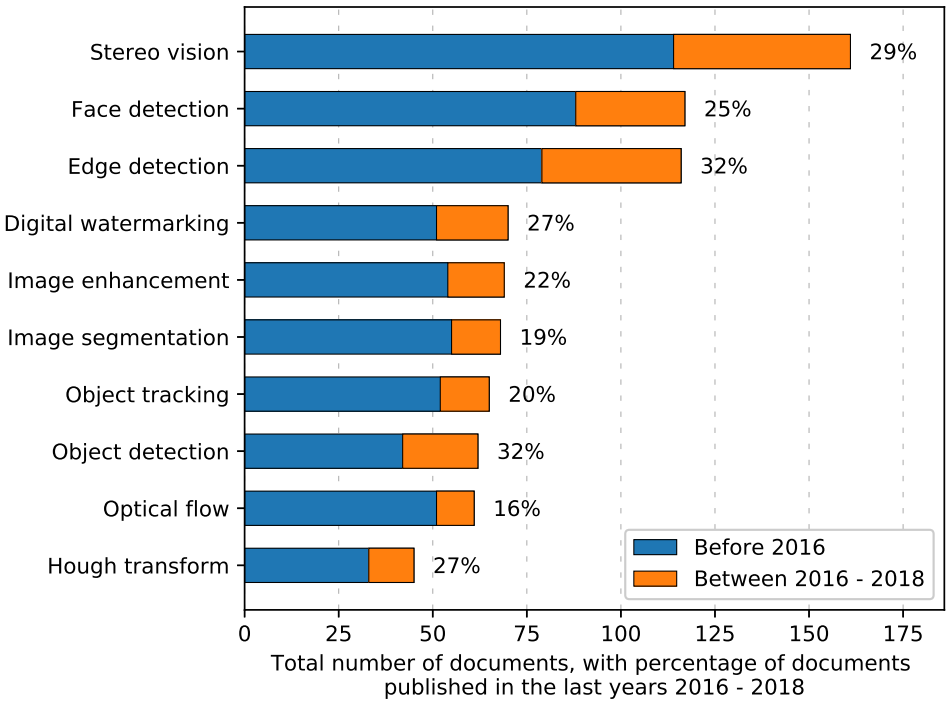

Figure 12. Image and video compressing processing top techniques implementations in FPGA research.

Digital watermarking is the act of hiding information in multimedia data, such as image, video or audio, for content protection or authentication [705]. FPGAs in digital watermarking have been used for real time watermarking detection in video [706,707], Discrete Cosine Transform (DCT) based digital image watermarking [708–710] and Discrete Wavelet Transform (DWT) based digital image/audio watermarking [555,711,712]. Image enhancement is used "to improve interpretability or perception of info available within the images, making it suitable for human vision, as well as to provide improved input to the other automated image processing techniques" [713]. FPGAs' implementations for this technique include histogram equalization [714–717], retinex image enhancement [718–720], Infrared Focal Plane Arrays (IRFPA) image enhancement [721,722] and telescopes' atmospheric turbulence mitigation [723, 724]. Other image processing applications that use FPGAs are image segmentation [725–729], object tracking [730–734], object detection [735–739] (real time object detection [740–742], moving objects detection [743–745], pedestrian detection [746–749] and background identification [750–752]), optical flow [753–757] and Hough transform [758–762].

Compression Standards

Images and videos need substantial storage space. A single uncompressed 12 megapixels image with 24-bit color depth requires 36 MB to be stored in PPM format (portable pixmap file format). A full HD video with 24-bit color depth and 60 fps requires 356 MB/s ($(24/8) \times 1920 \times 1080 \times 60 = 355.957$ MB/s) or 1.22 TB/h. If that were the case, a 3 Gbps Internet connection speed would be required to watch online full HD videos. For this reason, image and video codecs store the information with compression standards that reduce the required storage size significantly. FPGAs' implementations of these compression standards allow real-time coding of complex algorithms. To the present day H.264 is the most popular standard for video codding related to FPGAs' implementations (see Figure 13). The research of FPGAs' implementations for this codec started in 2003 [763] and some implementations are related to motion estimation [764–768], intra-prediction [767,769–772], quantization [773,774] and DCT (Discrete Cosine Transform) [775,776].

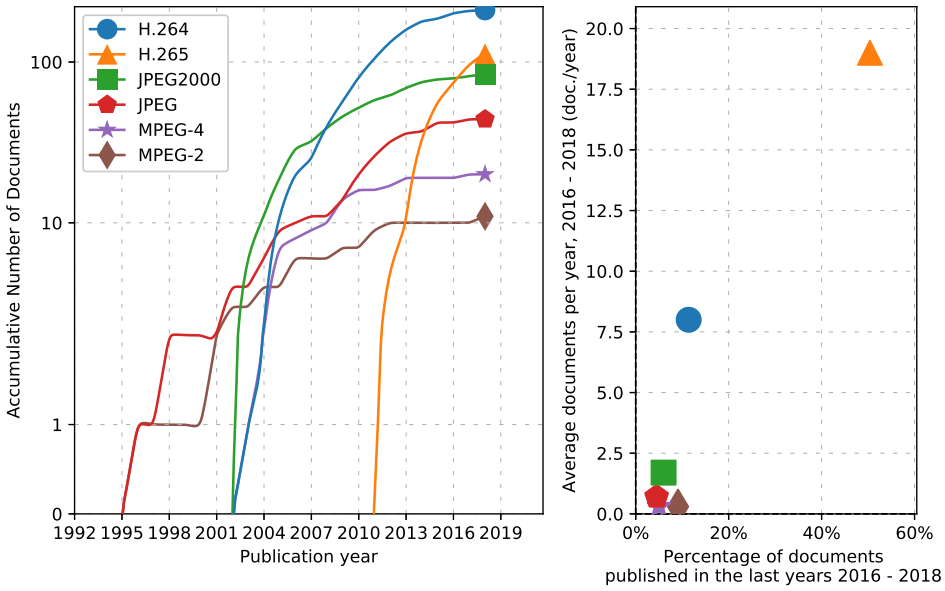

Figure 13. Image and video compressing codecs top implementations in FPGA research.

High-Efficiency Video Coding (HEVC) or H.265 is considered the successor of the H.264 video codec for higher resolution video applications [777,778]. This new codec is doubling the compression ration of its predecessor [779–781]. FPGA implementations and tests of this codec started in 2012 and today has the highest ADY and PDLY (50% of the documents published in the last three years, see Figure 13). One of the most critical challenges for H.265 is the efficient implementation of CABAC (Context-based Adaptive Binary Arithmetic Coding) that the research community considered as a well-known throughput bottleneck due to its strong data dependencies [782–784].

MPEG-2 (Moving Picture Experts Group) implementations in FPGAs started in 1996 [785] and MPEG-4 in 2003 [786]. The MPEG-2's ADY is close to zero, which indicates that there have been almost no publications in this topic from 2016. Similarly, MPEG-4 has a low ADY of 0.3 documents/year, with research documents focused on the AAC (Advanced Audio Coding) implementation [787–789].

On the other hand, image compressing standards implementation in FPGAs started with JPEG (Joint Photographic Experts Group) in 1996 [790]. JPEG2000 implementations started in 2003 [791–793] and surpassed JPEG the same year. JPEG2000 standard uses a wavelet-based method to provide better rate-distortion performance than the original JPEG [794]. The embedded wavelet coding algorithm know as EBCOT (Embedded Block Coding with Optimized Truncation of bit-stream), used for JPEG2000 standard, has been widely implemented in FPGAs for parallel optimization [795–800].

10. Big Data

Dumbill defines big data as the "data that exceeds the processing capacity of conventional database systems" [801]. Big data systems are focused on analyzing efficiently this kind of data with not conventional systems, which are boosted by FPGA-based applications. Figure 14 shows the leading big data techniques evolution graph related to FPGAs' research.

MapReduce is a programming model for processing and generating large big data sets with a parallel or distributed algorithms [802]. FPGAs have been used to accelerate MapReduce algorithms by different frameworks such as FPMR (FPGA MapReduce) [803], MrHeter for heterogeneous data centers [804] and Melia based on OpenCL [805]. Other accelerators for MapReduce include scalable data center FPGA-based accelerators (HLSMapReduceFlow [806]), coarse-grained reconfigurable architecture acceleration [807], energy-efficient accelerators [808,809] and others [810,811]. Hadoop (also known as Apache Hadoop) is an open-source framework for distributed storage and distributed processing on huge data sets into computer clusters [812]. For Hadoop, FPGAs' applications include energy-efficient acceleration of big data analytics [809], FPGA-accelerated Hadoop cluster for deep

learning computations [813], process streaming data from SSDs (Solid State Drives) using FPGAs [814] and low-power Hadoop cluster [815].

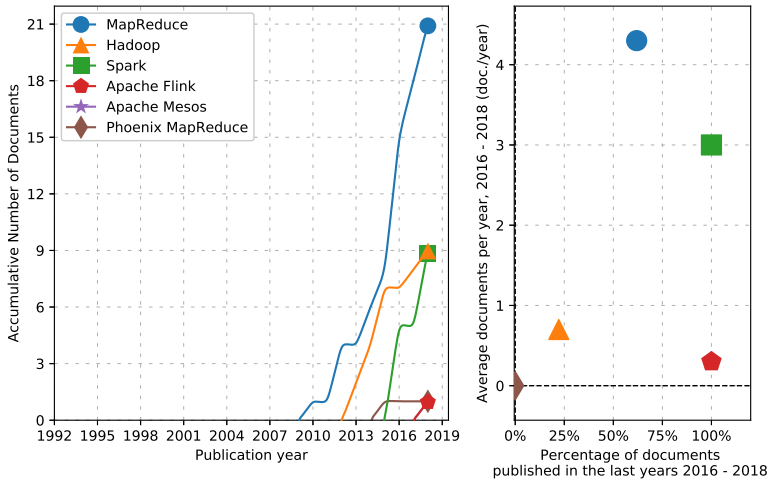

Figure 14. Big data top implementations in FPGA research.

Spark (also known as Apache Spark) is an open-source distributed general-purpose cluster computing system framework from Apache that supports in-memory computing, which enables it to process data faster compared to disk-based engines like Hadoop [816]. FPGAs' applications related to Spark have the highest relative growth, with 100% of the publications in the last three years. For Spark, FPGAs have been used to accelerate the Spark process [31,32,817] and deep convolutional Neural Netw. for the Spark environment [818]. Other big data frameworks accelerated by FPGAs are Apache Flink in heterogeneous hardware [819], Apache Mesos for cluster management for the HetSpark framework [820] and Phoenix MapReduce in multi-core FPGA's systems [821].

11. Computer Algorithms

FPGAs have a high capability to accelerate computer algorithms due to the parallel decomposition characteristics of some of them. This section shows the computer algorithms that are not enclosed in the previous sections. Figure 15 shows the top 10 algorithms implemented in FPGAs. CORDIC (for COordinate Rotation DIgital Computer) algorithm makes it possible to multiply and divide numbers by only shifting and adding steps. Also, it performs rotations to compute sine, cosine and arctangent functions [822]. The CORDIC algorithms implementations in FPGAs have been used for FFT processing [531,532,823], OFDM [824,825] and DCT transform [826,827]. Hardware floating point implementations in FPGAs are common for high performance FFT applications [828–831], floating point based Neural Netw. [832,833] and double precision floating point modules [834–837]. On the other hand, in Distributed Arithmetic (DA), multiplication is performed using precomputed lookup tables instead of the logic, reducing the cycles required to compute a final result [838]. FPGAs' implementations of DA have been used for FIR filters [612,613,839–841], discrete cosine transform [842–845] and wavelet transform [560,846–848]. Another FPGAs' computer algorithm implemented in FPGAs is the Smith-Waterman algorithm [849–852] and its implementation for DNA sequence analysis [853,854].

String matching algorithms tries to find the position where patterns are found within a larger string or text [855]. For FPGAs we found string matching implementations for network intrussion detection [856–858], deep packet inspection [859] and string matching algorithms based in bloom filter [860,861]. Fixed-point arithmetic algorithms have been used in FPGA for accuracy-guaranteed bit-width optimization [862,863], Jacobi SVD (Singular Value Decomposition) [864], Lanczos tridiagonalization [865,866] and deep belief networks [867,868]. Vedic mathematics is a system based on 16 sutras or aphorisms used for mathematical mental calculation operations [869].

Vedic mathematics algorithms have been implemented in FPGAs for faster [870–873] and energy efficient [874–876] multiplication operations. Other algorithms implemented in FPGAs are the trigger algorithms [877–880], trigger algorithms for the ATLAS experiment [881–884] and Montgomery algorithm for cryptography applications [885–888].

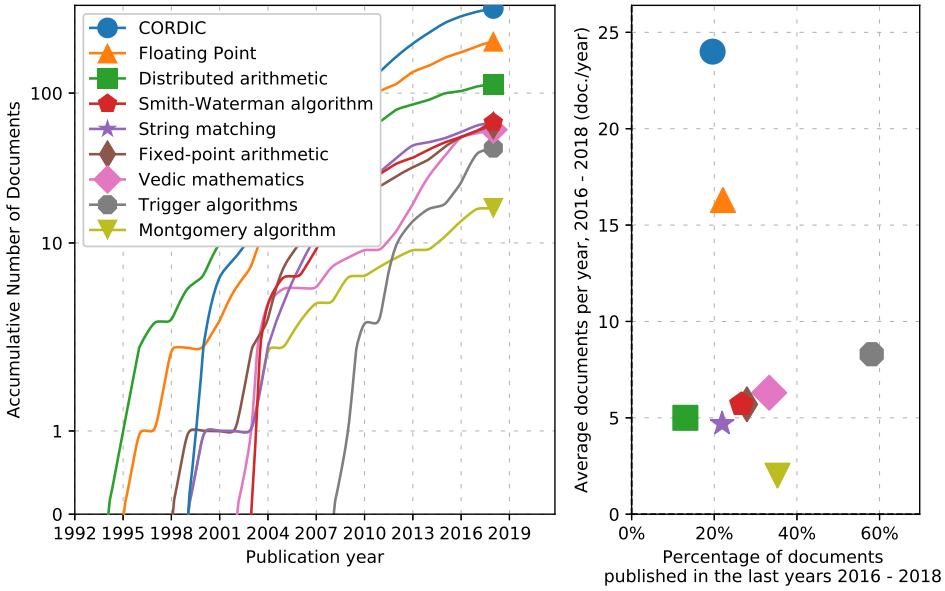

Figure 15. Top algorithms implementations in FPGA research.

12. Other Implementations

Figure 16 shows other top implementation techniques in FPGAs' research. Pulse Width Modulation (PWM) technique is one of the most used strategies for controlling the AC output of power electronic converter by varying the duty cycle of a converter switches [889]. FPGAs' implementations for PWM includes application for inverters [890–893], digital control for power converters [21,894–897] and total harmonic distortion reduction [898–901]. A Finite-State Machine (FSM) is a representation of an abstract machine that can be or can change into a state that represents a possible situation. This change from one to another state is called transition and occurs in response to an external input [902]. Implementations of FSMs in FPGAs include low power FSMs [903,904] and engineering education [905,906].

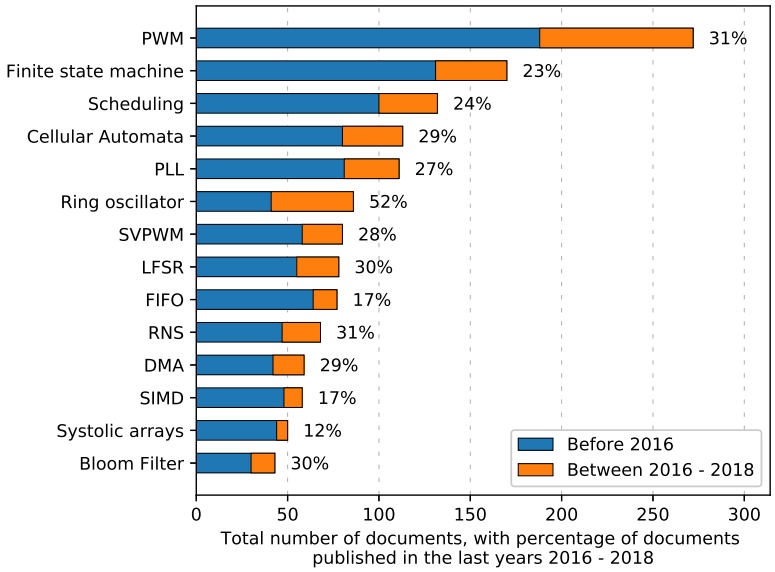

Figure 16. Other top implementations techniques in FPGA research.

In computing, "scheduling is the method by which work is assigned to resources that complete the work" [907]. Scheduling in FPGAs has been used for reconfigurable computing [908–910], real-time applications [911–913] and heterogeneous embedded systems [909,914,915]. According to Wolfarm, cellular automata consist of many identical simple components, that together are capable of complex behavior [916]. Alongside FPGAs, cellular automata has been used for cryptography [917–923], random number generation [924–927], systems modeling [928–937] and simulation [938–940]. Phase-Locked Loop (PLL) "synchronizes the frequency of the output signal generated by an oscillator with the frequency of a reference signal by means of the phase difference of the two signals" [941]. In FPGAs the PLLs have been used for motor speed control [942–944], demodulator synchronization [945–947] and jitter detection [607,948–952].

Ring oscillator in this list has the highest PDLY, with 52% of the documents published in the last three years. A ring oscillator is a cascaded combination of delay stages, connected in a close loop chain to generate an oscillating output [953]. FPGAs' implementations of ring oscillators include physical unclonable functions [339,342,954–957], time to digital converters [958–962] and random number generators [609,963–972]. Other implementations techniques in FPGAs covered in this top are SVPWM (Space Vector Pulse Width Modulation) [973–979], LFSR (Linear-Feedback Shift Register) [980–985], FIFO (First-In First-Out) [986–994], RNS (Residue Number System) [995–1001], DMA (Direct Memory Access) [1002–1005], SIMD (Single Instruction Multiple Data Stream) [1006–1009], systolic arrays [1010–1014] and bloom filter [860,1015–1020].

13. Other Applications

In this section, we present other FPGAs' applications not covered previously. Figure 17 shows the top other applications.

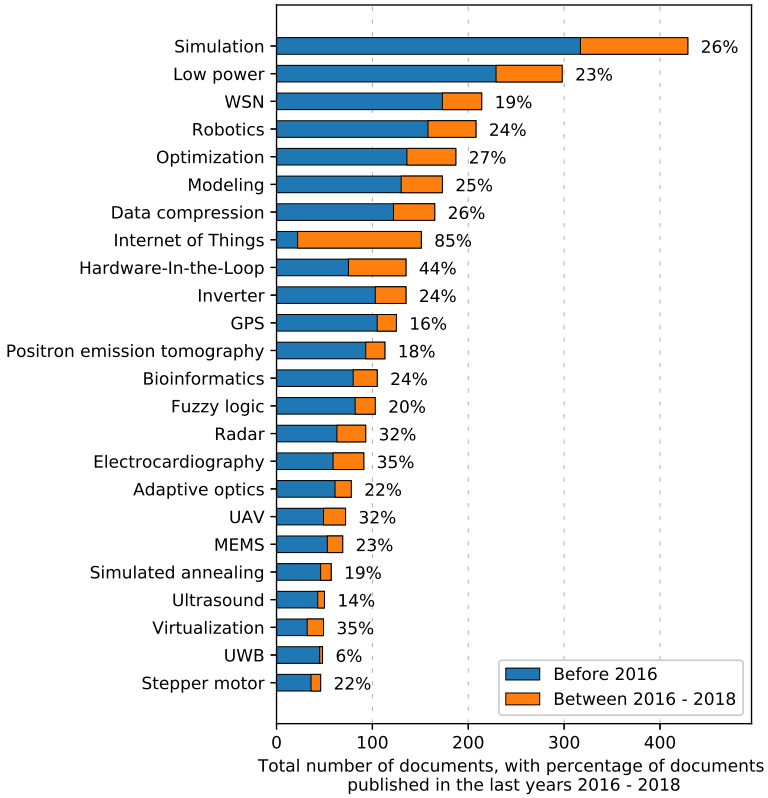

Figure 17. Other top applications in FPGA research.

Simulation is the top of this list and it refers to an approximate imitation of the operation of a process or system [1021]. In this area, we found FPGAs' usage for the simulation of different systems, such as the described following:

- Power Electronics [1022–1056]
- Multiprocessors/multicore architectures [19,1057–1061]
- Neural biological systems [1062–1065]
- Single even upsets (SEU) [1058,1066–1069]
- Photovoltaic systems [477,1070–1078]
- Read-out detectors [1079–1081]
- Electrical machines [1082–1089]
- Distribution grids [1090–1095]
- Vehicles [1096–1101]
- BPSK and QPSK modulators [1102,1103]
- Microprocessors cache [1104,1105]
- Fuel cells [1106,1107]
- Synthetic Aperture Radar (SAR) echo simulation [1108,1109]
- Wind farms, turbines [1110,1111]
- RFID tags [1112,1113]
- Biochemical reaction [1114]
- MEMS (Microelectromechanical Systems) [1115]
- Nanoscale devices [1116]
- Quantum computers [1117]
- HPC (High-Performance Computing) power consumption [1118]

Low power applications are the second in this other applications list, which include low power applications for image processing [1119–1124], H.264 encoding [769,771,1125–1129], finite state machine [904,1130], memory design [1131–1133] and AES encryption [1134–1137]. The WSN (Wireless Sensor Networks) comprises wireless Sensors that have a sensing comportment, on-board processing, communication and storage capabilities to cooperatively monitor a large physical environments [1138]. FPGAs have been used in WSN for elliptic curve cryptography implementations in sensor nodes [1139–1144], energy efficient sensor nodes [1145–1147], ZigBee MAC layer functions realization [268,1148] and ZigBee physical layer blocks simulation [1149]. Next, robotics applications (including mobile robots) in FPGAs involves:

- Localization [1150–1156]
- Trajectory/path planing [498,1157–1163]
- Visual servoing [483,1164–1169]
- Navigation [11,1153,1170–1173]
- Stereo vision [1173–1177]
- Object/person follower/tracking [1168,1178–1180]
- Ultrasonic Sensors [1181–1185]
- Robot Operating System (ROS) [1153,1186–1189]
- Educational [1190–1192]
- Motion control [1193–1195]
- Vector rotation [1183,1196,1197]
- Obstacle avoidance [1198–1200]
- Arm robot joints control [1201,1202]
- Mapping [1203]
- Collaborative robotics [1204]
- Spatial cognition [1205]
- Velocity estimation [1206]

Optimization applications in FPGAs enclose power optimization [1207–1209], CRC (Cyclic Redundancy Check) look-up table [1210], pipelines [1211,1212], Particle Swarm Optimization (PSO) [1213–1215], SM3 hash algorithm [1216], FIFO stack [1217], matrix multiplication [1218], torque ripple [1219], memory usage [1220], banking model [1221] and thermoelectric coolers [1222]. Modeling is the use of mathematical models as an idealization of a real-world phenomenon, for predicting the value of a variable at some time in the future [1223]. Similarly to simulation, FPGAs have been used in several modeling applications:

- Control systems [1224–1228]
- Power Electronics [1028,1086,1229–1232]
- Network on chip [1233,1234]
- Thermomechanical systems [1235,1236]
- Employees behavior and interactions in workplace [928]
- Computer networks [1237,1238]
- Arousal content [1239]
- FIFO stack [1217]
- HPC power consumption [1118]
- Meteorological systems [1240]
- UAV (Unmanned Aerial Vehicle), vehicles and mobile robots [1241,1242]
- Renewable energy systems [1225,1243,1244]
- RF (Radio Frequency) power amplifier [1245]
- Urban traffic [937]

Data compression is a reduction in the number of bits needed to represent the data [1246]. In FPGAs data compression has been implemented in the LZ77 algorithm [1247–1250], Huffman coding [1251–1253], LZW (Lempel–Ziv–Welch) algorithm [1248,1254–1257] and hardware accelerator compressing techniques [1247,1249,1258–1261]. Internet of Things (IoT) connects billions of devices to the Internet, devices that combine sensing, computation and communication techniques to deliver remote data collection and system control [1262]. IoT in this list is the application with the highest PDLY, with 85% of the documents published in the last three years. For IoT applications, FPGAs have been used in improving devices security [1263–1265], data encryption [460,1144,1266–1268], edge computing [1269–1271], FPGA-based gateways [1272,1273] and fog computing platforms [1274,1275].

Finally other FPGAs applications in this list includes Hardware-In-the-Loop (HIL) [34,1115,1276–1282], GPS (Global Positioning System) [1283–1298], Positron Emission Tomography (PET) [1299–1324], bioinformatics [1325–1342], fuzzy logic [1343–1353], radar [658,1354–1363], Electrocardiography [1364–1381], adaptive optics [1382–1394], Unmanned aerial vehicles [496,1395–1402], MEMS [174,1403–1411], simulated annealing [1412–1420], ultrasound [1421–1432], virtualization [1433–1438], UWB (Ultra-wideband) [1156,1439–1444] and stepper motor applications [1445–1462].

14. Applications Mapping

In this section, we describe the co-occurrence mapping for the different FPGAs' applications. For this purpose, we used the pre-processed output dataset generated by ScientoPy (which includes the merged datasets from WoS and Scopus in the Scopus data format) as an input to generate a network map in VOSviewer [1463]. In VOSviewer, we created an author keywords co-occurrence map, with a thesaurus file that merges the different variants of the applications names and filters the first 100 author's keywords that are not related to FPGA-based applications or implementations. Finally, we selected the first merged 35 author's keywords based on the total link strength values to generate the network map (see Figure 18). In this figure, we find five clusters described as follows. The yellow cluster indicates applications related to signal processing. The purple cluster is related to the applications that are related to low power implementations. Then, the green cluster contains applications related to security implementations. Next, the blue cluster shows high-performance and high-reliability systems. Finally, the red cluster points out real-time applications.

For the signal processing cluster (yellow color) we find relations that indicates for intance that MIMO is supported by OFDM [146,148,1464–1466] and OFDM is supported by FFT implementations [538,540,1467,1468]. The FFT implementations are supported by CORDIC [531–534] and also are designed as low power implementations [532,1469]. For the security cluster (green color), we found that AES has an strong relationship with security, encryption, cryptography and also with low power implementations [470,1134]. Similarly, we found that FPGAs' implementations have helped to add security to WSN nodes [1139–1141] and low power processing capabilities [1470–1472].

In the red cluster, we find FPGAs' applications focused in real-time implementations, such as data acquisition [565,1473–1475], simulations [1022,1024,1082,1476], Neural Netw. [1477–1479] and image processing [1480–1487]. Finally, the blue cluster shows that the fault tolerance and high reliability systems are based in fault injection impelmentations [1488,1489] and single event upset tolerance mechanisms [1490–1492]. In addition, other relevant relations are shown in colored lines, like digital control with PWM [1493,1494], simulation with modeling [1057,1118,1495] and performance with algorithms [1496–1498].

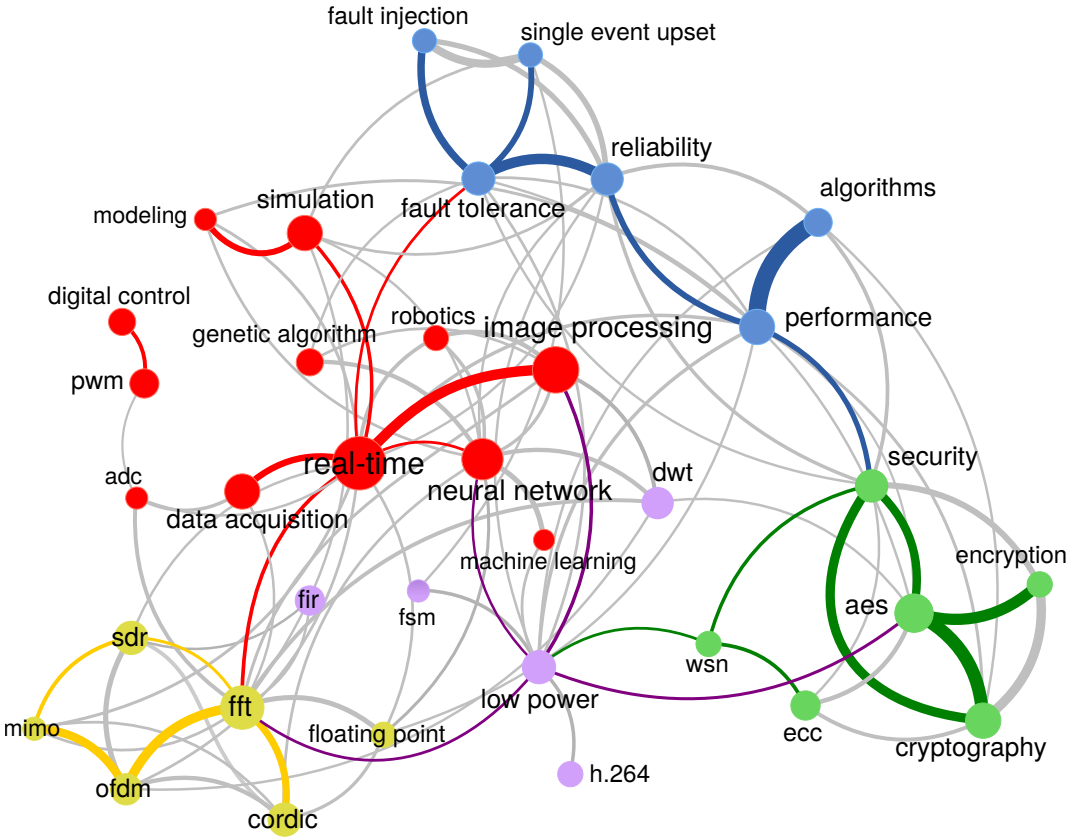

Figure 18. Co-occurrence network mapping of author keywords related to FPGAs' applications. Colors represent groups of applications that are relatively strongly linked to each other. The size of the node signifies the number of documents related and the width of the lines represent the strength of the relationship between two nodes.

15. Discussion

FPGAs have a wide range of applications, from real-time data processing to neural network implementations. In this review we divided these applications into eleven categories and in each category we presented the applications with most documents related to them, totaling 150 applications described in this review. For digital control we found that the most important control techniques are implemented in FPGAs, like fuzzy control [1499–1502], PID [69,1503,1504], model predictive control [73,76,1505], adaptive control [80,81,1506], sensorless control [1507–1509] and

distributed control [96,99,101]. These digital control techniques were implemented in FPGAs due the high speed response that a hardware digital control FPGA-based implementation can achieve and its reconfiguration capability, allowing control application to high speed system such as induction motors [1507,1510–1512], torque control [75,1513,1514], Brushless DC (Direct Current) motors [1515–1517], current control [1518,1519], among others [65,1520–1523].

The communications interfaces implemented for or with FPGAs have developed at the same rate that these interfaces have grown for other technologies, like computer or mobile interfaces. The implementations of these communication interfaces in FPGAs aims to high speed/real-time data capturing systems [565,1524–1531], security network processors [144,145], image capturing [108,113,1532–1534] and latest generation memory controller (DDR4 [133,134], HBM [135]). For networking, we found in this study that the FPGAs were used for the initial prototype and implementations of the new generation network standard like LTE [245,247,1535] and recently 5G [295,301,1536,1537]. Also, the FPGAs have been used for high-performance packet classification [257,258,1538–1540], Software Defined Radio (SDR) [186,1541,1542] and Network (SDN) [288,1543,1544], cognitive radio [224,225,238], Network on Chip (NoC) [1545–1547] and other network standards such as ZigBee [1548–1550] and WiMAX [279,1551,1552].

Computer security was one of the largest topic covered in this paper. FPGAs help to ensure the security of different systems with fault tolerance mechanism [14,1553,1554], single event upset recovery/mitigation [1555,1556] and emulation [321,1488], side channel attacks protection [330–332,1557,1558] and detection [1559–1561], physical unclonable function implementations [339,1562,1563], triple modular redundancy [1564–1566] and intrusion detection [399,1567,1568]. The applications and systems protected by these security techniques in FPGAs includes military [326,1569], space [308,1492,1570,1571] and medical [314,1572,1573] systems. Similarly, FPGAs have had an important role in the diverse cryptography techniques implementations. Different techniques like AES, ECC, RSA, SHA and others have been implemented in FPGAs for high throughput encoding/decoding [407,1574–1576], reconfigurable cryptographic processors [1577–1579] and low power consumption implementations [470,472,1580,1581].

Machine learning techniques implementations in FPGAs include in this paper neural networks, genetic algorithms, support vector machine, spiking neural network and AdaBoost. These have been implemented for image processing [527,1582,1583], pattern recognition [476,1584], real-time processing [671,1477,1585], melanoma cancer detection [510,511,1586,1587], speech recognition [1587,1588] and so forth. Digital signal processing techniques implementations in FPGAs covers FFT [537,1589–1593], DWT [597,1594–1597], time-to-digital converters [1598–1602], DCT [580,1603–1605] and digital filters like FIR filter [56,612,1606–1608], Kalman filter [620,1609–1611], median filter [1612,1613], LMS [1614–1616] and others.

For image and video processing, FPGAs have boosted different applications allowing real-time processing for stereo vision systems [661,667,1617–1619], face detection/recognition [675,677,679], object tracking [732,1620,1621] and digital watermarking for intellectual property protection [706,1622,1623]. These kind of applications have been used for different systems such as the Mars rovers computer vision [669,670], autonomous vehicles vision [1624–1629], atmospheric turbulence mitigation for telescope pictures reconstruction [723,724], among others. In addition, we found image and video compression standards implemented in FPGAs, from JPEG [1630], to most recent video compression standard H.265 [593]. The implementation in FPGAs of the different blocks that integrate the compression standards or codecs (intra prediction [1631–1633], Context-adaptive binary arithmetic coding (CABAC) [783,1634], DCT [775,1635], Context-adaptive variable-length coding (CAVLC) [1636–1638], etc.) allowed real-time [1639–1641] and low power [1125,1127,1129,1642] encoding. Similarly, big data processes have been accelerated with FPGAs [29], using Apache Hadoop [813,1643] and Apache Spark [31,32,1644].

Other computer algorithms implemented in FPGAs described in this review includes CORDIC [1645–1647], floating point [831,1648,1649], distributed arithmetic [1650,1651] and so on. Similarly, other implementations techniques for FPGAs found here were PWM [890,1652,1653], finite

state machines [1654–1656], scheduling [1657–1660], cellular automata [924,932], PLLs [950,1661,1662], ring oscillators [339,962,1663], and so forth. Finally, we summarized other FPGAs' applications which include simulation [1028,1040,1048,1057], low power consumption [16,1664,1665], WSNs [42,1666,1667], robotics [1150,1173,1668,1669], optimization [1208,1209,1670], modeling [937,1028,1671], Internet of things [1265,1266,1672], data compression [1673–1675], among others.

As noted above, FPGAs cover a vast range of applications in modern computing systems. These results summarize the top applications based on FPGAs, including evolution, trendings and co-relations. In this way, new evolving applications are shown here the trends of future technologies such as cryptographic standards (SHA-3), video compression algorithms (H.265) and even new generation networks like 5G. Similarly, another type of applications could inspire the developers in different and more efficient ways to solve actual problems, such as cancer detection systems, indoor location using the time of arrival or more efficient big data processing techniques.

This paper shows extensive background information on FPGA-based applications to researchers, graduate students, stakeholders, industry, journals and funding agencies. The overview of the FPGA-based accelerated applications mentioned here allows the researchers and industry to improve the efficiency of actually implemented systems. Also, the accelerated algorithms and techniques implementations allow the adoption of FPGAs for the acceleration of new kinds of applications. Finally, this work was limited to scientific publications in the two central databases (Scopus and WoS). Future research could examine these applications related to commercial and industrial ones, analyzing and comparing these applications trends with other sources like Google Analytics and others.

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