Supplementary Materials

Improved Pulse-Controlled Conductance Adjustment in Trilayer Resistors by Suppressing Current Overshoot

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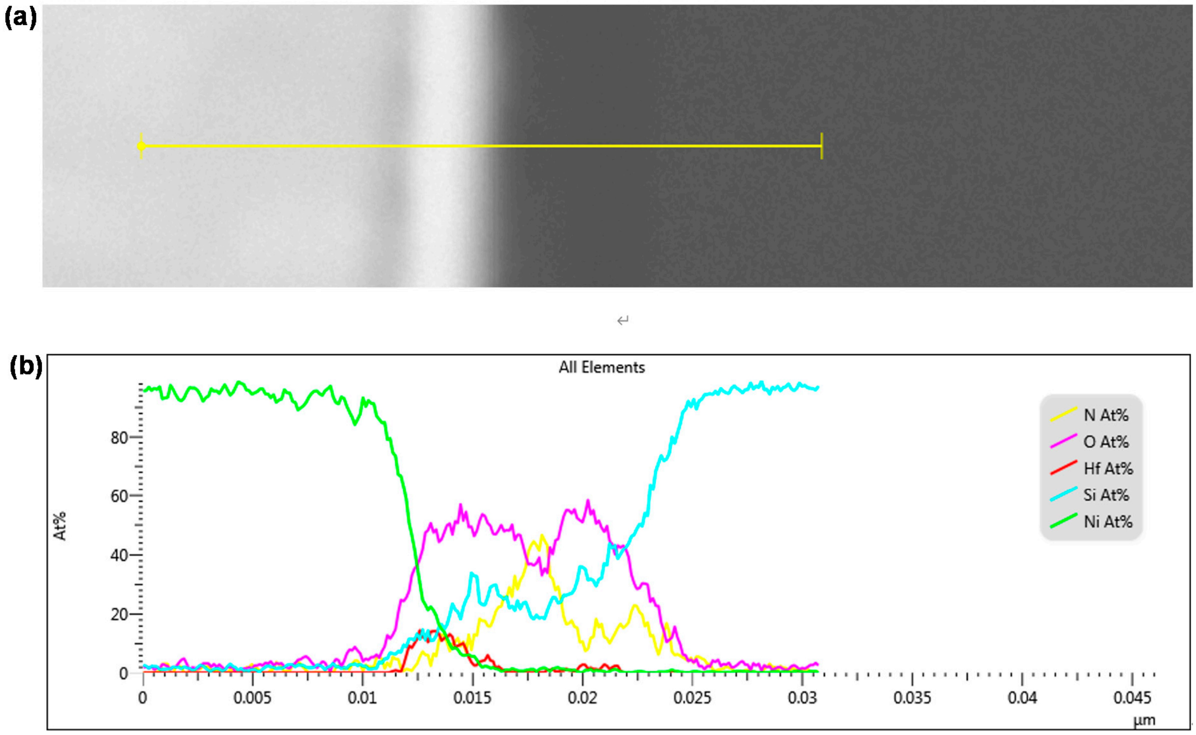


Figure S1. (**a**) STEM image and (**b**) EDS line scan of $Ni/HfO_2/Si_3N_4/SiO_2/Si$ device.

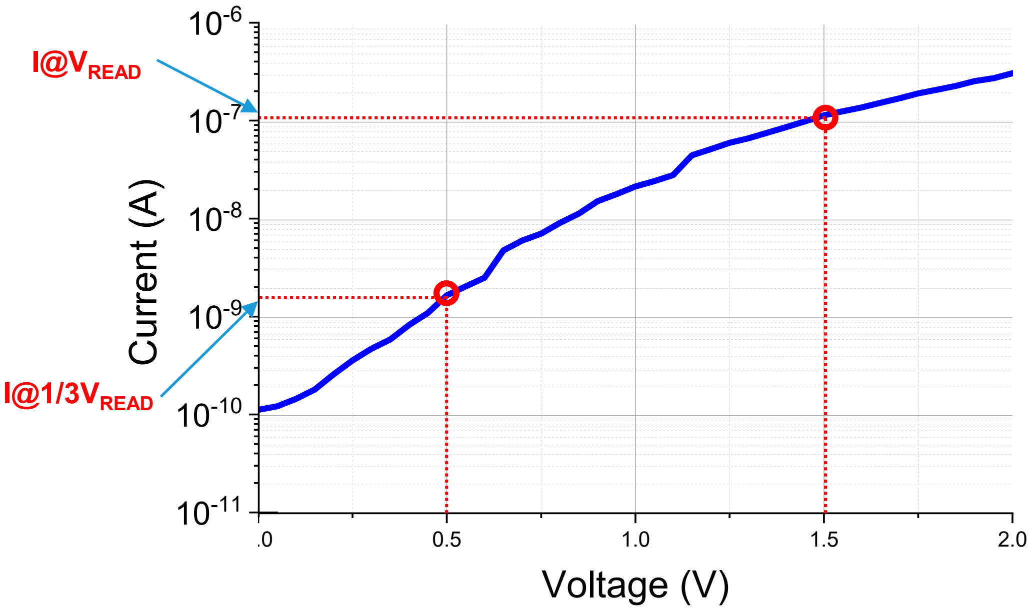
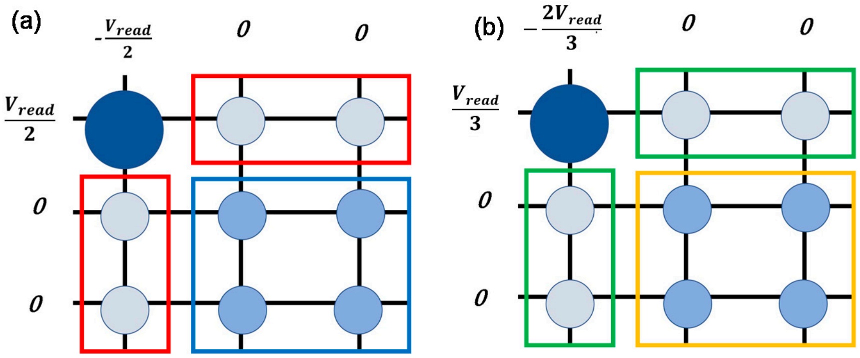


Figure S2. Definition of nonlinearity of I–V in the LRS.



½ scheme

$$\text{Read margin} = \left(\frac{R_{pu}}{\left(R_{LRS}(V_{cell})||\left(\frac{2R_{LRS}(\frac{V_{cell}}{2})}{N-1}+\frac{R_{LRS}(Vmi_{n})}{(N-1)^2}\right)\right)+Rpu} - \frac{R_{pu}}{\left(R_{HRS}(V_{cell})||\left(\frac{2RLR_{S}(\frac{V_{cell}}{2})}{N-1}+\frac{R_{LRS}(Vmi_{n})}{(N-1)^2}\right)\right)+Rpu}\right) \times 100\ (\%)$$

1/3 scheme

$$\text{Read margin} = \left(\frac{R_{pu}}{\left(R_{LRS}(V_{cell})||\left(\frac{R_{LRS}(\frac{V_{cell}}{3})}{N-1}+\frac{R_{LRS}(\frac{2V_{cell}}{3})}{N-1}+\frac{R_{LRS}(Vmi_{n})}{(N-1)^2}\right)\right)+Rpu} - \frac{R_{pu}}{\left(R_{HRS}(V_{cell})||\left(\frac{R_{LRS}(\frac{V_{cell}}{3})}{N-1}+\frac{R_{LRS}(\frac{2V_{cell}}{3})}{N-1}+\frac{R_{LRS}(Vmi_{n})}{(N-1)^2}\right)\right)+Rpu}\right) \times 100\ (\%)$$

Figure S3. Read scheme: (**a**) half bias scheme and (**b**) 1/3 bias scheme and their equation for read margin.