

Supplementary Information

Effect of Post-Annealing on Barrier Modulations in Pd/IGZO/SiO₂/p⁺-Si Memristors

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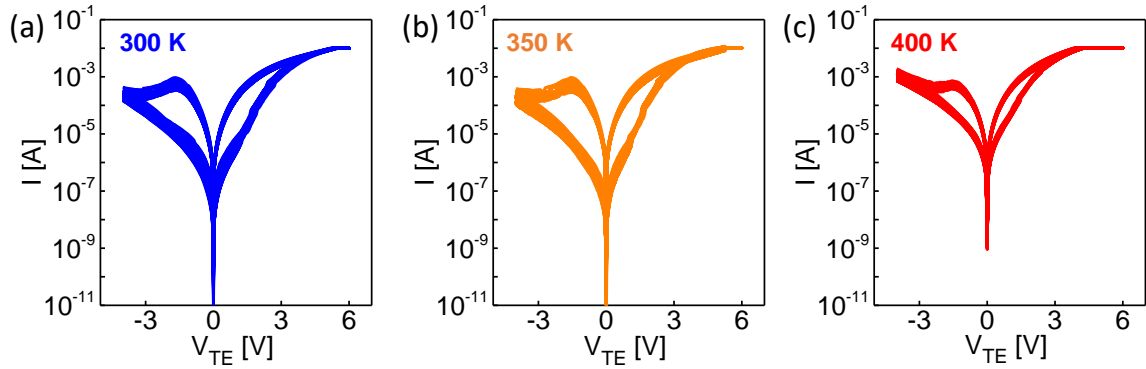


Figure S1. DC 100 cycles of the device at different temperatures (a) 300 K, (b) 350 K, and (c) 400 K.