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Probing the Electronic and Opto-Electronic Properties of Multilayer MoS₂ Field-Effect Transistors at Low Temperatures

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Abstract: Transition metal dichalcogenides (TMDs)-based field-effect transistors (FETs) are being investigated vigorously for their promising applications in optoelectronics. Despite the high optical response reported in the literature, most of them are studied at room temperature. To extend the application of these materials in a photodetector, particularly at a low temperature, detailed understanding of the photo response behavior of these materials at low temperatures is crucial. Here we present a systematic investigation of temperature-dependent electronic and optoelectronic properties of few-layers MoS₂ FETs, synthesized using the mechanical exfoliation of bulk MoS₂ crystal, on the Si/SiO₂ substrate. Our MoS₂ FET show a room-temperature field-effect mobility $\mu_{FE} \sim 40 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, which increases with decreasing temperature, stabilizing at $80 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ below 100 K. The temperature-dependent (50 K < T < 300 K) photoconductivity measurements were investigated using a continuous laser source $\lambda = 658 \text{ nm}$ ($E = 1.88 \text{ eV}$) over a broad range of effective illuminating laser intensity, P_{eff} ($0.02 \mu\text{W} < P_{eff} < 0.6 \mu\text{W}$). Photoconductivity measurements indicate a fractional power dependence of the steady-state photocurrent. The room-temperature photoresponsivity (R) obtained in these samples was found to be $\sim 2 \text{ AW}^{-1}$, and it increases as a function of decreasing temperature, reaching a maximum at $T = 75 \text{ K}$. The optoelectronic properties of MoS₂ at a low temperature give an insight into photocurrent generation mechanisms, which will help in altering/improving the performance of TMD-based devices for various applications.

Keywords: 2D materials; field effect transistors; opto-electronic transport; photodetector



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1. Introduction

Owing to the success of synthesis and applications of graphene and graphene-based materials, the scientific community has started to explore the possibility of isolating 2D atomic layers from other layered materials to investigate fundamental physics in non-carbon-based 2D crystals as well as for developing them in future electronic and optoelectronic applications. Recent advances in this area have shown that several other materials, such as hexagonal boron nitride (h-BN), transition metal di-chalcogenides (TMDCs), including MoS₂ and WS₂, and group III-VI layered semiconductors (e.g., GaSe, InSe, etc.), can be easily exfoliated from bulk crystals or grown using the CVD technique from a single to a few atomic layers [1–4]. In addition to the 2D structure, these materials also cover a wide range of the spectrum, from the insulator to semiconductors as far as the electrical properties are concerned [4–7]. For example, hexagonal B-N has a layered structure very similar to graphene, but with a very large band gap [5], whereas TMDCs MX₂ (M=Mo, W, Re, etc.) have band gap ranges from 0.8 eV to 3 eV and tunable as a function of the number of layers [6]. Some of these crystals, such as MoS₂, MoSe₂, WS₂, WSe₂, etc., show indirect to direct band gap transition when they swift from a bulk to single-atomic-layer structure due to the quantum confinement effect [7]. On the other hand, InSe [8–10], ReS₂ [11],

ReSe₂ [12] etc., show direct band gap independent to the number of layers. The magnitude of the band gap weakly depends upon the number of layers for ReS₂, where single-layer ReS₂ shows a gap at 1.5 eV and 1.58 eV for monolayer [11]. Most of the TMDCs have moderate bandgap, which results in a higher ON/OFF current ratio exceeding 10⁷ and small subthreshold voltage swing ~70 mV/decade when exploited as FETs [13]. Apart from FET applications, semiconducting TMDCs also exhibit superior optoelectronic properties, which strongly depend on the number of layers [14]. Additionally, some TMDCs are also strongly correlated electronic materials, exhibiting properties like metal-insulator quantum phase transition, superconductivity, Mott insulator, etc. [15–17].

Among the several abovementioned TMDs, the most extensively studied TMD material is MoS₂, with thickness ranging from monolayer to several tens of layers [18]. Monolayer MoS₂-based FET devices show electronic mobility 200 cm²·V⁻¹·s⁻¹ along with a very high ON/OFF ratio of 10⁸ [13]. Apart from FET applications, numerous studies show strong photo-response properties of 2D-MoS₂-based photodetectors with high photo-responsivity and detectivity [19,20]. However, performances of thin MoS₂-based photodetectors are mainly limited by low light absorption (5–10%) [20]. Further, most of the past studies are primarily focused on the room temperature as well as low-temperature electronic transport properties of either monolayer or bilayer MoS₂-based devices. We have shown in our previous study using indium-selenide-based FET [9] that both the transport mechanism as well as key figures of the merits of an FET device fabricated using a 2D-layered material depends on the number of layers. Additionally, other factors such as surface-induced trap charges, defects inside the MoS₂ channel, etc., also result in detrimental photo-response properties, such as short carrier lifetime and persistent photoconductance [21]. In comparison, multilayer MoS₂-based devices have several advantageous features, e.g., high density of states resulting in a high drive current as well as tunable electrical properties (n-type and p-type) [22]. However, multilayer MoS₂-based FETs and corresponding photo-detection properties have not been extensively studied. In this work, we have fabricated FET devices based on several-layers-thick MoS₂ and have systematically studied their electronic and photo-response properties. Multilayer MoS₂ FETs show n-type behavior with room-temperature electronic mobility ~40 cm²·V⁻¹·s⁻¹. The electronic mobility increases by almost double ~80 cm²·V⁻¹·s⁻¹ at low temperatures. We further found that maximum photo-responsivity reaches up to ~10 A/W at low temperatures while operating the FETs under the ON condition.

2. Synthesis and Device Fabrication

A few layers of MoS₂ were obtained using a mechanical exfoliation technique from commercially available bulk MoS₂ crystal (SPI Supplies). The exfoliated flakes/thin layers crystals were subsequently transferred on to a chosen substrate for device fabrication. For device fabrication, we chose a suitable MoS₂ flake. Using an optical microscope, a TEM square mesh grid (Electron Microscopy Sciences, Hatfield, PA, USA) was placed carefully on the top of the flake. This mesh grid works as a shadow mask for thermal deposition to put in direct electrical contacts. In this method, we do not use any photoresist or polymers and avoid further fabrication-process-related impurities which may lead to detrimental device performances [23]. After placing this shadow mask, the system was then mounted inside the thermal evaporator. We deposited Cr (10 nm)/Au (100 nm) for the contacts at the chamber pressure 10⁻⁶ Torr. The height of the MoS₂ flake was measured using atomic force microscopy, ~9–10 nm thick, which corresponds to ~13–15 layers of MoS₂. After deposition of the metal electrodes, the devices were annealed at a high temperature in an inert atmosphere.

3. Results and Discussion

Three terminal field-effect transistor (FET) measurements were performed on the as prepared MoS₂ devices (described in the previous section) under high vacuum ~10⁻⁶ Torr and at different sample temperatures 20 K ≤ T ≤ 280 K. To achieve the FET operation, a

small d.c voltage (V_d) of 100 mV was applied between the source and drain contacts. The gate voltage was swept between -80 V and $+80$ V, and the corresponding drain-source currents (I_d) were recorded. The fabricated devices were initially used to measure the electrical properties at room temperature. Figure 1a shows the schematic of the device with a laser light illuminating the whole device from the top. Figure 1b shows the optical micrograph image containing the 9–10 nm thick MoS₂ device (inset). The channel length and width of the devices is ~ 10 μm and ~ 13 μm , respectively.

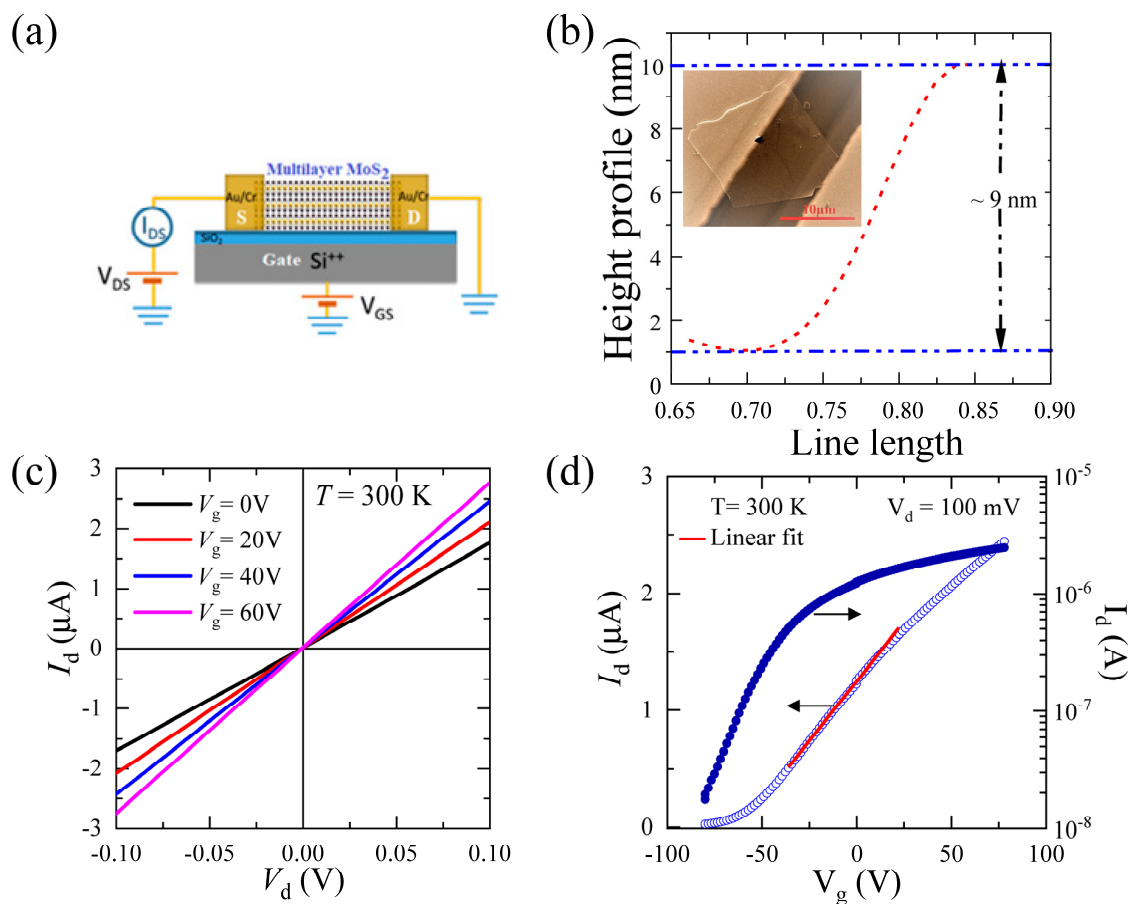


Figure 1. (a) Schematic of the three-terminal device architecture with laser light illumination in the channel region. (b) Height profile of the MoS₂ flakes (red dashed line) extracted from the optical image of the device (inset); (c) I_d - V_d characteristics of the MoS₂ FET device under different back-gate voltages. (d) Transfer (I_d - V_g) characteristics of the MoS₂ FET in linear scale (left axis) and log scale (right axis). The red color line represents the linear fit.

We used Keithley 2400 SMU to measure the drain-to-source current (I_d) by biasing the drain-to-source voltage (V_d), while gate voltages were applied using another Keithley 2410 SMU. The drain-to-source current (I_d) as a function of the drain-to-source voltage (V_d) at several gate voltages (V_g) is shown in Figure 1c. The I_d - V_d data look linear despite the Schottky barrier between the MoS₂ and Cr metal interface due to higher thermionic emission processes at room temperature. The low-temperature I_d - V_d data are presented later in this section, which reveal that the metal-semiconductor contacts are indeed of Schottky type. Figure 1d shows the FET transfer characteristics of our MoS₂ device at 300 K temperature, showing I_d as a function of V_g at $V_d = 100$ mV. A typical n-type transistor operation was observed with a threshold gate voltage (V_{th}) ~ -60 V. The drain-source current I_d reaches to the maximum saturation value of ~ 2 μA for gate voltages, $V_g > 60$ V and remains ~ 10 nA for $V_g < -60$ V. From this, we estimated the ON/OFF ratio to be $\sim 10^2$. The low ON/OFF ratio can be attributed to the higher thickness of the MoS₂ with a lower

bandgap. The red line shows the linear fit of the I_d - V_g characteristics plot and was used to extract the field-effect mobility of the device using the MOSFET transconductance formula given below,

$$\mu = \frac{L}{w} \frac{1}{C} \left(\frac{dI_d}{dV_g} \right) \frac{1}{V_d} \tag{1}$$

where L is the channel length, w is channel width, and C is the capacitance per unit area of the gate dielectric.

This n-type FET operation has been previously observed in many mechanically exfoliated single-layer MoS_2 devices. The field-effect electronic mobility was calculated from the linear region by using Equation (1) with an oxide layer thickness of 1000 nm. At 300 K, the field-effect mobility is $\sim 46 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$. This mobility value is similar to the previously obtained room-temperature mobilities of multilayered MoS_2 devices [24] and higher than single-layer MoS_2 devices [13,15]. However, with appropriate contact engineering, these mobility values can be further improved [25–28].

This higher mobility is mainly due to the higher density of states and lower Schottky barrier/Ohmic contacts found in the case of our multilayer MoS_2 device. Figure 2a shows the low-temperature FET transfer characteristics at different temperatures. We have calculated the back-gated field-effect mobilities at different temperatures, keeping the source-drain voltage constant (100 mV), as shown in Figure 2b. The mobility increases further up to $\sim 80 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ as the temperature reaches 50 K, which is generally attributed to reduced phonon scattering [29].

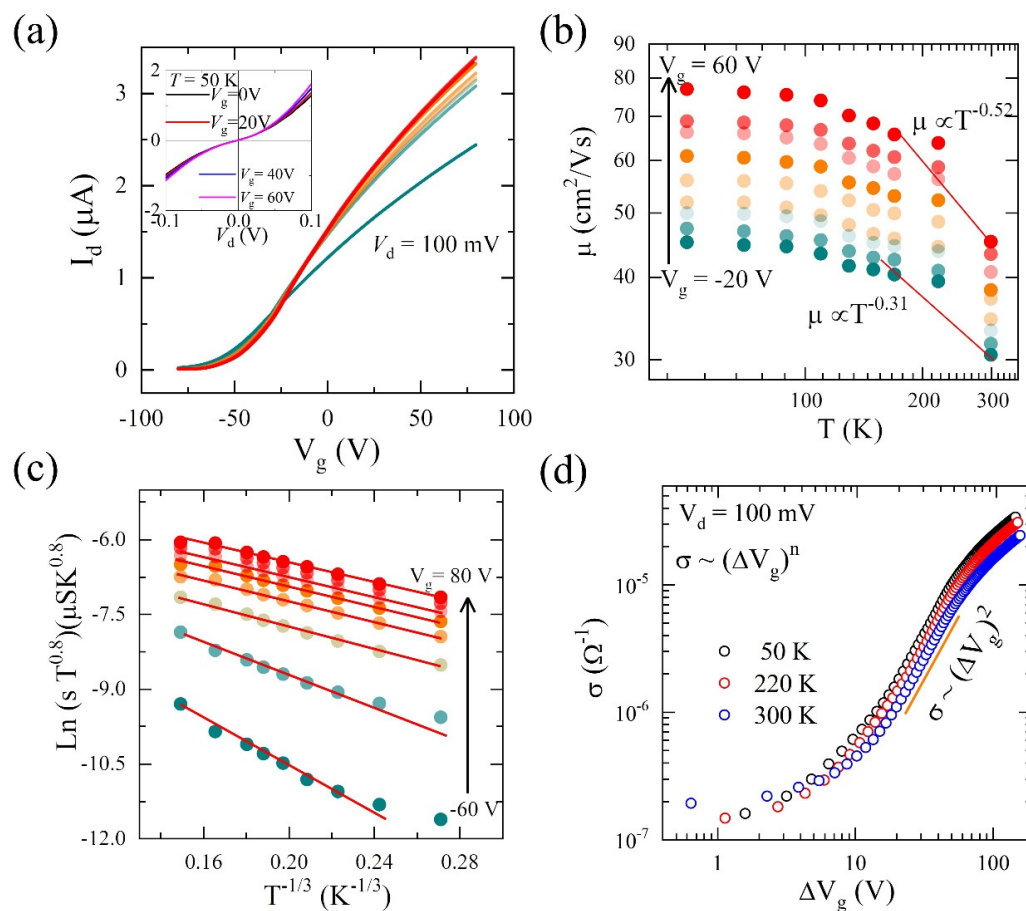


Figure 2. (a) I_d - V_g characteristics of MoS_2 FET at different temperatures ($50 \text{ K} \leq T \leq 300 \text{ K}$). (b) Temperature-dependent field-effect electronic mobility under different back-gate voltages. (c) Temperature dependence of conductivity (σ) and variable range hopping (VRH) at different back-gate voltages. (d) Variation in conductivity σ with ΔV_g at different temperatures.

The charge carrier transport in 2D semiconductors is mainly dependent on the carrier density or equivalently on the Fermi energy level E_F [30–33]. When the charge carrier density is “very-low”, the Fermi level E_F lies in the bandgap region without any mobile carriers. In this case, the system remains in a disorder-driven strongly localized insulating phase. In the case of an n-type semiconductor, the application of a positive gate-bias moves the Fermi level towards the conduction band edge. This results in the generation of mobile electrons by filling up the localized states by thermal excitation. Further increment in the gate bias shifts the Fermi level above the mobility edge, and thus the band transport becomes more dominant. Finally, when the carrier density becomes “very-high”, a strong apparent metallic phase is observed. At higher temperatures and at “very-high” doping level, the charge carrier transport is often influenced by the phonon effects and by short- and long-range scatterers, such as defects and charged impurities. The transition from the insulating state to the conducting state involves gradual progressive filling of the localized states or band edge disordered states arising from impurities and/or structural defects. At the intermediate carrier density level, charge carrier conduction occurs via the hopping of charge carriers through the localized states [34–37]. These type of conduction mechanisms can be described by the variable range hopping (VRH) model, which can be expressed by the following equation [34,38]:

$$\sigma(n, T) = A \cdot T^m \exp \left[- \left(\frac{T_0}{T} \right)^\gamma \right] \quad (2)$$

where the exponent $\gamma = 1/(d + 1)$, d is the dimension of the system ($d = 1$ for 1D system and $d = 2$ for 2D systems), $m = 0.8$ is an empirical constant, T is the temperature, T_0 is the characteristic temperature, and $\sigma(n, T)$ is the 2D conductivity.

To further confirm the charge transport mechanism process in our MoS₂ devices, we plotted the natural logarithm of the conductance as a function of $T^{-1/3}$ for different back-gate voltages, as shown in Figure 2c. Here we found that the charge transport for our MoS₂ device follows 2D VRH mechanisms, as given by Equation (2), over a wide range of temperatures $50 \text{ K} \leq T \leq 300 \text{ K}$. These 2D VRH mechanisms further support mobility $T^{-1/3}$ dependence, similar to the results found in monolayer MoS₂ devices [34].

In crystalline MoS₂, the presence of a high density of localized states in the band-gap region leads to hopping transport when the Fermi level moves through them upon changing the gate voltages. According to previous results [34], the physical origin of these localized states in MoS₂ films is connected to the random potential fluctuations from the trapped charges at the MoS₂-SiO₂ interface. Since the screening of these trapped charges is relatively poor due to the large band gap of MoS₂, a considerably long band tail thus exists from the interfacial traps which are randomly occupied during the processing of the device. For a 2D system with parabolic energy bands, if the main source of disorder arises from the randomly occupied interfacial traps, the scattering mechanisms are also expected to be dominated by charge impurity scattering [39]. This will further lead to:

$$\sigma \propto n \quad (\text{for screen coulomb impurity}) \quad (3a)$$

$$\sigma \propto n^2 \quad (\text{for bare Coulomb impurity}) \quad (3b)$$

Therefore, to understand the scattering mechanism in our devices, we have plotted the conductance σ as a function of the change in the back-gate voltage (ΔV_g) at different temperatures, as shown in Figure 2d. We found that for our MoS₂ devices towards the higher gate voltages, σ almost follows the power law expression $\sigma \sim \Delta V_g^{-2}$ for all different temperatures, which indicates scattering from almost unscreened charge impurities in our MoS₂ devices.

4. Optoelectronic Transport

The optoelectronic properties of MoS₂ FET were investigated by using a continuous wave laser with an illumination wavelength $\lambda = 658$ nm ($E = 1.88$ eV) and a spot size of ~ 3 mm in diameter. A larger laser spot size helps reduce photo-thermal effects, such as the photo-thermoelectric effect, photo-bolometric effect, etc., as both contacts are illuminated alike [40]. Additionally, laser illumination intensity (P_{laser}) is scaled to an effective laser illumination intensity (P_{eff}) owing to a larger laser spot size as $P_{\text{eff}} = P_{\text{laser}} \times A_{\text{device}}/A_{\text{spot}}$, where A_{device} is the area of a device and A_{spot} is the area of a laser spot. Room-temperature optoelectronic transport measurements of an MoS₂ FET are shown in Figure 3. A continuous laser was switched ON and OFF for an interval of ~ 10 s, and the corresponding drain currents were measured. With the data shown in Figure 3a,b, it can be estimated that the decay response times of this device studied are very fast, perhaps of the order of a few seconds; however, due to the limitation of the measurement system, an accurate determination of this parameter was not possible. Photocurrents (I_{ph}) were estimated as a difference between the drain current under laser illumination (laser on) and the drain current under a dark current (laser off) as $I_{\text{ph}} = I_{\text{d,laser ON}} - I_{\text{d,laser OFF}}$. The time-dependent response of the photocurrent at $V_g = 0$ V and various V_g 's is shown in Figure 3a,b, respectively. It was observed that the photocurrent reverts to the drain current under dark conditions as soon as the laser is switched off, implying the presence of only a photoconductive/photogating effect.

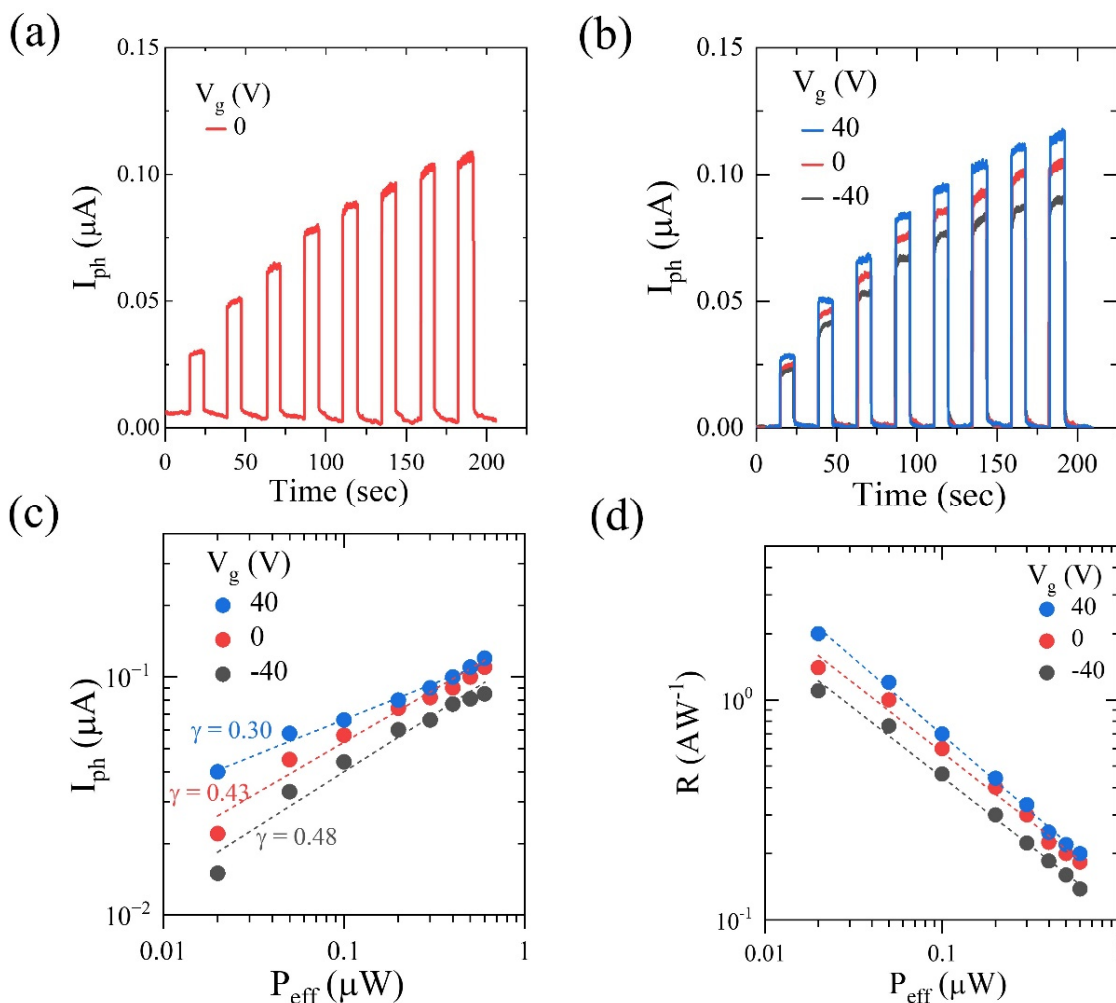


Figure 3. (a) Photocurrent vs. time at room temperature with no back-gate voltage and (b) with different back-gate voltages. (c) Photocurrent vs. effective power illumination in the whole channel region in log–log scale. (d) Responsivity vs. effective power under different back-gate voltages.

The photocurrent (I_{ph}) extracted for three different applied gate voltages ($V_g = -40$ V, 0 V, 40 V) is plotted as the function P_{eff} in log–log scale, as shown in Figure 3c. The photocurrent follows power law dependence on the effective laser illumination intensity as $I_{ph} \propto (P_{eff})^\gamma$. The value of the exponent is $0 \leq \gamma \leq 1$, indicating the presence/absence of trap states in FET. In the absence of trap states, the exponent, $\gamma = 1$, and photocurrent generation mechanism follow a pure photoconductive effect. In the presence of trap states, the exponent becomes fractional ($\gamma < 1$) and the photocurrent mechanism manifests into a trap-dominated photoconductive effect, commonly known as the photogating effect. It should be noted that crossover of a photo generation mechanism from photoconductive to photogating because of an increased applied gate voltage has been observed in various 2D materials, such as In_2Se_3 [40], $CuIn_7Se_{11}$ [41], and $ReSe_2$ [42], which indicates that trap states can be modulated. However, the fractional value of γ for all gate voltages (in Figure 3c) indicates that the trap states in MoS_2 FET have a strong influence on the optoelectronic properties of MoS_2 FETs.

The photo-responsivity (commonly known as responsivity) of a phototransistor can be estimated by $R = I_{ph}/P_{eff}$. The responsivity as a function of P_{eff} in log–log scale for three different applied gate voltages is shown in Figure 3d. In the case of a pure photoconduction-generated photocurrent (where photoconductive gain is absent), responsivity will have an upper limit, given by $R = (\eta \times e \times \lambda)/(h \times c) = \eta \times \lambda/1240$, where η is the quantum efficiency, e is the electron charge, h is the plank's constant, and c is the speed of light [43,44]. For a laser with $\lambda = 658$ nm, a maximum R of 0.53 A W^{-1} can be achieved for $\eta = 1$ (100% conversion). For MoS_2 FET, responsivity values greater than 0.52 (as seen in Figure 3d) indicate that the gain > 1 . Gain can be estimated as τ_m/τ_d , where τ_m is the minority carrier lifetime and τ_d is the carrier drift or transit time [45]. For gain > 1 , $\tau_m > \tau_d$, which means that minority carriers are immobile and trapped. This results in a trap-dominated photoconductive effect. As seen in Figure 3d, the responsivity decreases as the effective laser intensity increases, and this could be attributed to a decrease in the average carrier lifetime of minority charge carriers [43]. As light intensity increases, trap states gradually start filling up. At certain light intensities, all the trap states are filled, and a further increase in intensity will result in the generation of minority carriers that cannot be trapped. As a result of this, τ_m decreases, thus reducing the gain and the responsivity [43]. For MoS_2 FET, a maximum $R = 2 \text{ A W}^{-1}$ at 300 K can be obtained at $P_{eff} = 0.02 \text{ }\mu\text{W}$ and $V_g = 40$ V. When the gain > 1 , quantum efficiency (η) is known as the external quantum efficiency (EQE) and is defined as $EQE = R(h \times c)/(e \times \lambda) = R \times 1240/\lambda$. We found a maximum EQE of $\sim 380\%$ at $P_{eff} = 0.02 \text{ }\mu\text{W}$ and $V_g = 40$ V.

Temperature plays an important role in determining the strength of traps states. Thus, to emphasize the role of traps states on the photogeneration mechanism, we studied the optoelectronic properties at a low temperature ($50 \text{ K} < T < 300 \text{ K}$). Photocurrents at all studied temperatures show similar behaviors as that of those at room temperature. The time-dependent response of the photocurrent (at various V_g 's) measured at the lowest temperature is shown in Figure 4a, and the photocurrent reverts to the drain current under the dark condition as soon as the laser is switched OFF. Responsivity is a function of P_{eff} at constant $V_g = 40$ V, and all the temperature studies are shown in Figure 4b. Responsivity increased as temperature decreased, indicating strong trapped states.

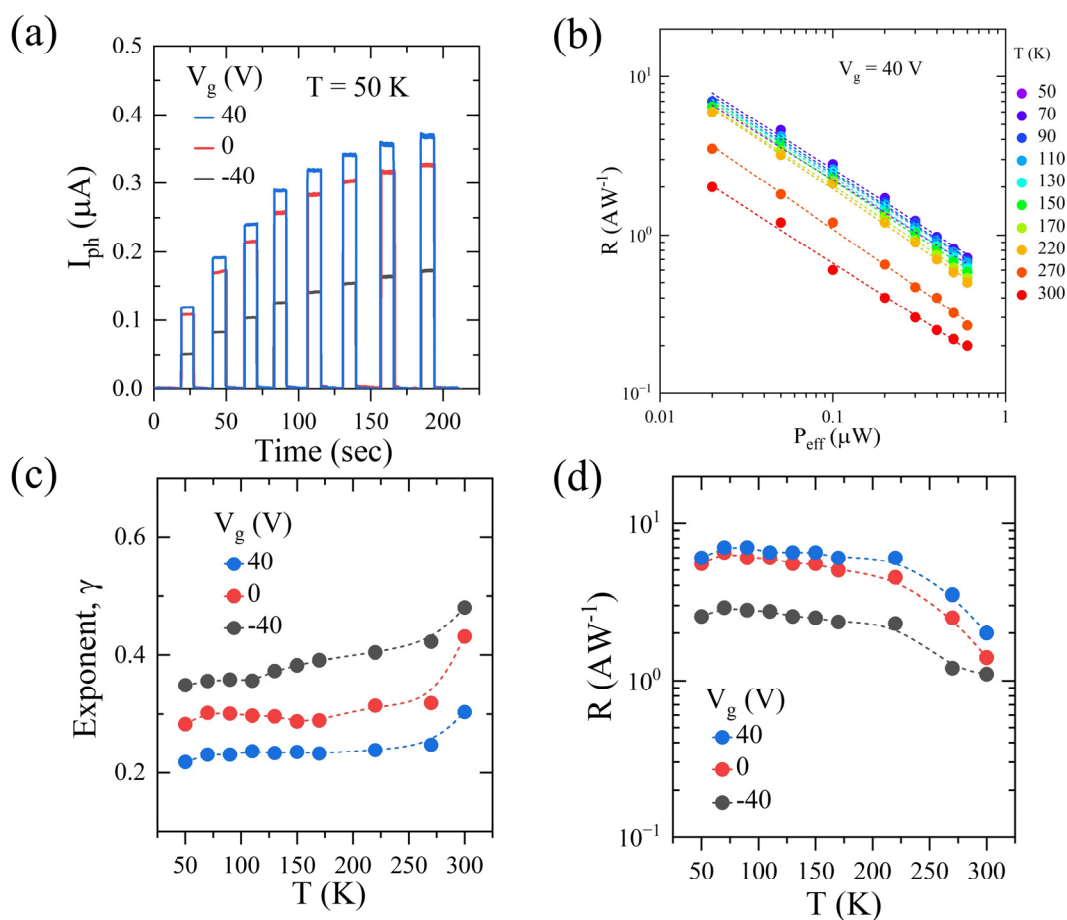


Figure 4. (a) Photocurrent vs. time under different back-gate voltages. (b) Responsivity variation with effective power and temperature under back-gate voltage of 40 V. (c) Exponent (γ) vs. temperature (extracted from (c)); (d) responsivity vs. temperature.

The temperature dependence of γ and R is shown in Figure 4c,d, respectively. It is observed that as temperature decreases, γ decreases, and, correspondingly, responsivity increases for all the studied gate voltages (V_g 's). A strong dependence of γ and R have been observed in various 2D-materials-based FETs, and this was studied in detail in the case of ReSe₂ [42]. A clear correlation between R and γ was observed, where lower γ corresponds to higher R . These parameters are determined by trap states, and these traps can be modulated by temperature and gate voltages. In a semiconductor where the steady-state Fermi level is away from the valence band, this results in mid-gap states being available for trapping. Lowering the temperature results in carrier freeze out and strongly trapped minority carriers, resulting in a strong photogating effect. Thus, responsivity increases at lower temperatures.

5. Conclusions

In conclusion, here we have presented the detailed temperature-dependent electronic and optoelectronic properties of few-layers MoS₂ FETs. Our MoS₂ FETs show mobility $\mu_{FE} \sim 40$ cm²·V⁻¹·s⁻¹ at room temperature and 80 cm²·V⁻¹·s⁻¹ below 100 K. The temperature-dependent (50 K < T < 300 K) photoconductivity measurements show the room-temperature photoresponsivity (R) to be ~ 2 AW⁻¹, and this increases as a function of decreasing temperature. Photoconductivity measurements indicate a fractional power dependence on the steady-state photocurrent, indicating trap-controlled optoelectronic properties. Understanding the optoelectronic properties of MoS₂ at low temperatures will help in altering/improving the performance of TMD-based devices for various applications. Further, these studies may lead to the development of broadband photodetectors, as shown

by Wei et al. [46], using ternary-selenide-based materials or components in neuromorphic computing [47].

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