# Artificial Synapse Emulated by Indium Tin Oxide/SiN/TaN Resistive Switching Device for Neuromorphic System

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**Abstract:** In this paper, we fabricate an ITO/SiN/TaN memristor device and analyze its electrical characteristics for a neuromorphic system. The device structure and chemical properties are investigated using transmission electron microscopy and X-ray photoelectron spectroscopy. Uniform bipolar switching is achieved through DC sweep under a compliance current of 5 mA. Also, the analog reset phenomenon is observed by modulating the reset voltage for long-term memory. Additionally, short-term memory characteristics are obtained by controlling the strength of the pulse response. Finally, bio-inspired synaptic characteristics are emulated using Hebbian learning rules such as spike-rate-dependent plasticity (SRDP) and spike-timing-dependent plasticity (STDP). As a result, we believe that the coexistence of short-term and long-term memories in the ITO/SiN/TaN device can provide flexibility in device design in future neuromorphic applications.

**Keywords:** resistive switching; neuromorphic system; synaptic plasticity; Hebbian learning rules; short-term memory

## 1. Introduction

The amount of data we can access is continuously expanding as industrial technology advances. Significant issues arise as a result of the access speed disparity between the CPU resistor and the main memory in von-Neumann computing architecture, which results in a decrease in data processing performance. As a result, the available data hit a bottleneck, limiting its amount [1]. To overcome the bottleneck problem, a novel computing design known as neuromorphic computing architecture is proposed [2]. Neuromorphic computing architecture is based on parallel processing mimicking the human brain, where information proceeds through pre- and post-synapse chemical interactions. The structure based on an artificial neural network (ANN) has advantages in terms of power consumption due to its ability to process large amounts of data in parallel [3,4].

Additionally, charge-based NAND flash memory is about to face limitations in non-volatile storage technology due to its scaling limits [5]. To address the aforementioned issues, different next-generation non-volatile memories such as phase-change memory (PCM) [6], magnetic random-access memory (MRAM) [7], ferroelectric random-access memory (FRAM) [8], and resistive random-access memory (RRAM) [2,9–13] are emerging. RRAM is a viable contender among them due to its high scalability, low-power operation, fast switching speed, long retention time, and high endurance [14–21]. Moreover, due to the simple metal–insulator–metal structure, RRAM has the additional benefits of simple fabrication and mimicking the human brain, where the top electrode metal imitates the pre-synapse and the bottom electrode metal mimics the post-synapse [22]. It is reported that various metal oxides can act as an insulating active layer of RRAM, including $TaO_x$ [23], $HfO_x$ [24], $AlO_x$ [25], $ZnO$ [26], and $ZrO_x$ [27]. Under applied bias, these metal oxides form a conducting filament through oxygen-vacancy migration, inducing a change in their resistance state. However, an unstable interface is formed between the electrode and the insulating layer, creating fluctuations in cycle-to-cycle uniformity because of the high

reactivity of oxygen ions [28,29]. Recently, studies have focused on nitride-based insulating layers such as AlN [30], SiN [31,32], and WN [33] because of their excellent electrical properties and ionic chemistry, providing a choice to solve the mentioned problems of metal oxides [34,35]. The performance of SiN-based resistive switching devices compared with metal-oxide-based resistive switching devices is summarized in Table 1.

**Table 1.** Performance of nitride-based devices compared with oxide-based devices in previous reports.

| No | Structure | Endurance | On/Off Ratio | Retention | Ref. |
|----|-----------|-----------|--------------|-----------|------|
| 1 | $ITO/WO_x/TiN$ | <10 | NA | NA | [2] |
| 2 | $ITO/WO_x/TaO_x/TiN$ | $>10^2$ | >10 | $>10^4$ | [2] |
| 3 | $Ag/ZnO/TiN$ | <936 | <10 | NA | [18] |
| 4 | $TiN/SiOx/ITO$ | $>2 \times 10^2$ | NA | $>10^4$ | [19] |
| 5 | $ITO/SiN/TaN$ | $>10^3$ | >43 | $>10^4$ | This work |

Silicon nitride has been widely studied as a passivation and buffer layer in complementary metal–oxide–semiconductor (CMOS) technology. It is also utilized in flash memory as a charge-trapping layer. Recently, researchers have reported the usage of SiN in RRAM applications, where it is used as a switching layer due to its rich inert defects [36–38]. Furthermore, SiN films were reported to have advantages in resistive switching processes such as quick switching speed, extended retention time, high cycle durability, and a large on/off ratio [39–41]. Some studies have concentrated on the synaptic applications of SiN-based RRAM devices. Kim et al. reported the co-existence of short-term memory (STM) and long-term memory (LTM) characteristics of $Ni/SiN_x/SiO_2/Si$ devices [42]. Choi et al. described the potentiation and depression properties of $Ni/SiN_x/Si$ devices [43]. Rahmani et al. observed spike-timing-dependent plasticity behavior in $Ni/SiN/BN/Si$ devices [44].

In this work, we investigate more kinds of long- and short-term characteristics of ITO/SiN/TaN. The top electrode ITO is chosen because of its high inert resistance, which can prevent a hard breakdown of the device [45,46]. The device exhibits affirmative characteristics as a memory device, showing good endurance and retention characteristics over 1000 cycles and $10^4$ s, respectively. Additionally, various pulse tests are conducted on the device to obtain short-term characteristics such as paired-pulse facilitation (PPF) [47], paired-pulse depression (PPD) [48], and electric excitatory postsynaptic current (EPSC) [49,50] by altering the compliance current, pulse interval, and pulse width. Finally, Hebbian rules are tested to seek neuromorphic applications [51]. The tests involve potentiation and depression under identical and incremental pulse schemes, spike-rate-dependent plasticity (SRDP), and spike-timing-dependent plasticity (STDP), proving its future applications as a memory device [52–54].

## 2. Materials and Methods

The ITO/SiN/TaN device was prepared by performing the following steps. A 100 nm-thick TaN bottom electrode was deposited on a $SiO_2/Si$ wafer through DC sputtering using a Ta target (99.99% purity) under a power of 65 W. With a deposition pressure of 5 mTorr, the sputtering gas was a mixture of Ar (19 sccm) and $N_2$ (1 sccm). A 6 nm-thick insulating SiN film was deposited through plasma-enhanced chemical vapor deposition (PECVD) (Oxford Instruments, Tubney Woods, Abingdon, UK) at a temperature of 250 °C and an RF power of 100 W. The reactive gas consisted of $SiH_4$ (5%), He (95%), $NH_3$ (9 sccm), and N2 (450 sccm). Then, using photolithography, square patterns of 100 μm × 100 μm were made. Finally, a 110 nm thick Indium Tin Oxide (ITO) top electrode was achieved through a lift-off process in acetone after depositing ITO through RF sputter using a commercial ITO target (99.99% purity) with an RF power of 80 W. The gas pressure was 3 mTorr with Ar of 8 sccm. To determine the DC and pulse characteristics of the device, the electrical properties were characterized using a Keithley 4200-SCS semiconductor parameter analyzer (Keithley Instruments, Cleveland, OH, USA) and a 4225-PMU pulse measuring

unit (Keithley Instruments, Cleveland, OH, USA). The top electrode (ITO) was biased, while the bottom electrode (TaN) was grounded. X-ray photoelectron (XPS) analysis and transmission electron microscopy (TEM) (Oxford Instruments, Tubney Woods, Abingdon, UK) were used to examine the depositions and chemical properties of the device.

## 3. Results and Discussion

The schematic illustration of the fabricated ITO/SiN/TaN device is shown in Figure 1a. In Figure 1b, the cross-sectional image of an ITO/SiN/TaN device is investigated through transmission electron microscopy (TEM). It is observed that the film thickness of PECVD-deposited amorphous SiN is about 6 nm. It is noted that the surface of the SiN film is not flat. The surface roughness could produce the electric field that affects the resistive switching [55,56]. The uneven surface can cause the variation in switching parameters even though the enhancement of the electric field can reduce the switching voltage [57].
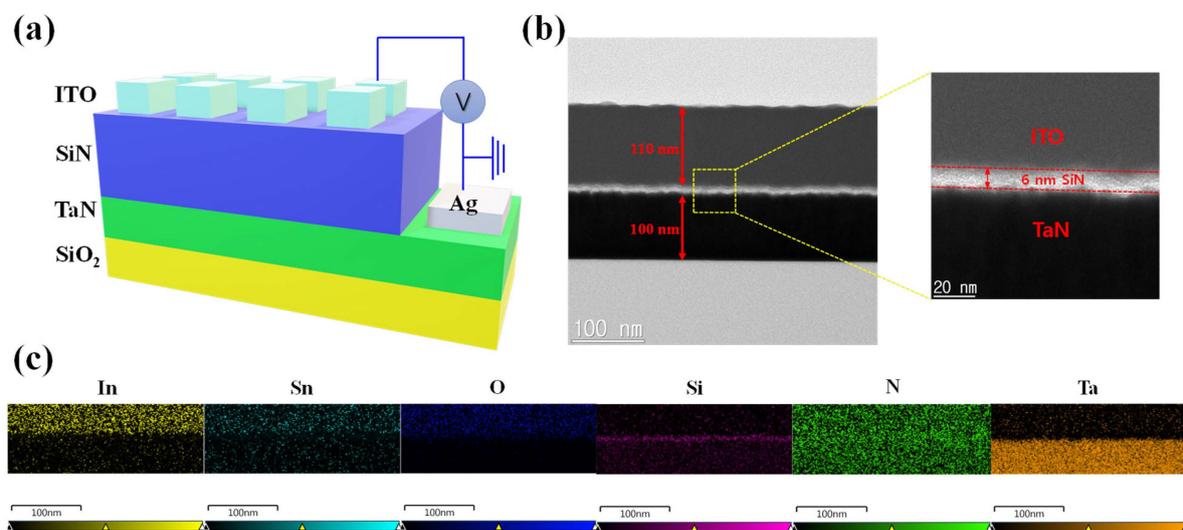


**Figure 1.** (**a**) Schematic illustration of the ITO/SiN/TaN memristive device structure. (**b**) Typical cross-sectional TEM image of ITO/SiN/TaN structure. (**c**) EDS color mapping of In, Sn, O, Si, N, and Ta.

The top and bottom electrode thicknesses are about 110 nm and 100 nm, respectively. Figure 1c shows the energy dispersion X-ray spectroscopy mapping of In, Sn, O, Si, N, and Ta elements in the ITO/SiN/TaN device. The spatial distribution of each element in the ITO/SiN/TaN device is observed. It is shown that the nitrogen overlaps the area of ITO, which can be inferred as the formation of an ITON layer. To further investigate the chemical compositions of a 6 nm-thick insulating layer, an XPS in-depth profile mode is conducted. The XPS spectra of the SiN film at the etch time of 6 s are shown in Figure 2. Figure 2a shows the Si 2p spectra, where its peak is located at a binding energy of around 101.97 eV for the Si-N bond [32]. Furthermore, the N 1s spectra are illustrated in Figure 2b with a peak at 498.32 eV, corresponding to the Si-N bond. Nitrogen diffuses during the reactive sputtering process of ITO deposition on a silicon nitride layer.

Next, the electrical characteristics of the ITO/SiN/TaN device are investigated. As shown in Figure 3a, the electrical soft breakdown process [52,53] under a voltage of 5.5 V and a compliance current of 1 mA is needed to switch the device from its initial resistance state to a low-resistance state (LRS). The strong bias applied to the top electrode gathers the initial randomly scattered defects in the SiN thin film and forms an initial conducting filament, increasing the flow of current. The set and reset processes occur under voltage biases of about 3 V and –3 V, with a compliance current of 5 mA. The first and 100th I–V cycles are shown in Figure 3b. The high-resistance state (HRS) and LRS are repeatedly switched without severe breakdown. To further observe the cycle-to-cycle variance of

the device, a DC sweep over $10^3$ cycles is performed as shown in Figure 3c. Each resistance state is distinguishable during the cycles, obtaining an average on/off ratio of 43.98. Figure 3d shows the retention characteristics of the device in the LRS and HRS at a read voltage of 0.1 V. Each LRS and HRS maintains their resistance level over $10^4$ s, displaying promising non-volatile memory properties [49]. Furthermore, analog reset, which is critical for neuromorphic computing applications for multi-level states [58,59], is illustrated in Figure 3e. The set process occurs in a single digital set process at 3 V and a sequential reset process occurs by modulating the reset voltage from –2 V to –3 V. To confirm the cell-to-cell uniformity of ITO/SiN/TaN, 10 randomly selected cells are tested under the same voltage bias of 3 V and –3 V over 20 cycles. As shown in Figure 3f, a significant difference in HRS is observed in all 10 cells, showing its cell-to-cell uniformity.
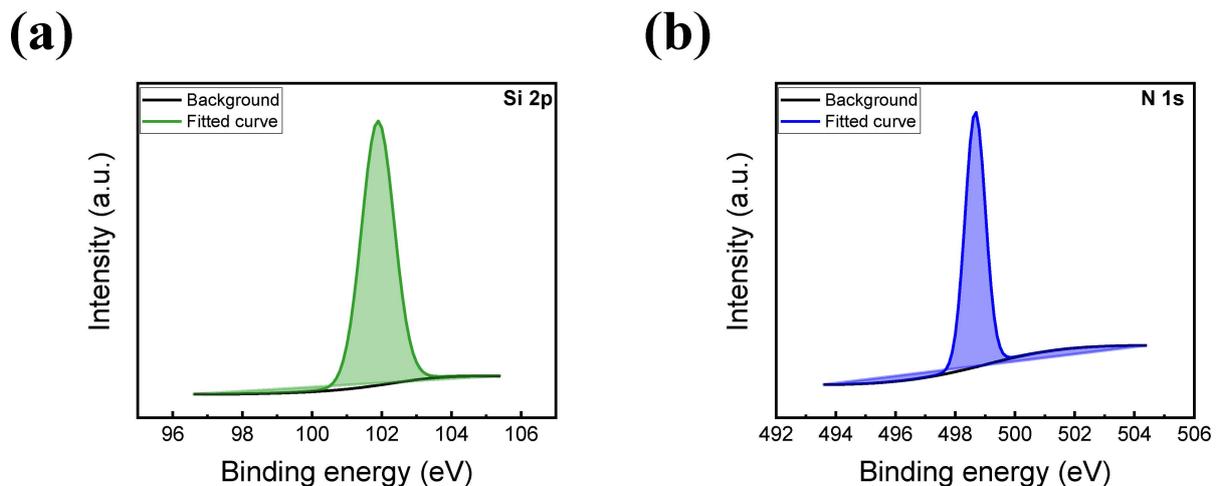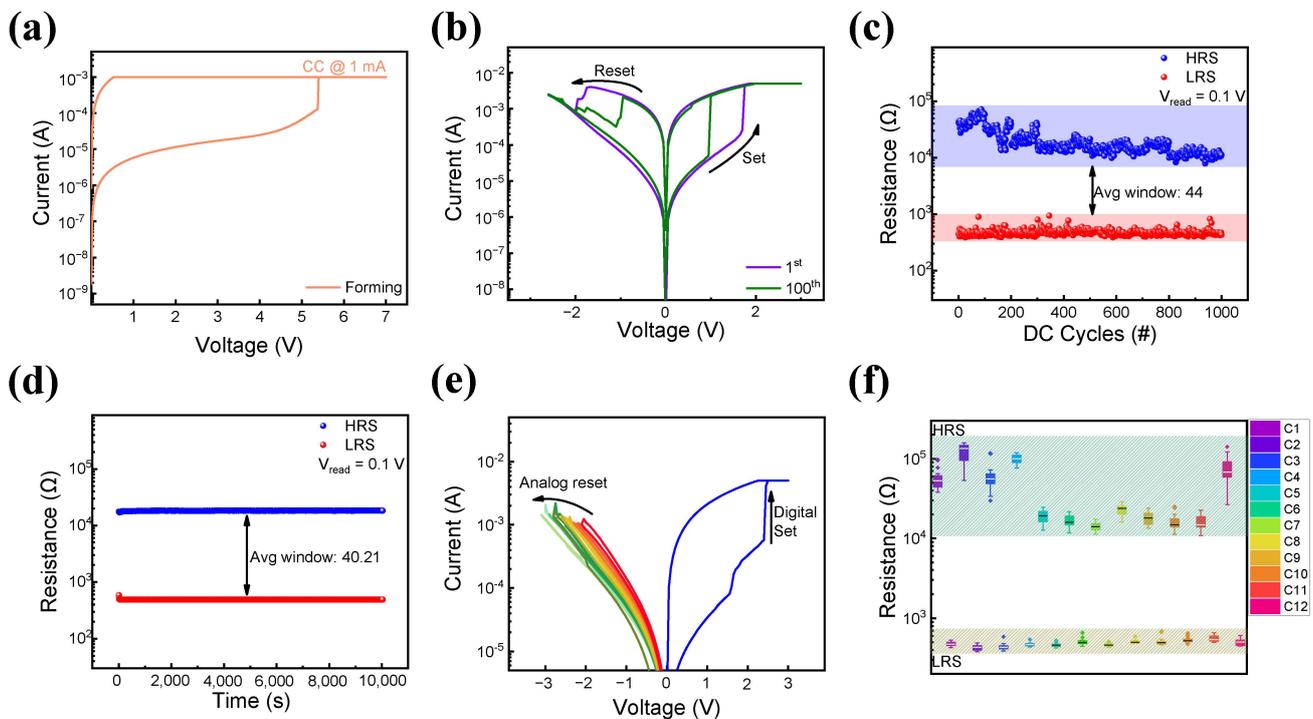


**Figure 2.** XPS spectra of (**a**) Si 2p and (**b**) N 1s.



**Figure 3.** (**a**) Initial breakdown process of ITO/SiN/TaN device. (**b**) I-V curves of the 1st and 100th DC sweep cycles. (**c**) DC endurance performance over $10^3$ cycles. (**d**) Retention characteristics of HRS and LRS over $10^4$ s. (**e**) Analog reset process of the device. (**f**) Cell-to-cell uniformity over 10 cells.

Figure 4 illustrates a conduction mechanism based on the migration of nitride vacancies based on the I–V characteristics of Figure 3. When the top electrode is biased positively, nitride ions ($N^{3-}$) move toward the top electrode ITO, forming a nitride-rich ITON layer that works as a nitride reservoir. The remaining nitride vacancies (silicon dangling bond) aggregate and form a conducting filament toward the top electrode. Under continuous voltage bias, the filament tip contacts the top electrode and the device, and a large amount of current flows through conducting filament. Thus, the device switches from an HRS to an LRS, which is an "on" state (Figure 4a) [60,61]. On the other hand, when a negative voltage is applied to the top electrode, nitride ions that have gathered in the ITON region are expelled to their original location, recombining with the nitrogen-vacancy and rupturing the conducting path. As a result, the current level of the device decreases, switching it from an LRS to an HRS, and the device is turned "off" (Figure 4b) [62].
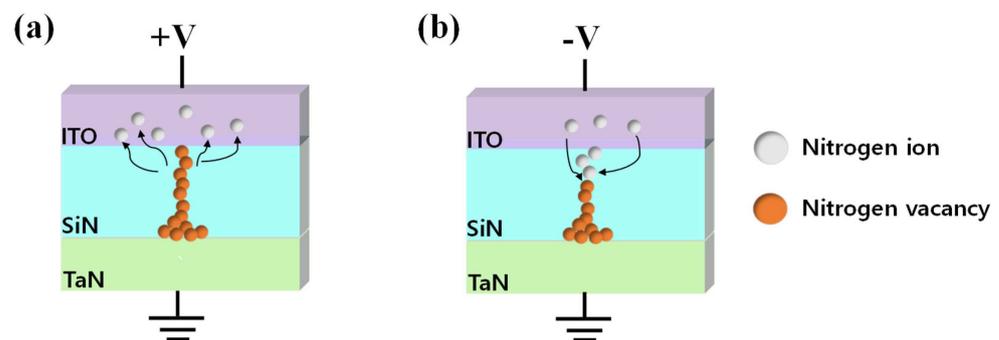


**Figure 4.** Conduction mechanism of ITO/SiN/TaN device. (**a**) Set process. (**b**) Reset process.

Multi-level cell (MLC) characteristics are important factors in memory devices due to their practical applications in high-density memory and neuromorphic devices [63–66]. In a single-level cell (SLC), for example, one cell retains two bits, meaning that the cell only remains in two types of resistance states: LRS and HRS [67]. On the other hand, MLCs can display multiple resistance states, increasing the storage density. Two controllable approaches exist to embody MLCs; the first is by controlling the compliance current in the set operation [68]. During the set operation, defects accumulate, forming a conducting filament. In this process, compliance current is applied to avoid the hard breakdown of the device by limiting the size of the conducting filament and restricting the current flow. Thus, the current flow can be optimized by the applied compliance current, resulting in multiple LRS states while the HRS level remains the same. As shown in Figure 5a, while the off current remains at the same level in all compliance current statuses, the on current can be varied. The second way to obtain MLC is by changing the reset voltage [69]. In the reset process, nitride ions that migrate into the ITON layer repel back to their original space. This can be noted as the amount of repelled ions can be controlled by the strength of the reset voltage applied to the top electrode, controlling the rupture of the conducting filament. Thus, when a strong reset voltage is applied, the conducting path will be more ruptured, resulting in a multi-HRS state with the same LRS. Figure 5c shows the I-V of the ITO/SiN/TaN device with different reset voltages applied from −2.6 V to −3.2 V. As shown, four different acquired I-Vs have the same LRS but differing HRS. To determine the ability of the device to maintain its multi-level states as a non-volatile memory, retention characteristics are tested and read at 0.1 V. The result is illustrated in Figure 5b,d, where the states remain in their resistance state over $10^4$ s without significant variance.
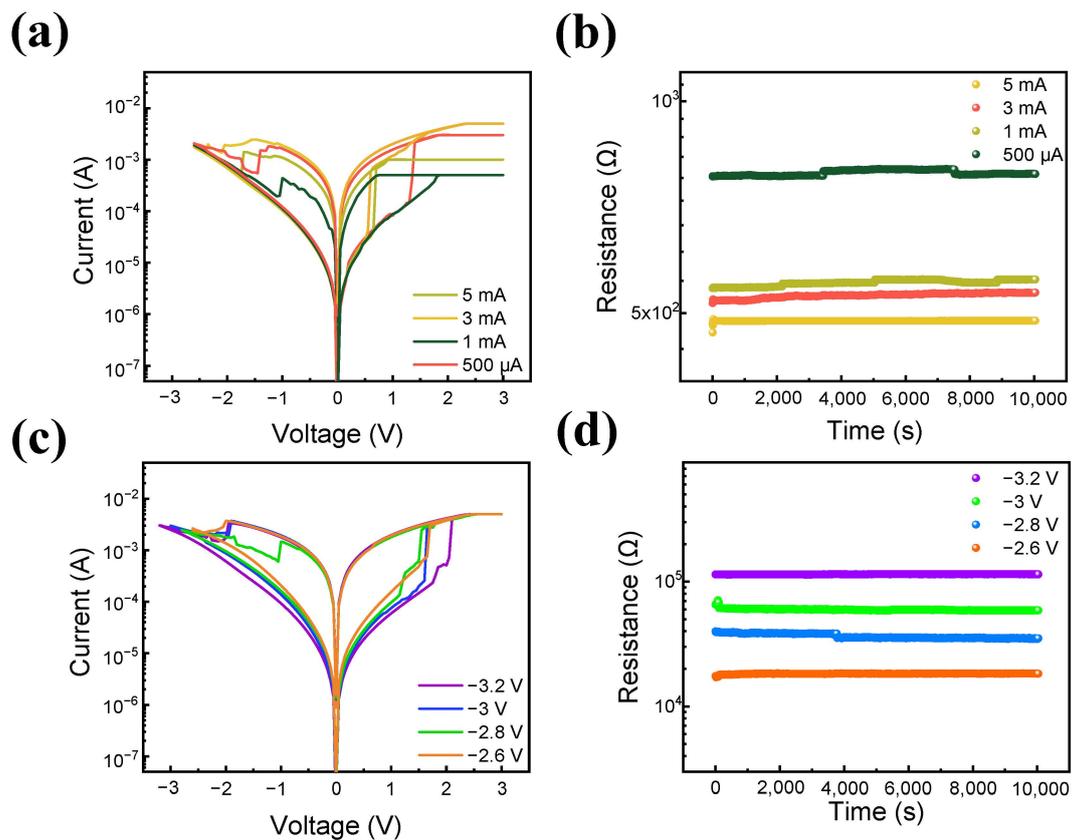
**Figure 5.** (**a**) MLC characteristics under different compliance currents. (**b**) Retention characteristics of MLC under different compliance currents. (**c**) MLC characteristics under different reset voltages. (**d**) Retention characteristics of MLC under different reset voltages.

In the human brain, various information processes occur to realize memory. This information processing is frequently influenced by synaptic plasticity, which is a method for modulating synaptic weight between the post- and pre-synapse. The synaptic weight is updated by the interval time of electrical input between the pre- and post-synapse [70,71]. To mimic a biological synapse, AC pulse analyses are usually used. One way to perform neuromorphic applications on an electronic synaptic device is through potentiation and depression. Long-term potentiation (LTP) and long-term depression (LTD) characteristics are found in ITO/SiN/TaN devices by applying pulses of 50 identical set pulses and 50 identical reset pulses. The pulse train is composed of a pulse width and an interval of 1 μs. The pulse voltage is 2.5 V and −2.5 V for each set, and the reset pulse train with data reads at a read voltage of 0.1 V. Figure 6a shows an increase and decrease in conductance states. A five-cycle pulse cycle of LTP and LTD is demonstrated by the consecutive set and consecutive reset pulses in Figure 6b. However, when developing neuromorphic computing systems, the linearity and asymmetry of LTP and LTD are critical considerations [72]. To regulate the non-linearity of the LTP process, we use an incremental pulse train with a voltage ranging from 1.8 V to 2.5 V on the device. The result of incremental pulse application is shown in Figure 6c, showing the improved linearity of conductance change. To further seek the application of ITO/SiN/TaN devices in neuromorphic computing applications, the pattern recognition system (PRS) based on the Modified National Institute of Standards and Technology database (MNIST) is tested using Python and Google Colab. The PRS is divided into three categories, as indicated in Figure 6d: the input, output, and hidden neurons. The conductance graph of LTP and LTD is translated into a 28 × 28 MNIST handwritten image where the pixel change follows the change in conductance. Then, the numbers are inserted into PRS, where neurons in each layer calculate the correctness of the handwritten image.

Figure 6e shows the calculated accuracy in which the gradual and linear incremental pulse scheme has a better accuracy of 97.22%.
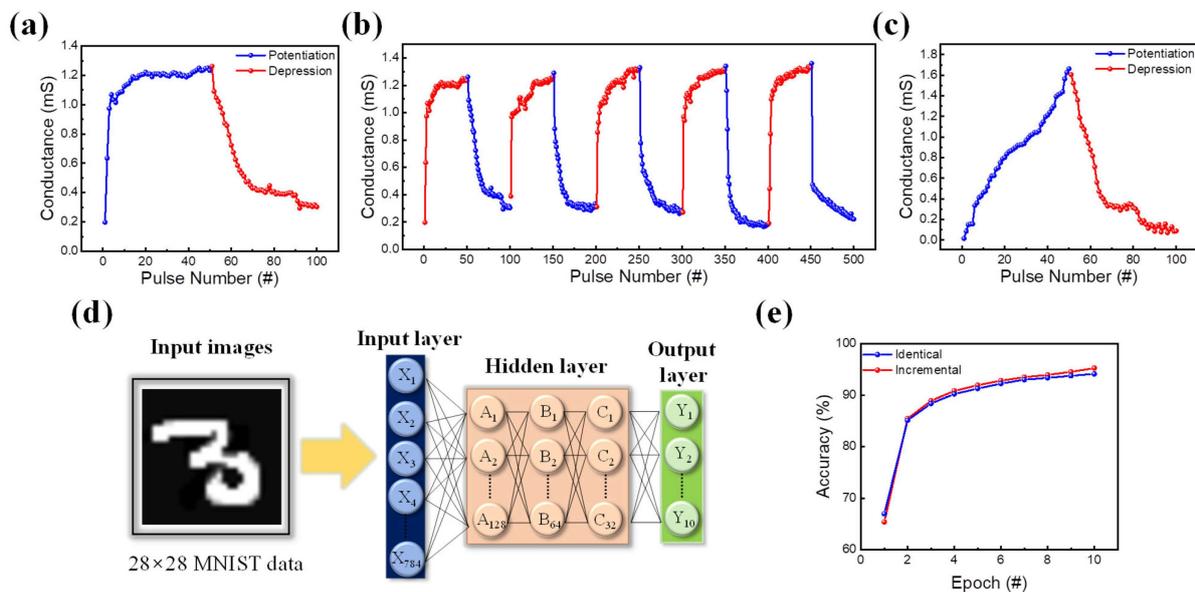


**Figure 6.** (**a**) Potentiation and depression. (**b**) 5-cycle potentiation and depression. (**c**) Result of the incremental pulse scheme applied to the ITO/SiN/TaN device. (**d**) Deep neural network simulation framework for MNIST pattern recognition. (**e**) The pattern recognition accuracy of a synaptic device over ten consecutive epochs.

In addition to long-term memories, the human brain has short-term memories that we swiftly forget. Thus, when emulating the human brain, a cohabitation of short- and long-term actions may be incorporated as an added strength [42,73]. PPF is a standard method to seek short-term memory behavior by applying two identical pulse trains with different pulse intervals [74]. Figure 7a shows the PPF index that is defined as $((I_2 - I_1)/I_1) \times 100$, where $I_1$ is the current achieved by the first pulse train and $I_2$ is the current achieved by the next pulse train. When the pulse interval is short, the second pulse is affected by the first, resulting in a larger current. When the gap is sufficiently long (1 ms), the device forgets the first pulse, resulting in no change in current by the second pulse. In addition, PPD is used to confirm the short-term properties of an ITO/SiN/TaN device [48]. The measurement is conducted by varying pulse intervals between two consecutive pulse trains. The term PPD index is also defined as $((I_2 - I_1)/I_1) \times 100$. As shown in Figure 7b, the current responds by the second pulse decreasing as the interval increases, well mimicking short-term memory. Furthermore, by rehearsing the applied simulation, short-term memory can be convolved into long-term memory at the biological synapse [75]. Thus, a pulse test with varying numbers of pulses is applied to calculate the change in EPSC. The pulse amplitude and width are 2.3 V and 100 s, respectively, while the pulse number ranges from 1 to 20. When the number of pulses is small, as shown in Figure 7c, the current abruptly climbs and falls, which can be implemented as STM characteristics. However, when 20 identical pulses are administered, the read current increases, indicating LTM properties, where STM is changed into LTM through event rehearsal.
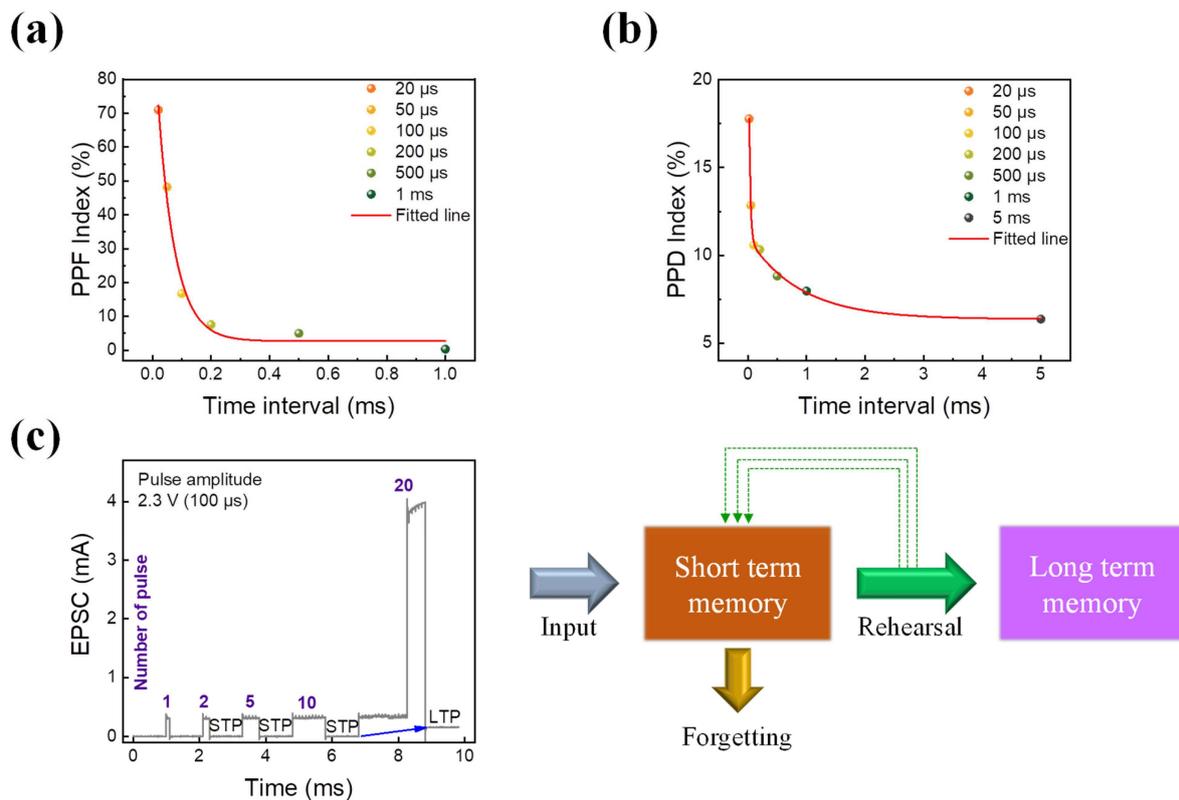
**(a)**



**(b)**



**(c)**



**Figure 7.** (**a**) PPF measurement. (**b**) PPD measurement. (**c**) The transition of STM to LTM of ITO/SiN/TaN device with the change in EPSC.

Hebbian principles are frequently used to assess a device's ability to simulate pre- and post-synaptic neurons and their functions. One of those learning rules is SRDP, which tests the synaptic response under different frequency simulations [76]. To demonstrate the SRDP function, sets of 10 identical pulse trains with different pulse intervals are prepared. The amplitude and width of the pulse are 2.7 V and 10 s, respectively. To obtain SRDP, the interval is varied from 1 μs to 500 μs, as shown in Figure 8a. Figure 8b shows a desirable relationship between pulse interval and conductance. A quick escalation of conductance is found for short pulse intervals, whereas the conductance update is smaller for larger pulse intervals. Furthermore, synaptic functions by altering pulse amplitude are also tested. As depicted in Figure 8c, a fixed pulse interval and width of 50 μs and 10 μs are applied to observe the conductance change. The varied amplitude of the pulse ranges from 2.6 V to 4.1 V. Figure 8d shows the linear relationship between pulse amplitude and conductance. Rapid conductance changes are observed for large pulse amplitudes, similar to the SRDP result. In the event of a small pulse amplitude, however, no significant variation is observed.

In addition to mimicking the function of the biological synapse, duplicating its physical form can bring value to the realization of an efficient neuromorphic system [72]. As shown in Figure 9a, the structure of a biological synapse is located between the post- and pre-synapse. The synaptic information from the pre-synapse migrates toward the post-synapse receptor, which passes the information to the post-synapse. RRAM, for example, has a simple two-terminal structure that can easily mimic a biological synapse, where the top electrode imitates the pre-synapse, and the bottom electrode imitates the post-synapse. The synaptic information can be changed by the formation of a conducting filament. On the other hand, the memristor conductance is regarded as synaptic weight. Another Hebbian rule known as STDP is investigated to efficiently replicate the biological structure and synaptic weight change of the top and bottom electrodes [77,78]. In the STDP, pulse trains of the same components are fired at both the pre-and post-synapse with a time difference.

The time difference between synapses decides whether the device experiences LTP or LTD. The time difference ($\Delta t$) between post- and pre-synapses is defined as Equation (1):

$$\Delta t = t_{post} - t_{pre} \tag{1}$$

where $t_{post}$ and $t_{pre}$ are the times when pulses are applied to the pre- and post-synapses, respectively. When the pre-synapse exceeds the post-synapse ($\Delta t > 0$), effective positive set pulse trains are applied, resulting in a decrease in resistance, and LTP occurs. On the other hand, when the post-synapse exceeds the pre-synapse ($\Delta t < 0$), effective negative reset pulse trains are applied, increasing resistance, and LTD occurs. The result of applying a pair of pulse trains is illustrated in Figure 9b, where the synaptic weight ($\Delta W$) is defined as Equation (2):

$$\Delta W = \frac{G_f - G_i}{G_i} \times 100(\%) \tag{2}$$

where $G_f$ and $G_i$ are the conductance values of the device after and before applying a pair of pulses, respectively. As revealed in the results, the synaptic weight is greatest when the time gap between the pre- and post-synapse is smallest and the synaptic weight decreases as the time difference is large, replicating the STDP behavior.
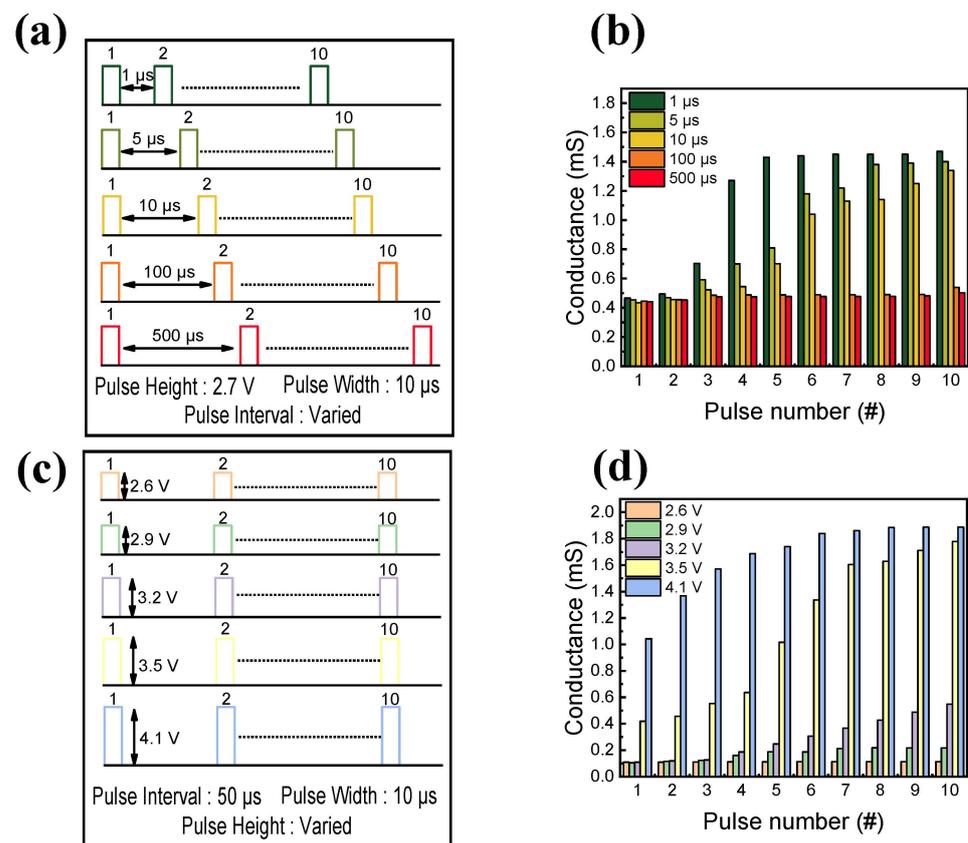


**Figure 8.** (**a**) Schematic illustration of the designed pulse scheme for the demonstration of the SRDP function. (**b**) Conductance response of the SRDP function. (**c**) Schematic illustration of the designed pulse scheme for the demonstration of spike-amplitude-dependent synaptic behavior. (**d**) The conductance response of spike-amplitude-dependent synaptic function.
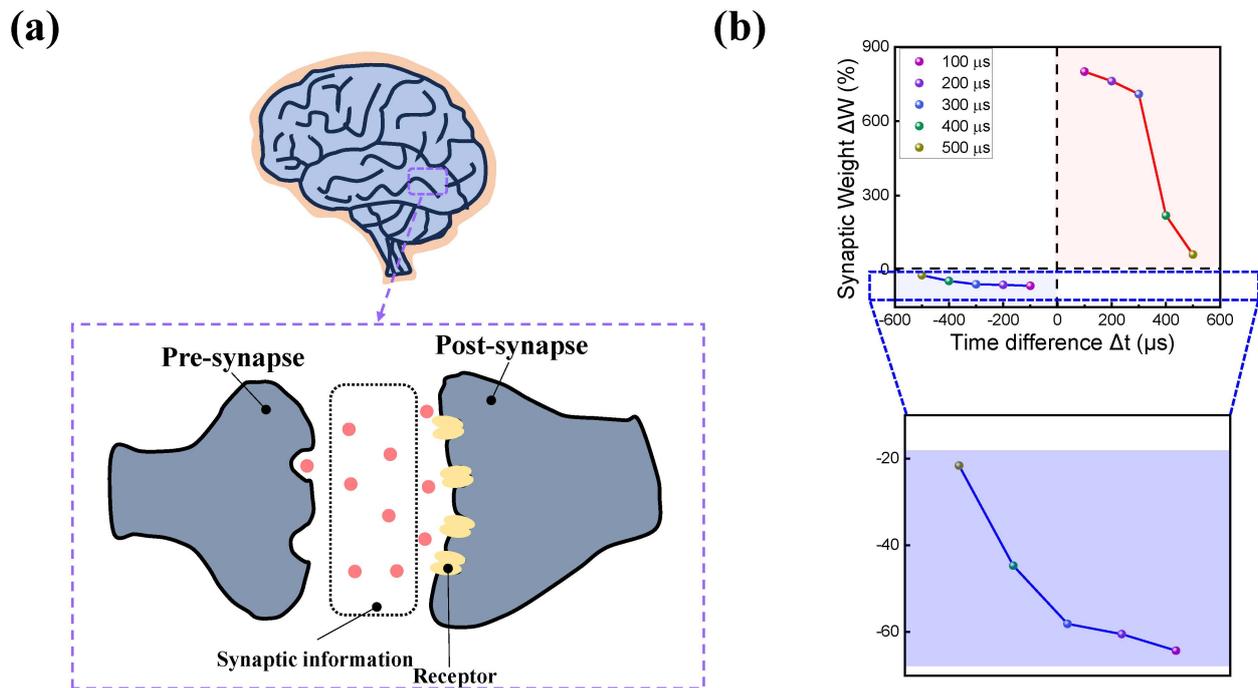
**Figure 9.** (**a**) Schematic illustration of the biological brain's pre- and post-synapse. (**b**) Synaptic weight as a function of the time difference between two pulse trains.

## 4. Conclusions

In summary, we fabricated a SiN-based memristor to investigate the resistive switching characteristics and synaptic functions. The nitride-based resistive switching shows uniform resistive switching for $10^3$ s with a large on/off window. The MLC characteristics are obtained by varying the reset voltage and compliance current, which enlarge the data storage of the device. The coexistence of STM and LTM is found during the pulse scheme, whereby PPF, PPD, and EPSC are demonstrated to emulate bio-inspired nerve systems. Finally, we demonstrate that the ITO/SiN/TaN device could mimic the human brain's Hebbian rules.

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