nanomaterials

MDPI

Article

Enhancing Charge Trapping Performance of Hafnia Thin Films Using Sequential Plasma Atomic Layer Deposition

So-Won Kim [1,†], Jae-Hoon Yoo [1,†], Won-Ji Park [1], Chan-Hee Lee [1], Joung-Ho Lee [2], Jong-Hwan Kim [1,3], Sae-Hoon Uhm [3] and Hee-Chul Lee [1,*]

[1] Department of Advanced Materials Engineering, Tech University of Korea, Siheung 15073, Republic of Korea; swkim9193@tukorea.ac.kr (S.-W.K.); pullat@tukorea.ac.kr (J.-H.Y.); wonji1221@tukorea.ac.kr (W.-J.P.); leech5026a6@tukorea.ac.kr (C.-H.L.); rmfladl91@tukorea.ac.kr (J.-H.K.)
[2] Korea Evaluation Institute of Industrial Technology, Seoul 06152, Republic of Korea; plasma@keit.re.kr
[3] EN2CORE Technology Inc., Daejeon 18469, Republic of Korea; shuhm@en2core.com
* Correspondence: eechul@tukorea.ac.kr; Tel.: +82-32-8041-0589
† These authors contributed equally to this work.

Abstract: We aimed to fabricate reliable memory devices using HfO_2, which is gaining attention as a charge-trapping layer material for next-generation NAND flash memory. To this end, a new atomic layer deposition process using sequential remote plasma (RP) and direct plasma (DP) was designed to create charge-trapping memory devices. Subsequently, the operational characteristics of the devices were analyzed based on the thickness ratio of thin films deposited using the sequential RP and DP processes. As the thickness of the initially RP-deposited thin film increased, the memory window and retention also increased, while the interface defect density and leakage current decreased. When the thickness of the RP-deposited thin film was 7 nm, a maximum memory window of 10.1 V was achieved at an operating voltage of ±10 V, and the interface trap density (D_{it}) reached a minimum value of 1.0×10^{12} $eV^{-1}cm^{-2}$. Once the RP-deposited thin film reaches a certain thickness, the ion bombardment effect from DP on the substrate is expected to decrease, improving the $Si/SiO_2/HfO_2$ interface and thereby enhancing device endurance and reliability. This study confirmed that the proposed sequential RP and DP deposition processes could resolve issues related to unstable interface layers, improve device performance, and enhance process throughput.

Keywords: charge-trapping memory; sequential plasma ALD; interface trapping density; memory window; HfO_2; retention

Citation: Kim, S.-W.; Yoo, J.-H.; Park, W.-J.; Lee, C.-H.; Lee, J.-H.; Kim, J.-H.; Uhm, S.-H.; Lee, H.-C. Enhancing Charge Trapping Performance of Hafnia Thin Films Using Sequential Plasma Atomic Layer Deposition. *Nanomaterials* **2024**, *14*, 1686. https://doi.org/10.3390/nano14201686

Academic Editor: Liang Li

Received: 4 October 2024
Revised: 20 October 2024
Accepted: 20 October 2024
Published: 21 October 2024

1. Introduction

With recent advancements in ultra-miniaturization and high integration of semiconductor devices, thin-film technology has become increasingly prominent in enhancing the performance of next-generation memory devices. In particular, memory devices utilizing HfO_2-based materials are gaining significant attention for their performance and stability [1–3]. Compared to other non-volatile memories such as magnetic random-access memory (MRAM), phase-change random-access memory (PCRAM), and ferroelectric random-access memory (FRAM), NAND flash memory has relatively slower speeds and issues with durability. However, it offers significant advantages in terms of memory cost and capacity, making it widely applicable [4,5]. Reducing the thickness of the charge-trapping layer (CTL) helps to further increase the integration density of NAND flash memory devices. Therefore, it is essential to develop materials that can replace the traditional silicon nitride-based CTL [6–8]. HfO_2 is being highlighted as a potential material for CTL in next-generation NAND flash memory owing to its high trap density, large band offset with silicon, and small equivalent oxide thickness (EOT) [9–11]. Currently, atomic layer deposition (ALD) is the most widely used process for forming such ultra-thin films in the order of a few nanometers [12–15].

In previous studies, our research team analyzed the operational characteristics of charge-trapping memory (CTM) devices fabricated by depositing HfO_2 CTL thin films using remote plasma ALD (RPALD) and direct plasma ALD (DPALD). The results indicated that CTM devices utilizing remote plasma (RP)-HfO_2 thin films exhibited superior charge trapping efficiency and device reliability [16]. This was because, although direct plasma (DP)-HfO_2 thin films contained more internal oxygen vacancies than RP-HfO_2 thin films, the deposition of HfO_2 thin films using DP resulted in ion bombardment damage to the Si substrate, leading to the formation of unstable interface layers and degradation of memory characteristics [17–19]. Conversely, the RP deposition method has the advantage of minimizing substrate damage and interface reactions caused by plasma, as it does not directly apply plasma to the substrate. However, RPALD has the drawback of having significantly longer reactant injection and plasma discharge times than DPALD, resulting in reduced throughput [20–22]. Therefore, we propose a new process technology to prevent the degradation of thin-film characteristics due to substrate damage and unstable interface layers, while improving process throughput for the fabrication of highly reliable memory devices.

In this study, we closely analyzed the phenomenon of memory-characteristic degradation due to DP-induced substrate damage and interface reactions. To mitigate the degradation, we deposited HfO_2 thin films through a new ALD process that utilized alternating RP and DP. Initially, a thin film of a certain thickness was formed using RP, followed by further deposition using DP until the target thickness was achieved. Using the deposited HfO_2 thin films, we fabricated CTM devices with a MAHOS ($Au/Al_2O_3/HfO_2/SiO_2/p\text{-}Si$) structure. By electrically characterizing the CTM devices, we investigated the effect of $Si/SiO_2/HfO_2$ interface characteristics on the memory properties of the devices based on the thickness ratio of the RP/DP sequentially deposited thin films.

2. Materials and Methods

In this study, p-type (100) silicon wafers were used as substrates. The substrates were cleaned using RCA cleaning and then immersed in buffered oxide etchant for approximately 30 s to remove the native oxide layer on the surface. For thin-film deposition on the substrate, we used a plasma-enhanced ALD (PEALD, iOV-dx2, iSAC Research, Daejeon, Korea) system. The RP was generated using a separate remote plasma system (RPS, En2ra-RPS, EN2CORE Technology, Daejeon, Korea), which was located in a space separate from the main chamber, whereas the DP was generated by the plasma generator within the PEALD system. For the deposition of HfO_2 thin films, tetrakis (ethylmethylamino) hafnium (TEMAH, iChems, Hwaseong, Korea) was used as the Hf precursor. As shown in Figure 1, each cycle was repeated such that the thickness ratio of the thin films deposited using RP and DP was $x{:}10 - x$ (x = 0–10 nm), forming a single HfO_2 thin film with a total thickness of 10 nm. At this time, the interface layer formed by the interface reaction between the Si and HfO_2 thin films was utilized as a tunneling oxide (TO) layer. During deposition, the process temperature for both RP and DP processes was maintained at 200 °C, and O_2 was used as the reactive gas. On top of the 10 nm HfO_2 thin film, an Al_2O_3 thin film was formed through DPALD as the blocking oxide (BO) layer to fabricate the CTM device. The top electrode was fabricated using the lift-off method to create a 50 nm thick Au electrode, and Au was deposited at room temperature for 3 min via DC magnetron sputtering. Finally, post-deposition annealing was conducted at 400 °C for 20 min in an N_2 atmosphere using a rapid thermal annealing system.

X-ray diffraction (XRD, SmartLab, Rigaku, Tokyo, Japan) was utilized to analyze the crystallinity of the HfO_2 thin films deposited using RP/DP sequential plasma ALD. The chemical bonding states of the $Si/SiO_2/HfO_2$ interface layer were examined using X-ray photoelectron spectroscopy (XPS, AXIS-NOVA, Manchester, UK). Additionally, to analyze the electrical and reliability characteristics of the fabricated MAHOS-structured CTM, measurements and analyses were conducted using a semiconductor parameter analyzer (4200-SCS, Keithley, Cleveland, OH, USA) connected to a microprobe station (APX-6B, WIT Co., Suwon, Korea).

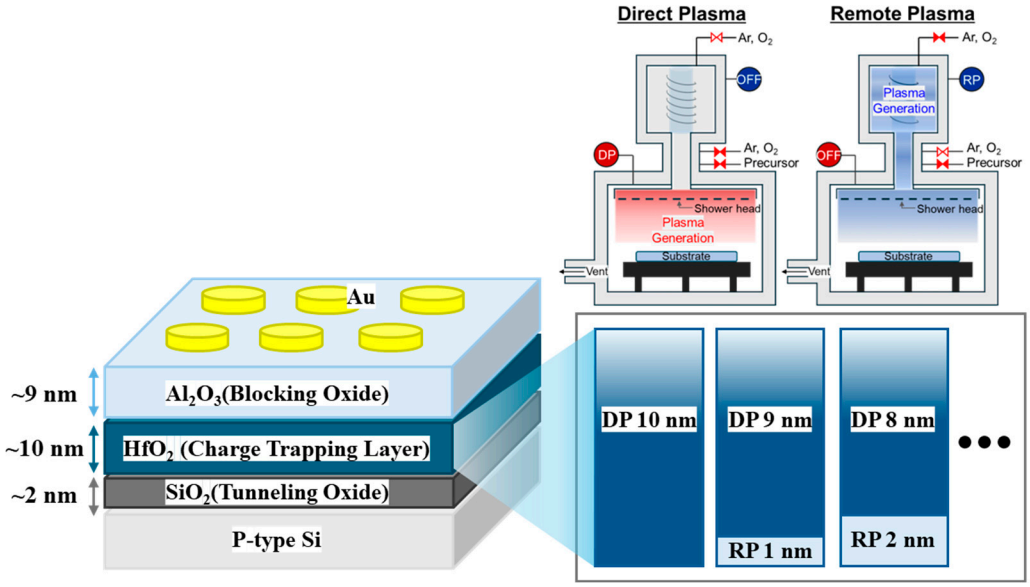

Figure 1. Schematic of the CTM device and equipment deposited using sequential remote plasma (RP) and direct plasma (DP).

3. Results and Discussion

Figure 2 shows the results of XRD pattern analysis of HfO_2 thin films according to the equivalent oxide thickness (EOT) and deposition method based on HfO_2 deposition thickness in a metal-oxide-semiconductor structure. The dielectric constant of the HfO_2 thin films was calculated using Equation (1) based on the measured capacitance values from the C-V accumulation region of the MAHOS samples, in which HfO_2 thin films were deposited using RP and DP, respectively (Figure 2a). Based on these values, the EOT of the HfO_2 thin films was calculated using Equation (2).

$$\kappa_{HfO_2} = \frac{C_{HfO_2} \times t_{HfO_2}}{\varepsilon_0} \quad (1)$$

$$EOT = t_{HfO_2} \frac{\kappa_{SiO_2}}{\kappa_{HfO_2}} \quad (2)$$

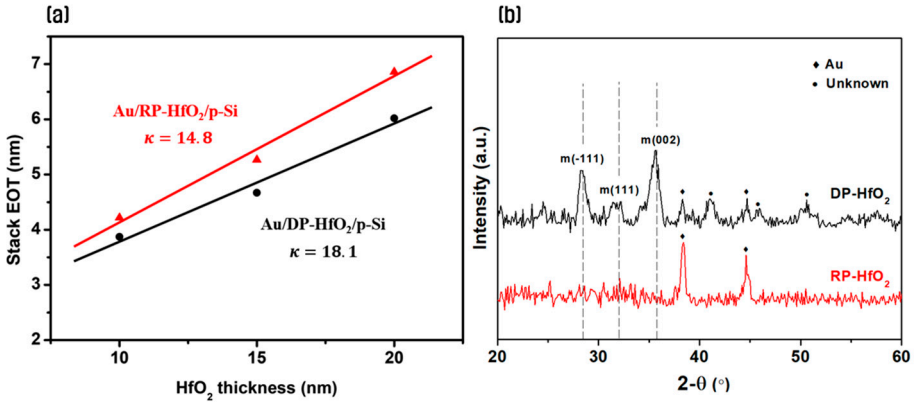

Figure 2. (**a**) Variation of EOT with HfO_2 deposition thickness and (**b**) X-ray diffraction pattern analysis results of DP- and RP-HfO_2 thin films.

Here, κ_{HfO2} represents the dielectric constant of HfO_2, C_{HfO2} is the measured capacitance per unit area, t_{HfO2} is the actual thickness of the HfO_2 thin films, ε_0 is the permittivity of vacuum, and κ_{SiO2} is the dielectric constant of SiO_2 [23,24]. The results indicated that the dielectric constant was lower when using RP (κ = 14.8) compared to DP (κ = 18.1). As

can be observed from the XRD results in Figure 2b, the HfO_2 thin film deposited using RP shows an amorphous state with minimal HfO_2 crystallization, whereas the thin film deposited using DP exhibits monoclinic crystal phases around 28°, 32°, and 36° [25,26]. This suggests that the thin film deposited using DP has a higher dielectric constant due to crystallization than that deposited using RP. Although the HfO_2 thin film deposited using RP shows a larger EOT, it is expected to be advantageous for reducing leakage current and suppressing charge de-trapping phenomena owing to its amorphous state, unlike the thin film deposited using DP [27–30]. Therefore, despite a slight EOT loss, we aimed to investigate the feasibility of leveraging the high-quality interface characteristics and improved electrical properties of high-k HfO_2 thin films for a CTL by controlling the thickness ratio of HfO_2 thin films deposited using the sequential RP and DP deposition processes.

Figure 3 shows the interface trap density for different thickness ratios of thin films deposited using the sequential plasma ALD process (RP/DP). The trap density was calculated using the high-low-frequency capacitance method proposed by Castagne and Vapaille [31]. Figure 3a shows the distribution of interface trap density in the energy region of Si. The surface potential with respect to the gate voltage was obtained using the Berglund integral, and the D_{it} distribution within the Si bandgap was calculated accordingly [32,33]. It was confirmed that as the thickness of the thin film initially deposited with RP increased, the interface trap density per unit area decreased across the energy region. This is attributed to the occurrence of deposition and plasma discharge in one space when deposited using only DP, damaging the substrate and thin film due to ion bombardment and creating an unstable interface layer and defects. The ion bombardment effect at the interface is mitigated when the thin film is initially deposited using RP, decreasing the interface trap density [22,34]. In Figure 3b, the D_{it} value at the midgap (0.56 eV) of the silicon bandgap (1.12 eV) is shown. The D_{it} value decreases to below 1.31×10^{12} $eV^{-1}cm^{-2}$ when the thickness of RP-HfO_2 exceeds 4 nm, which is more than four times lower than the D_{it} value of a 10 nm HfO_2 thin film deposited using only DP. In a previous study, the D_{it} value of the 10 nm HfO_2 thin film deposited only using RP was confirmed to be 1.18×10^{12} $eV^{-1}cm^{-2}$ [16]. Therefore, a saturating trend is observed as the thickness of the RP-HfO_2 film increases, and it is expected that the influence of DP on the interface significantly decreases beyond a film thickness of 4 nm.

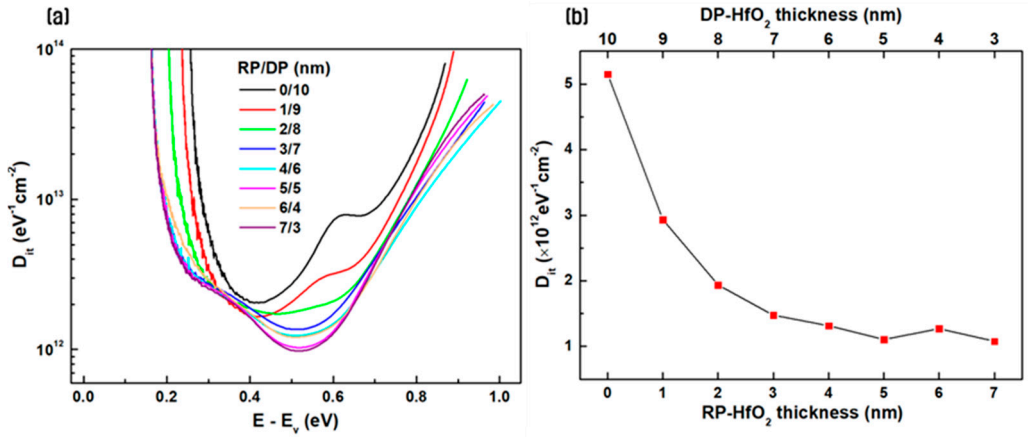

Figure 3. (**a**) Distribution of interface trap density (D_{it}) within the Si bandgap and (**b**) calculated D_{it} values at midgap for different thickness ratios of thin films deposited via the sequential remote plasma (RP) and direct plasma (DP) processes.

Figure 4 compares the C-V measurement results and the size of the memory window for HfO_2 CTM according to the thickness ratio of the thin film layers deposited using the sequential RP and DP processes. The measurements were conducted at 1 MHz using a forward and reverse sweeping method. In the C-V curve shown in Figure 4a, a typical counterclockwise hysteresis caused by the trapping of mobile carriers, such as electrons and

holes, can be observed [35]. The memory window value was calculated from the difference in V_{FB} (flat-band voltage) between the program and erase states in the C-V measurement results, and it is presented in Figure 4b. As the sweeping voltage increases, the thin film initially deposited using RP exhibits a significant increase in the memory window with increasing thickness compared to the thin film deposited solely using DP at a thickness of 10 nm. Additionally, for the device based on the 10 nm HfO_2 thin film deposited only using DP, a memory window of 4.68 V is observed at an operating voltage of ±10 V. However, as the thickness of the thin film initially deposited using RP increases, the memory window gradually increases, reaching a maximum value of 10.1 V at an operating voltage of ±10 V when the RP-deposited thin film is 7 nm thick. As shown in Figure 3, the interface defect density is higher when only DP is used for deposition. The presence of interface defects likely hindered the trapping and de-trapping of charges through TO, and the concentration of traps in specific defect regions may have contributed to the reduced size of the memory window [36–38].

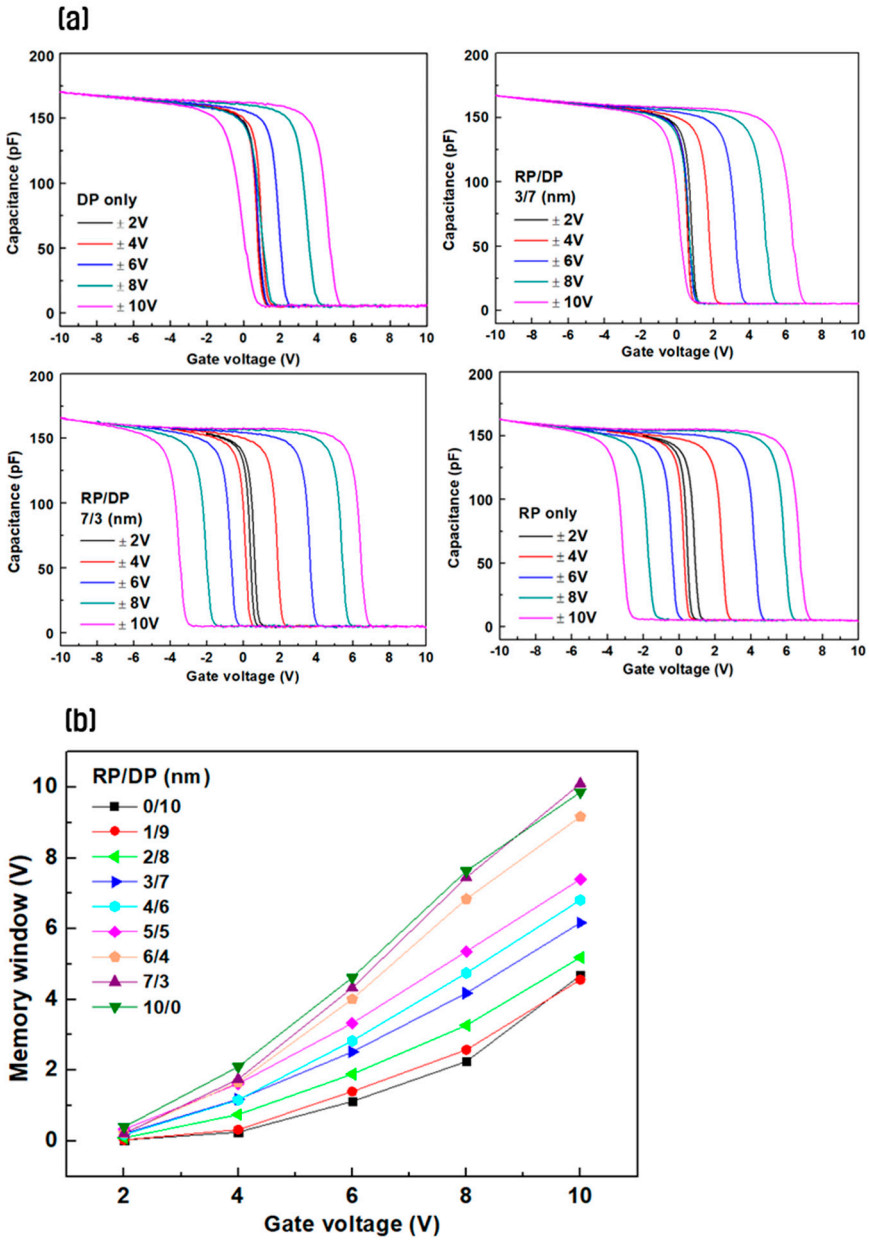

Figure 4. Comparison of (**a**) C-V curves and (**b**) memory window of HfO_2 CTM deposited using the sequential remote plasma and direct plasma processes.

Figure 5a shows the charge density in the thin film according to the thickness ratio of the thin films deposited through the sequential RP and DP processes. The charge trapping density per unit area (N_t) was calculated using the equation $N_t = (C_{ox} \times \Delta V_{FB})/qA$ at the point where the memory window saturated as the sweeping voltage increased. Here, C_{ox} is the capacitance in the accumulation region, ΔV_{FB} is the memory window, q is the electron charge, and A is the effective area of the top electrode [39]. N_t showed a value of 1.6×10^{13} cm^{-2} when the deposition was performed using only DP, and it continuously increased as the thickness of the RP-deposited film increased. When the thickness of the RP-deposited film was 7 nm, N_t reached 3.31×10^{13} cm^{-2}, which is approximately twice the maximum value, indicating excellent charge trapping efficiency. Figure 5b shows the V_{FB} shift results according to the thickness ratio of the thin films deposited through the sequential RP and DP processes. As the thickness of the initially RP-deposited film increased, the V_{FB} shift increased during the reverse sweep, indicating an increase in the number of effective sites within the CTL where charges can be repeatedly trapped and de-trapped [38,40]. Additionally, during the forward sweep, hole trapping gradually increased as the thickness of the RP-deposited film increased up to a thickness of 5 nm and then rapidly increased after x = 6 nm. This result suggests that up to x = 5 nm, the ion bombardment effect from the subsequent DP deposition affected the underlying TO, reducing the hole-trapping efficiency. From x = 6 nm, the ion bombardment effect from DP disappeared, resulting in a V_{FB} shift similar to that of electron trapping. Therefore, it is expected that the Program/Erase (P/E) operation of the device can be smoothly performed when the thickness of the RP-deposited film is higher than or equal to 6 nm.

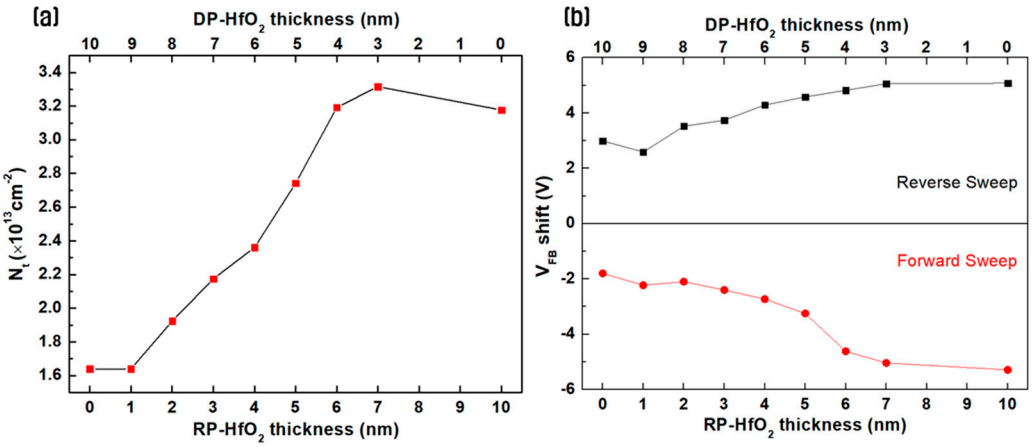

Figure 5. (**a**) Charge density in the thin film and (**b**) V_{FB} shift results of HfO_2 CTM according to the thickness ratio of the thin film layers deposited using the sequential remote plasma and direct plasma processes.

Figure 6 shows the degree of defects at the interface according to the thickness ratio of the thin film layers deposited through the sequential RP and DP processes. To confirm the results, XPS analysis was performed near the $Si/SiO_2/HfO_2$ interface to measure the ratio of the number of lattice bonds to that of non-lattice bonds at the interface. The non-lattice ratio, which indicates oxygen vacancies as one of the defect factors, was 15.3% in the XPS O1s peak spectra when only DP was used. When the thickness ratio of the RP-deposited film was 3 nm and 7 nm, the non-lattice ratio gradually decreased to 14.5% and 11.02%, respectively. The non-lattice ratio was 10.9% when only RP was used for deposition. This result is consistent with previous research findings that reported that the initial deposition of the thin films using RP reduces ion impact damage, thereby decreasing oxygen vacancies near the interface and forming a stable interface [16].

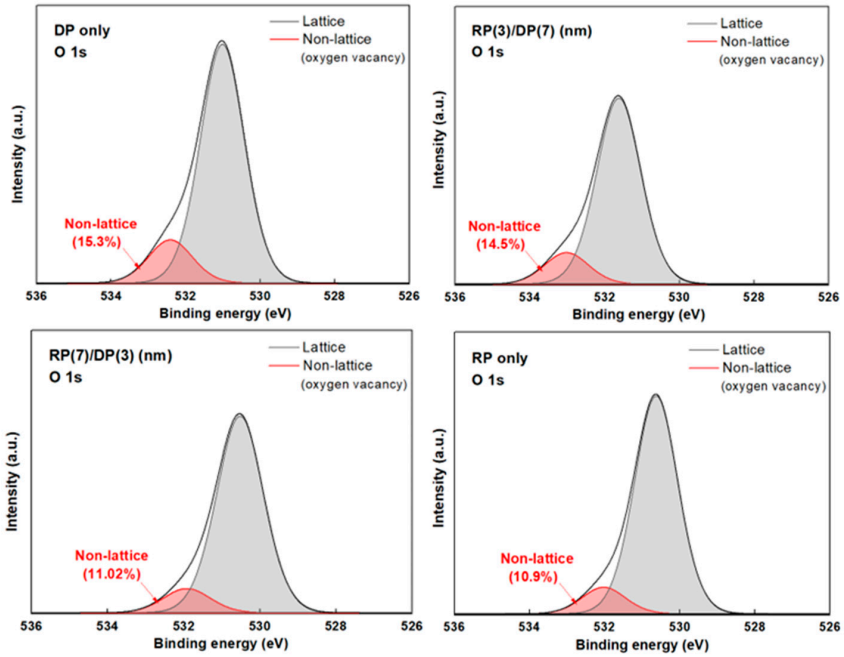

Figure 6. Comparison results of O 1s narrow scan XPS patterns according to the thickness ratio of thin film layers deposited using the sequential remote plasma and direct plasma processes.

Figure 7 shows the evaluation results of V_{FB} shift characteristics according to P/E (Program/Erase) cycling to confirm the extent of device degradation based on the thickness ratio of thin films deposited using the sequential RP and DP processes. The P/E cycling was performed using a pulse train of amplitude and period ±8 V and 10 ms, respectively. For RP-deposited films with a thickness in the range of 0–2 nm, the overall V_{FB} shift was clearly observed to be in the negative direction. Generally, V_{FB} shift degradation is attributed to the failure of de-trapping electrons trapped due to the degradation of the Si/TO interface, TO, and CTL during P/E cycling, leading to a decrease in erase speed at the same gate voltage. This is likely because, during P/E cycling, thinner RP-deposited films result in unstable interface layers with many interface trap charges [31–44]. Therefore, it was confirmed that initially depositing a thin film of a certain thickness using RP, followed by DP deposition, enhances the reliability of the device during actual memory operation cycling.

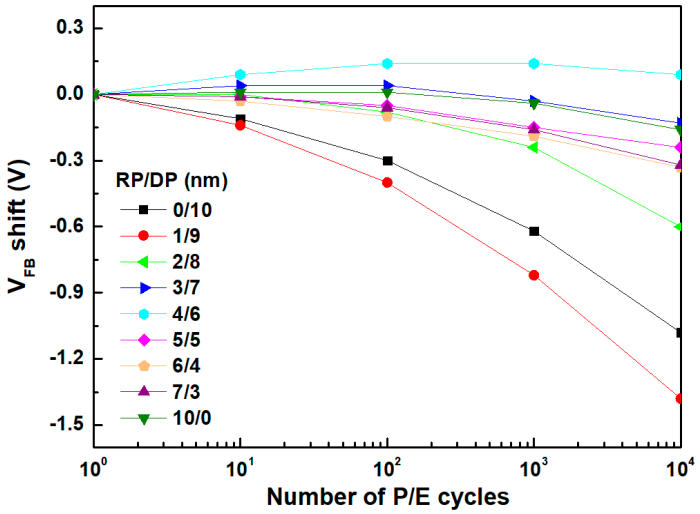

Figure 7. Endurance characteristics measurement results of HfO_2 charge-trapping memory (CTM) deposited using the sequential remote plasma and direct plasma processes.

Figure 8a shows the results of a time-dependent dielectric breakdown (TDDB) test conducted on HfO_2 CTM devices deposited using the sequential RP and DP processes to predict the reliability of the high-k HfO_2 thin film. The measurements were conducted at room temperature, and a high voltage of 5.5 MV/cm was applied to the device to observe changes in leakage current characteristics over time. For thin films deposited with an initial RP thickness of x = 0–4 nm, weak endurance was observed within approximately 10 s. However, beyond x = 5 nm, the endurance time increased, and the initial leakage current gradually decreased as the thickness of the RP-deposited film increased. Generally, defects at the interface concentrate electrical stress, accelerating thin film degradation and affecting stable charge storage and reduction of leakage current [45,46]. Therefore, it was confirmed that when the thickness of thin films initially deposited using RP was 5 nm or more, the ion bombardment effect on the TO was reduced, resulting in decreased interface defect density and increased device endurance, as shown in Figure 3. Figure 8b presents the memory retention characteristics, which were obtained to investigate the memory performance of the fabricated CTM device. A voltage of ±8 V was applied for 1 s, and the memory window was observed over time from 10^0 to 10^3 s to predict the memory characteristics of the device after 10 years [47]. During the 10-year retention period, the memory window of the thin film deposited using the sequential RP and DP processes showed an intermediate value between those of the DP-only and RP-only films. However, the memory window decay rate showed no significant variation with the thickness ratio of the thin film layers. This is believed to be because the degradation of retention characteristics is more influenced by the quality of the TO than by the interface defect density. Therefore, a wide memory window value of 3.8 V was maintained even after 10 years, irrespective of the charge loss, particularly when the thickness ratio of the sequential RP and DP-deposited thin film was RP(7):DP(3) [48,49].

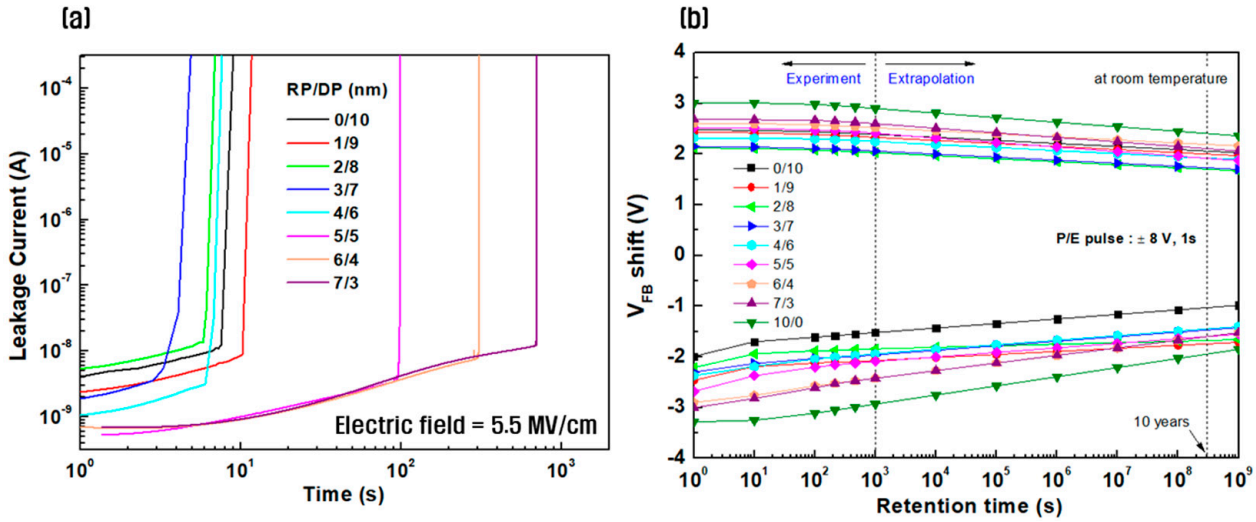

Figure 8. Evaluation results of (**a**) TDDB and (**b**) memory retention characteristics of HfO_2 charge-trapping memory (CTM) deposited using the sequential remote plasma and direct plasma processes.

The results comparing the memory characteristics of the CTM device fabricated in this study with previously published research findings are presented in Table 1. The CTM device produced in this study exhibited superior memory window characteristics, even at lower annealing temperatures and operating voltages, compared to existing CTM device characteristics, indicating significant improvements.

Table 1. Comparison among the memory characteristics of high-k-based CTM devices.

TO/CTL/BO	Thickness (nm)	Annealing temp. (°C)	Operating Voltage (V)	Memory Window (V)	Charge Loss (%)	References
$SiO_X/RP:DP\text{-}HfO_2/Al_2O_3$	2/7:3/9	400	±10	10.1	37	This work
$SiO_X/RP\text{-}HfO_2/Al_2O_3$	2/9/9	400	±12	12.66	34.32	[16]
$SiO_2/HfO_2/Al_2O_3$	3/10/10	1000	±15	7.4	31	[50]
$SiO_2/HfAlO/Al_2O_3$	3/9/8	800	±16	11.5	14.9	[51]
$Al_2O_3/HfAlO/Al_2O_3$	2/9/12	600	±12	6.29	79	[52]
$SiO_2/ZrO_2/Al_2O_3$	5/10/15	700	±11	7.1	16	[53]

4. Conclusions

In this study, a new ALD process that involved the sequential deposition of RP and DP was employed to deposit an HfO_2 CTL. We meticulously investigated the effect of the interface characteristics of $Si/SiO_2/HfO_2$ on the operational characteristics of CTM devices. As the thickness of the initially RP-deposited thin film increased, the memory window increased, and the interface trap density (D_{it}) decreased. Specifically, when the RP-deposited thin film thickness was 7 nm, the memory window reached a maximum value of 10.1 V at an operating voltage of ±10 V, and D_{it} reached a minimum value of 1.0×10^{12} $eV^{-1}cm^{-2}$. XPS analysis results confirmed that the thin film deposited using the sequential RP and DP processes exhibited a lower non-lattice ratio, indicating defects at the $Si/SiO_2/HfO_2$ interface compared to the thin film deposited using only DP. This suggests that using RP reduces interface defects. Additionally, when the RP-deposited thin film thickness was higher than or equal to 5 nm, the device endurance significantly increased, and the V_{FB} shift results also showed improved charge trapping efficiency. This suggests that during DP thin-film deposition, ion bombardment affects the substrate up to approximately 5 nm depth. When the thickness of the RP-deposited thin film was 5 nm or more, the ion bombardment effect of DP on the TO decreased, improving endurance and reliability.

Consequently, the HfO_2 thin film deposited using the sequential RP and DP processes exhibited overall improved electrical characteristics. These results confirm that the sequential plasma deposition process can solve substrate damage and unstable interface layer issues, improving thin film characteristics and enhancing device performance. Moreover, by applying the DP process alternately with the RP process, which has a long process time, the deposition rate increased and the overall process time shortened, confirming the effect of increased throughput. In the future, it is anticipated that this process technology can be applied to various structures to develop memory devices with superior performance and reliability.

Author Contributions: Conceptualization, S.-H.U. and H.-C.L.; methodology, J.-H.Y. and S.-W.K.; software, J.-H.Y.; validation, S.-W.K., J.-H.L., and S.-H.U.; formal analysis, J.-H.Y. and S.-W.K.; investigation, W.-J.P. and C.-H.L.; resources, W.-J.P. and C.-H.L.; data curation, J.-H.Y. and C.-H.L.; writing—original draft preparation, J.-H.Y. and S.-W.K.; writing—review and editing, J.-H.K., J.-H.L., and H.-C.L.; visualization, W.-J.P. and C.-H.L.; supervision, S.-H.U. and H.-C.L.; project administration, H.-C.L.; funding acquisition, J.-H.K. and H.-C.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by EN2CORE Technology, Inc. (R&D project "Application of Remote Plasma Process to Semiconductor Memory Devices"), the Priority Research Centers Program (2017R1A6A1A03015562) through the National Research Foundation (NRF) of Korea funded by the Ministry of Education, and K-CHIPS (Korea Collaborative and High-tech Initiative for Prospective Semiconductor Research) (1415187710, RS-2023-00237030, 23027-15FC) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea).

Data Availability Statement: The data presented in this study are contained within the article.

Conflicts of Interest: Authors Jong-Hwan Kim and Sae-Hoon Uhm were employed by the company EN2CORE Technology Inc. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Böscke, T.S.; Müller, J.; Bräuhaus, D.; Schröder, U.; Böttger, U. Ferroelectricity in Hafnium Oxide Thin Films. *Appl. Phys. Lett.* **2011**, *99*, 102903. [CrossRef]
2. Park, M.H.; Lee, Y.H.; Mikolajick, T.; Schroeder, U.; Hwang, C.S. Review and Perspective on Ferroelectric HfO_2-Based Thin Films for Memory Applications. *MRS Commun.* **2018**, *8*, 795–808. [CrossRef]
3. Liao, J.; Dai, S.; Peng, R.C.; Yang, J.; Zeng, B.; Liao, M.; Zhou, Y. HfO_2-Based Ferroelectric Thin Film and Memory Device Applications in the Post-Moore Era: A Review. *Fundam. Res.* **2023**, *3*, 332–345. [CrossRef]
4. Han, S.T.; Zhou, Y.; Roy, V.A.L. Towards the Development of Flexible Non-Volatile Memories. *Adv. Mater.* **2013**, *25*, 5425–5449. [CrossRef] [PubMed]
5. Ni, Y.; Wang, Y.; Xu, W. Recent Process of Flexible Transistor-Structured Memory. *Small* **2021**, *17*, 1–23. [CrossRef] [PubMed]
6. Kim, D.H.; Cho, S.; Li, D.H.; Yun, J.G.; Lee, J.H.; Lee, G.S.; Kim, Y.; Shim, W.B.; Park, S.H.; Kim, W.; et al. Program/Erase Model of Nitride-Based NAND-Type Charge Trap Flash Memories. *Jpn. J. Appl. Phys.* **2010**, *49*, 084301. [CrossRef]
7. Choi, B.; Lee, J.; Yoon, J.; Jeon, M.; Lee, Y.; Han, J.; Lee, J.; Park, J.; Kim, Y.; Kim, D.M.; et al. Effect of Charge Trap Layer Thickness on the Charge Spreading Behavior within a Few Seconds in 3D Charge Trap Flash Memory. *Semicond. Sci. Technol.* **2018**, *33*, 1–5. [CrossRef]
8. Lee, G.H.; Hwang, S.; Yu, J.; Kim, H. Architecture and Process Integration Overview of 3d Nand Flash Technologies. *Appl. Sci.* **2021**, *11*, 6703. [CrossRef]
9. You, H.W.; Cho, W.J. Charge Trapping Properties of the HfO_2 Layer with Various Thicknesses for Charge Trap Flash Memory Applications. *Appl. Phys. Lett.* **2010**, *96*, 94–97. [CrossRef]
10. Zhang, Y.; Shao, Y.Y.; Lu, X.B.; Zeng, M.; Zhang, Z.; Gao, X.S.; Zhang, X.J.; Liu, J.M.; Dai, J.Y. Defect States and Charge Trapping Characteristics of HfO_2 Films for High Performance Nonvolatile Memory Applications. *Appl. Phys. Lett.* **2014**, *105*, 172902. [CrossRef]
11. Wang, J.; Bi, J.; Xu, Y.; Niu, G.; Liu, M.; Stempitsky, V. Effects of Charge Trapping on Memory Characteristics for HfO_2-Based Ferroelectric Field Effect Transistors. *Nanomaterials* **2023**, *13*, 638. [CrossRef]
12. Profijt, H.B.; Potts, S.E.; van de Sanden, M.C.M.; Kessels, W.M.M. Plasma-Assisted Atomic Layer Deposition: Basics, Opportunities, and Challenges. *J. Vac. Sci. Technol. A Vac. Surf. Film.* **2011**, *29*, 050801. [CrossRef]
13. Knoops, H.C.M.; Faraz, T.; Arts, K.; Kessels, W.M.M. (Erwin) Status and Prospects of Plasma-Assisted Atomic Layer Deposition. *J. Vac. Sci. Technol. A Vac. Surf. Film.* **2019**, *37*, 030902. [CrossRef]
14. Lee, H.R.; Beom, K.W.; Kim, M.J.; Yoon, T.S. Post-annealing temperature-dependent electrical properties of thin-film transistors with ZnO channel and HfO_x gate insulator deposited by atomic layer deposition. *Semicond. Sci. Technol.* **2020**, *35*, 075013. [CrossRef]
15. Han, J.; Jeong, B.; Sahu, D.P.; Kim, H.M.; Yoon, T.S. Non-Volatile Charge-Trap Memory Characteristics with Low-Temperature Atomic Layer Deposited HfO_{2-x} Charge-Trap Layer and Interfacial Tunneling Oxide Formed by UV/Ozone Treatment. *J. Alloys Compd.* **2023**, *951*, 169858. [CrossRef]
16. Yoo, J.H.; Park, W.J.; Kim, S.W.; Lee, G.R.; Kim, J.H.; Lee, J.H.; Uhm, S.H.; Lee, H.C. Preparation of Remote Plasma Atomic Layer-Deposited HfO_2 Thin Films with High Charge Trapping Densities and Their Application in Nonvolatile Memory Devices. *Nanomaterials* **2023**, *13*, 1785. [CrossRef] [PubMed]
17. Profijt, H.B.; Kessels, W.M.M. Ion Bombardment during Plasma-Assisted Atomic Layer Deposition. *ECS Trans.* **2012**, *50*, 23–34. [CrossRef]
18. Oh, I.K.; Yoo, G.; Yoon, C.M.; Kim, T.H.; Yeom, G.Y.; Kim, K.; Lee, Z.; Jung, H.; Lee, C.W.; Kim, H.; et al. Very High Frequency Plasma Reactant for Atomic Layer Deposition. *Appl. Surf. Sci.* **2016**, *387*, 109–117. [CrossRef]
19. Kim, K.; Oh, I.K.; Kim, H.; Lee, Z. Atomic-Scale Characterization of Plasma-Induced Damage in Plasma-Enhanced Atomic Layer Deposition. *Appl. Surf. Sci.* **2017**, *425*, 781–787. [CrossRef]
20. Yuan, G.; Li, H.; Shan, B.; Liu, J. Critical Atomic-Level Processing Technologies: Remote Plasma-Enhanced Atomic Layer Deposition and Atomic Layer Etching. *Micro Nanosyst.* **2018**, *10*, 76–83. [CrossRef]
21. Cho, H.; Lee, N.; Choi, H.; Park, H.; Jung, C.; Song, S.; Yuk, H.; Kim, Y.; Kim, J.W.; Kim, K.; et al. Remote Plasma Atomic Layer Deposition of SiNx Using Cyclosilazane and H_2/N_2 Plasma. *Appl. Sci.* **2019**, *9*, 3531. [CrossRef]
22. Khosla, R.; Schwarz, D.; Funk, H.S.; Guguieva, K.; Schulze, J. High-Quality Remote Plasma Enhanced Atomic Layer Deposition of Aluminum Oxide Thin Films for Nanoelectronics Applications. *Solid. State. Electron.* **2021**, *185*, 108027. [CrossRef]
23. Kim, H.K.; Yu, I.H.; Lee, J.H.; Park, T.J.; Seong Hwang, C. Scaling of Equivalent Oxide Thickness of Atomic Layer Deposited HfO_2 Film Using RuO_2 Electrodes Suppressing the Dielectric Dead-Layer Effect. *Appl. Phys. Lett.* **2012**, *101*, 1–6. [CrossRef]
24. Cheng, Y.L.; Hsieh, C.Y.; Chang, Y.L. Deposition Cycle of Atomic Layer Deposition HfO_2 Film: Effects on Electrical Performance and Reliability. *Thin Solid Films* **2013**, *528*, 77–81. [CrossRef]

25. Hackley, J.C.; Gougousi, T. Properties of Atomic Layer Deposited HfO_2 Thin Films. *Thin Solid Films* **2009**, *517*, 6576–6583. [CrossRef]
26. Li, S.; Zhang, Y.; Yang, D.; Yang, W.; Chen, X.; Zhao, H.; Hou, J.; Yang, P. Structure and Optical Properties of HfO_2 Films on Si (100) Substrates Prepared by ALD at Different Temperatures. *Phys. B Condens. Matter* **2020**, *584*, 412065. [CrossRef]
27. Jung, J.S.; Kwon, J.Y.; Xianyu, W.; Noguchi, T.; Jeong, S.H.; Jeong, S.W.; Roh, Y.; Noguchi, T. Study of HfO_2 High-k Gate Oxide for Low-Temperature Poly-Si TFT. *J. Korean Phys. Soc.* **2006**, *48*, 32–34.
28. Migita, S.; Morita, Y.; Mizubayashi, W.; Ota, H. Preparation of Epitaxial HfO_2 Film (EOT = 0.5 nm) on Si Substrate Using Atomic-Layer Deposition of Amorphous Film and Rapid Thermal Crystallization (RTC) in an Abrupt Temperature Gradient. In Proceedings of the 2010 International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; pp. 269–272. [CrossRef]
29. Mannequin, C.; Gonon, P.; Vallée, C.; Latu-Romain, L.; Bsiesy, A.; Grampeix, H.; Salaün, A.; Jousseaume, V. Stress-Induced Leakage Current and Trap Generation in HfO_2 Thin Films. *J. Appl. Phys.* **2012**, *112*, 074103. [CrossRef]
30. Cheema, S.S.; Shanker, N.; Wang, L.C.; Hsu, C.H.; Hsu, S.L.; Liao, Y.H.; San Jose, M.; Gomez, J.; Chakraborty, W.; Li, W.; et al. Ultrathin Ferroic HfO_2–ZrO_2 Superlattice Gate Stack for Advanced Transistors. *Nature* **2022**, *604*, 65–71. [CrossRef]
31. Engel-Herbert, R.; Hwang, Y.; Stemmer, S. Comparison of Methods to Quantify Interface Trap Densities at Dielectric/III-V Semiconductor Interfaces. *J. Appl. Phys.* **2010**, *108*, 124101. [CrossRef]
32. Del Prado, A.; San Andrés, E.; Mártil, I.; González-Díaz, G.; Kliefoth, K.; Füssel, W. Annealing Effects on the Interface and Insulator Properties of Plasma-Deposited Al/$SiO_xN_yH_z$/Si Devices. *Semicond. Sci. Technol.* **2004**, *19*, 133–141. [CrossRef]
33. Lee, W.; Oh, J.; Hwan, J.; Choi, S.; Kang, T.; Chu, H.; Kim, H. Comparative Study of C-V-Based Extraction Methods of Interface State Density for a Low-Temperature Polysilicon Thin Film. *Mater. Res. Express* **2021**, *8*, 085902. [CrossRef]
34. Gong, N.; Ma, T.P. A Study of Endurance Issues in HfO_2-Based Ferroelectric Field Effect Transistors: Charge Trapping and Trap Generation. *IEEE Electron. Device Lett.* **2018**, *39*, 15–18. [CrossRef]
35. Gong, C.; Yin, Q.; Ou, X.; Lan, X.; Liu, J.; Sun, C.; Wang, L.; Lu, W.; Yin, J.; Xu, B.; et al. The Dominant Factors Affecting the Memory Characteristics of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ High-k Charge-Trapping Devices. *Appl. Phys. Lett.* **2014**, *105*, 3–8. [CrossRef]
36. An, H.M.; Kim, H.D.; Kim, T.G. Analysis of the Energy Distribution of Interface Traps Related to Tunnel Oxide Degradation Using Charge Pumping Techniques for 3D NAND Flash Applications. *Mater. Res. Bull.* **2013**, *48*, 5084–5087. [CrossRef]
37. Lan, X.; Ou, X.; Cao, Y.; Tang, S.; Gong, C.; Xu, B.; Xia, Y.; Yin, J.; Li, A.; Yan, F.; et al. The Effect of Thermal Treatment Induced Inter-Diffusion at the Interfaces on the Charge Trapping Performance of HfO_2/Al_2O_3 Nanolaminate-Based Memory Devices. *J. Appl. Phys.* **2013**, *114*, 044104. [CrossRef]
38. Spassov, D.; Paskaleva, A. Challenges to Optimize Charge Trapping Non-Volatile Flash Memory Cells: A Case Study of HfO_2/Al_2O_3 Nanolaminated Stacks. *Nanomaterials* **2023**, *13*, 2456. [CrossRef]
39. Ding, P.; Yang, Y.; Wang, Y.; Liu, C.; Yin, J.; Xia, Y.; Li, A.; Liu, Z. Band-Alignment Dominated Retention Behaviors in High-k Composite Charge-Trapping Memory Devices. *Appl. Phys. Lett.* **2019**, *114*, 053506. [CrossRef]
40. Martínez-Puente, M.A.; Horley, P.; Aguirre-Tostado, F.S.; López-Medina, J.; Borbón-Nuñez, H.A.; Tiznado, H.; Susarrey-Arce, A.; Martínez-Guerra, E. ALD and PEALD Deposition of HfO_2 and Its Effects on the Nature of Oxygen Vacancies. *Mater. Sci. Eng. B* **2022**, *285*, 115964. [CrossRef]
41. Kim, S.; Woo, S.; Kim, H.; Kim, I.; Lee, K.; Jeong, W.; Park, T.; Jeon, H. Atomic Layer Deposition of HfO_2 Thin Films on Ultrathin SiO_2 Formed by Remote Plasma Oxidation. *J. Korean Phys. Soc.* **2008**, *52*, 1103–1108. [CrossRef]
42. Arreghini, A.; Zahid, M.B.; Van Den Bosch, G.; Suhane, A.; Breuil, L.; Cacciato, A.; Van Houdt, J. Effect of High Temperature Annealing on Tunnel Oxide Properties in TANOS Devices. *Microelectron. Eng.* **2011**, *88*, 1155–1158. [CrossRef]
43. Lun, Z.; Wang, T.; Zeng, L.; Zhao, K.; Liu, X.; Wang, Y.; Kang, J.; Du, G. Simulation on Endurance Characteristic of Charge Trapping Memory. In Proceedings of the 2013 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Glasgow, UK, 3–5 September 2013; Volume 2, pp. 292–295. [CrossRef]
44. Tang, Z.; Zhu, X.; Xu, H.; Xia, Y.; Yin, J.; Liu, Z.; Li, A.; Yan, F. Impact of the Interfaces in the Charge Trap Layer on the Storage Characteristics of ZrO_2/Al_2O_3 Nanolaminate-Based Charge Trap Flash Memory Cells. *Mater. Lett.* **2013**, *92*, 21–24. [CrossRef]
45. Zhao, C.; Zhao, C.Z.; Taylor, S.; Chalker, P.R. Review on Non-Volatile Memory with High-k Dielectrics: Flash for Generation beyond 32 nm. *Materials* **2014**, *7*, 5117–5145. [CrossRef]
46. Hou, Z.Z.; Wang, G.L.; Xiang, J.J.; Yao, J.X.; Wu, Z.H.; Zhang, Q.Z.; Yin, H.X. Improved Operation Characteristics for Nonvolatile Charge-Trapping Memory Capacitors with High-k Dielectrics and SiGe Epitaxial Substrates. *Chin. Phys. Lett.* **2017**, *34*, 097304. [CrossRef]
47. Nedoseka, A. Diagnostics and Prediction of the Residual Life of Welded Structures. *Fundam. Eval. Diagn. Welded Struct.* **2012**, e322–e372. [CrossRef]
48. Khera, E.A.; Mahata, C.; Imran, M.; Niaz, N.A.; Hussain, F.; Khalil, R.M.A.; Rasheed, U.; SungjunKim, N. Improved Resistive Switching Characteristics of a Multi-Stacked $HfO_2/Al_2O_3/HfO_2$ RRAM Structure for Neuromorphic and Synaptic Applications: Experimental and Computational Study. *RSC Adv.* **2022**, *12*, 11649–11656. [CrossRef]
49. Spassov, D.; Paskaleva, A.; Guziewicz, E.; Wozniak, W.; Stanchev, T.; Ivanov, T.; Wojewoda-Budka, J.; Janusz-Skuza, M. Charge Storage and Reliability Characteristics of Nonvolatile Memory Capacitors with HfO_2/Al_2O_3-Based Charge Trapping Layers. *Materials* **2022**, *15*, 6285. [CrossRef]

50. Maikap, S.; Lee, H.Y.; Wang, T.Y.; Tzeng, P.J.; Wang, C.C.; Lee, L.S.; Liu, K.C.; Yang, J.R.; Tsai, M.J. Charge Trapping Characteristics of Atomic-Layer-Deposited HfO_2 Films with Al_2O_3 as a Blocking Oxide for High-Density Non-Volatile Memory Device Applications. *Semicond. Sci. Technol.* **2007**, *22*, 884–889. [CrossRef]
51. Yoo, J.; Kim, S.; Jeon, W.; Park, A.; Choi, D.; Choi, B. A Study on the Charge Trapping Characteristics of High-k Laminated Traps. *IEEE Electron. Device Lett.* **2019**, *40*, 1427–1430. [CrossRef]
52. Lan, X.; Gong, C.; Ou, X.; Cao, Y.; Sun, C.; Chen, Y.; Xu, B.; Xia, Y.; Li, A.; Yin, J.; et al. Enhancement of the Charge Trapping Performances with HfAlO Composite Oxide Thin Films in SONOS-Type Nonvolatile Memory. *Microelectron. Eng.* **2015**, *133*, 88–91. [CrossRef]
53. Liu, J.; Wang, Q.; Long, S.; Zhang, M.; Liu, M. A Metal/Al_2O_3/ZrO_2/SiO_2/Si (MAZOS) Structure for High-Performance Non-Volatile Memory Application. *Semicond. Sci. Technol.* **2010**, *25*, 055013. [CrossRef]