Article

Surface Uniformity of Wafer-Scale 4H-SiC Epitaxial Layers Grown under Various Epitaxial Conditions

Siqi Zhao [1,2,†], Jiulong Wang [1,2,†], Guoguo Yan [2,3], Zhanwei Shen [2,3], Wanshun Zhao [2], Lei Wang [2] and Xingfang Liu [1,2,3,*]

1 College of Materials Science and Opto-Electronic Technology, University of Chinese Academy of Sciences, Beijing 100049, China; zhaosiqi@semi.ac.cn (S.Z.); wangjiulong19@semi.ac.cn (J.W.)
2 Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China; ggyan@semi.ac.cn (G.Y.); zwshen@semi.ac.cn (Z.S.); zwshuke@semi.ac.cn (W.Z.); wangl@semi.ac.cn (L.W.)
3 Beijing Key Laboratory of Low Dimensional Semiconductor Materials and Devices, Beijing 100083, China
* Correspondence: liuxf@semi.ac.cn; Tel.: +86-10-82304231
† These authors contributed equally to this work.

Abstract: Wide band gap semiconductor 4H-SiC is currently widely used in the manufacture of high-frequency and high-voltage power devices. The size of commercial 4H-SiC wafers is increasing, from 4 inches to 6 inches. Surface roughness, as one of the parameters reflecting the quality of epitaxial wafers, is closely related to the performance of power devices. Most studies on the uniformity of epitaxial layers did not focus on RMS; however, the uniformity of epitaxial surface roughness also affects the device yield. In this paper, the root mean square roughness (RMS) and uniformity (σ) of epitaxial wafers are investigated as a function of epitaxy conditions, including C/Si ratio, growth temperature, and Si/H ratio. It was found that the best values of RMS and σ were obtained with C/Si ratio = 1 in the experimental range. Growth temperature had opposite effects on RMS and σ, with better RMS uniformity obtained at lower growth temperatures. An insignificant effect on RMS and σ has been found with the Si/H ratio changes in the experimental range. We hope that our experiments can play a certain role in promoting the improvement of the surface roughness of wafer-scale 4H-SiC epitaxial layers.

Keywords: 4H-SiC; homogeneous epitaxy; LPCVD; uniformity

Citation: Zhao, S.; Wang, J.; Yan, G.; Shen, Z.; Zhao, W.; Wang, L.; Liu, X. Surface Uniformity of Wafer-Scale 4H-SiC Epitaxial Layers Grown under Various Epitaxial Conditions. *Coatings* **2022**, *12*, 597. https://doi.org/10.3390/coatings12050597

Academic Editor: Andrey V. Osipov

Received: 15 March 2022
Accepted: 25 April 2022
Published: 27 April 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

As a third-generation wide-bandgap semiconductor, SiC has good application prospects in high-temperature, high-voltage, and high-power devices [1–3]. SiC has more than 200 poly-type structures, among which 4H-SiC is widely used in the development of microelectronic devices due to its higher electron mobility and higher power conversion efficiency [3–6]. The most widely used growth method for 4H-SiC epitaxial wafers is the chemical vapor deposition (CVD) method [7–9]. Other methods of growing 4H-SiC epitaxial layer include sublimation [8] and molecular beam epitaxy [10]. Among them, the growth temperature required by the sublimation method is higher, which increases the cost of epitaxial growth. Although molecular beam epitaxy can obtain high-quality epitaxial layers at low temperatures, the growth rate is relatively slow. Using the CVD method to grow 4H-SiC not only has good controllability, but also the 4H-SiC epitaxial layer obtained by homoepitaxy has good crystallinity. High-quality homogeneously grown epitaxial wafers without multi-type mixing can be obtained on off-axis substrates by "Step-Controlled Epitaxy" mode using CVD [11–14]. Epitaxial growth at a lower growth pressure can effectively suppress the homogenous products of the gas phase, and the Cl-containing additive can selectively etch the regions with poor surface crystalline quality. Therefore, epitaxial growth is often carried out in a Cl-containing environment or under low pressure, so as to suppress the formation of Si droplets and obtain a higher quality

of the epitaxial layer [15–18]. As the pressure decreases, the step bunching on the epitaxial surface becomes more and more obvious, and the triangular defect density, which is fatal to the device, is reduced. This is believed to be due to the increased surface mobility and diffusion length of adatoms and the decreased epitaxial surface free energy [13,19–21]. When the surface free energy is relatively high, the epitaxial surface tends to minimize the surface free energy by forming defects or steps. The epitaxial surface under low pressure forms step bunching, so the density of triangular defects is reduced. Step bunching has been reported to increase leakage current in Schottky barrier diodes and reduce channel mobility or oxide breakdown characteristics in metal-oxide-semiconductor field-effect transistors [21,22]. The uniformity of the steps on the surface of the wafer-scale epitaxial layer directly affects the yield of the fabricated devices. Therefore, it is very important to improve the uniformity of the surface topography of 4H-SiC wafer-scale epitaxial layers.

With the continuous development of power devices, the large size of 4H-SiC epitaxial wafers has become the main way for manufacturers to reduce costs, improve device productivity and improve device performance [23]. The performance of power devices depends to a large extent on the quality of 4H-SiC epitaxial wafers [24,25], so the homoepitaxial growth of 4H-SiC is critical for the fabrication of 4H-SiC power devices. However, the process parameters of large-size 4H-SiC epitaxial wafers and small-size epitaxial wafers are not exactly the same, which undoubtedly increases the technical difficulty of growing large-size epitaxial wafers. At the same time, as the size of the epitaxial wafer increases, the uniformity of the epitaxial surface is also more difficult to ensure. The uniformity of the wafer-scale epitaxial surface is closely related to the uniformity of the subsequent fabricated device performance. In order to improve the consistency of device performance in industry, it is first necessary to ensure the uniformity of the surface of the epitaxial layer. The surface topography of the 4H-SiC epitaxial layer is affected by several epitaxial parameters, such as temperature, pressure, and C/Si ratio [26–28]. Therefore, by adjusting the epitaxy parameters, wafer-scale 4H-SiC epitaxial layers with high uniformity can be obtained.

The uniformity of wafer-scale 4H-SiC epilayers has been investigated by many groups [14,29–35]. However, in these studies, the study of uniformity does not focus on the RMS of the surface. According to literature surveys, studies on the uniformity of epitaxial surface roughness are rare. On the other hand, as mentioned above, the epitaxial surface quality can affect the performance of the device, so the study of the root mean square roughness (RMS) of 4H-SiC wafers is necessary. In order to study the standard deviation (σ) of RMS, the epitaxial parameters with larger surface roughness were selected for homoepitaxy in this experiment. In this way, the degree of distinction between epitaxial wafers is large enough, which is more conducive to analysis. The sizes of the 4H-SiC wafers in the experiments include 4 inches and 6 inches. On 4-inch wafers, we chose typical five-point measurements to characterize wafer roughness and uniformity. The size of 6-inch wafers is relatively large, which was characterized by radial measurement in many past studies, as the susceptor kept rotating [14,29–31]. Therefore, the radius measurement is adopted for 6-inch wafers in this paper. We chose to use σ to characterize the uniformity of RMS due to the small value of surface roughness RMS.

In this paper, 4H-SiC epitaxial layers were grown on 4° off-angle substrates by low-pressure chemical vapor deposition. Through single-variable experiments, the optimal values of process parameters such as growth temperature, C/Si ratio, and Si/H ratio of large-size 4H-SiC epitaxial wafers were determined, and a high-quality 4H-SiC epitaxial layer with good uniformity was obtained.

2. Materials and Methods

In this experiment, 4H-SiC homoepitaxial experiments were carried out in the home-made vertical hot-wall chemical vapor deposition (CVD) reactor. The substrates were 4-inch and 6-inch commercially available (purchased from SICC Co., Ltd. Shandong, China), n-type 4H-SiC with Si-terminated (0001) faces, with an off-angle of 4° along the (0001) crystal direction. In the epitaxy experiment, SiH_4 (CAS No.7803-62-5) and C_2H_4

(CAS No.74-85-1) were used as Si source and C source, and H_2 (CAS No.1333-74-0) was used as carrier gas and etching gas. H_2 was used for in-situ etching before epitaxial growth. Figure 1 shows the process of homoepitaxial experiments on 4H-SiC wafers. The typical growth pressure is 40 Torr, the growth time is 30 min, and the temperature varies from 1500 °C to 1650 °C. By varying the C/Si ratio, temperature, and Si/H ratio respectively, the effects of different parameters on the step size and uniformity of the 4H-SiC epitaxial surface were investigated. Part of the 4H-SiC wafers obtained by epitaxial growth is shown in Figure 2.

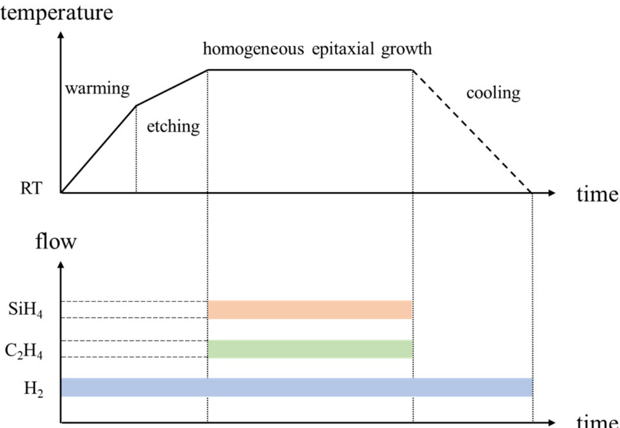

Figure 1. Schematic diagram of the experimental process of 4H-SiC epitaxy.

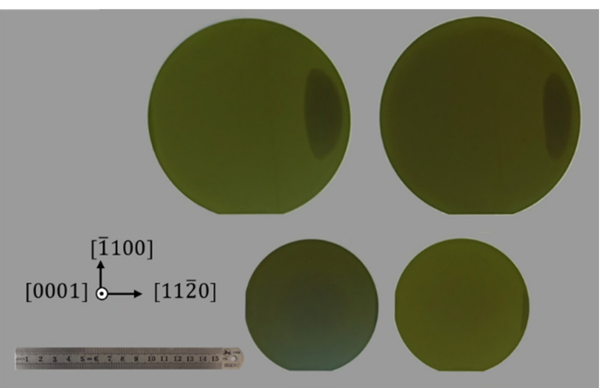

Figure 2. Images of 4H-SiC epitaxial wafer.

The surface topography of the 4H-SiC epitaxial samples was analyzed using an optical microscope. The surface roughness was studied by an atomic force microscope (AFM) in tapping mode.

3. Results and Discussion

The main mode of 4H-SiC epitaxial growth is the "Step-Controlled Epitaxy" mode. After the atoms are adsorbed on the surface, they can migrate to the steps for growth. Therefore, the use of an off-axis substrate can make the 4H-SiC epitaxial layer well replicate the crystal form of the substrate. Due to the minimization of surface energy, topographical defects such as step bunching and triangles are prone to appear on the epitaxial surface when epitaxial growth is performed using the "Step-Controlled Epitaxy" mode. The surface atomic mesa of the 4° off-angle substrate is wider, and several atomic steps on the epitaxial surface may gather together to form a giant step. These surface topographies and defects increase the roughness and surface non-uniformity of the epitaxial layer.

3.1. C/Si Ratio

C/Si ratio and growth temperature are two important parameters affecting the surface steps of 4H-SiC epitaxial layers. Studies have found that the C/Si ratio affects the roughness of the epitaxial surface, and its magnitude determines whether the epitaxial surface is in a silicon-rich or carbon-rich atmosphere. The C/Si ratio affects not only doping [36] but also epitaxial surface topography. In a carbon-rich environment with a large C/Si ratio, the resulting epitaxial surface has more serious step bunching and increased roughness [37,38]. In a silicon-rich atmosphere, a gas-phase homogeneous reaction is likely to occur to generate silicon droplets. In order to study the effect of C/Si ratio on the surface uniformity of 4H-SiC epitaxy, experiments were carried out under the conditions of Si/H = 0.08%, and T = 1650 °C. The RMS measurement points for a single 4-inch wafer are shown in Figure 3. By changing the source gas flow rate to change the C/Si ratio, the RMS and σ of the 4-inch epitaxial wafer surface are obtained as shown in Figure 4. The formula for calculating data uniformity σ is Equation (1):

$$\sigma = \sqrt{\sigma^2} = \sqrt{\frac{\sum_{i=1}^{n}(x_i - \overline{x})^2}{n - 1}} \quad (1)$$

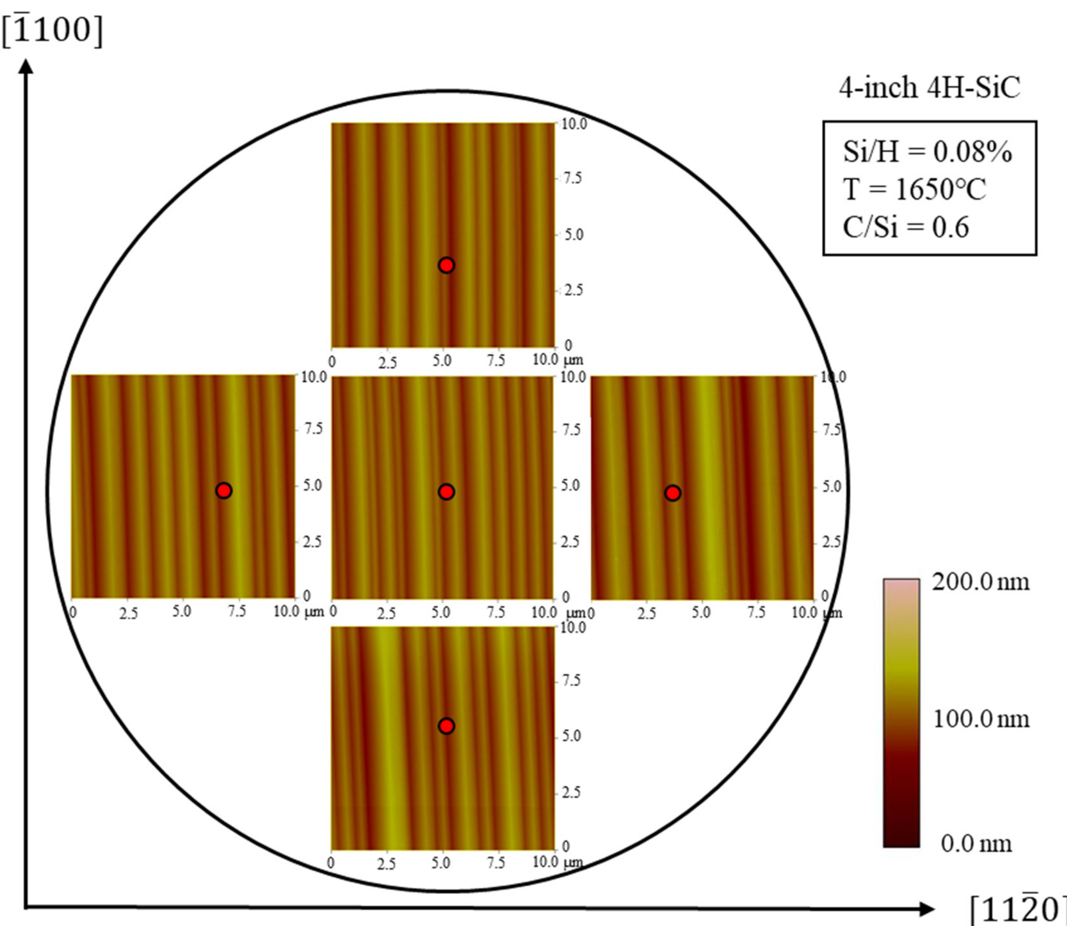

Figure 3. Schematic diagram of RMS measurements of 4H-SiC wafers.

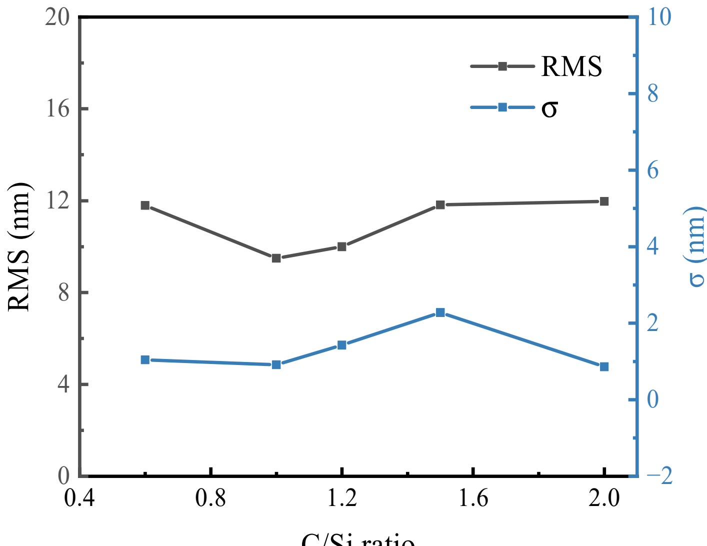

Figure 4. RMS and σ of 4H-SiC epitaxial wafers as a function of C/Si ratio, with C/Si ratios of 0.6, 1.0, 1.2, 1.5, and 2.0, respectively.

As shown in Figure 4, with the increase of C/Si ratio, σ gradually increased and then decreased, and RMS first decreased and then increased. On the whole, with the change of C/Si ratio in the experimental range, the change of RMS is relatively small; the range is only 1.825 nm. In addition, the gradual increase of σ around C/Si = 1.5 indicates that the uniformity in the whole epitaxial wafer is deteriorated. The AFM images of the epitaxial wafers are shown in Figure 5. When the C/Si ratio is small, the overall steps formed are relatively large, and most of the steps have a height of 45–50 nm. Although the roughness is relatively large, the intra-wafer uniformity is good. When C/Si = 1.0, the RMS obtained the minimum value in the experimental range, which proves that C/Si around 1.0 is the most suitable value for epitaxial growth. When the C/Si ratio increases to 1.5, the surface roughness recovered to basically the same magnitude as when C/Si = 0.6. However, the intra-wafer uniformity deteriorated severely, and the step height varies in the range of 35–59 nm. When the C/Si ratio is increased to 2, although the surface uniformity is improved, the epitaxial surface topography is no longer a regular step distribution. During the epitaxial growth process, although the theoretical C/Si ratio is a stable value, it is difficult for the C/Si ratio of the entire 4-inch sample to achieve a uniform distribution on the surface of the epitaxial wafer. Therefore, the step size at different positions fluctuates greatly. The optical microscope image of the epitaxial wafer is shown in Figure 6. The epitaxial surface of 4H-SiC was observed at a magnification of 4200 times, and it was found that, when the C/Si ratio was 0.6 and 1.5, the epitaxial surface was prone to huge steps, while, when the C/Si ratio was 1.0, the epitaxial surface was relatively smooth. Combined with the topography of the epitaxial surface and the variation trend of σ, the C/Si ratio of 1 was selected in the subsequent experiments.

3.2. Growth Temperature

The growth temperature is an important parameter in the epitaxy process. When the temperature increases within a certain range, the step bunching phenomenon will become more and more serious as the temperature increases [12,13]. The step bunching is more serious at higher growth temperature because the migration speed of atoms in the 4H-SiC mesa increases, and the difference between the growth rate of the steps and the mesas becomes larger, thus leading to the enhancement of the step bunching phenomenon [13].

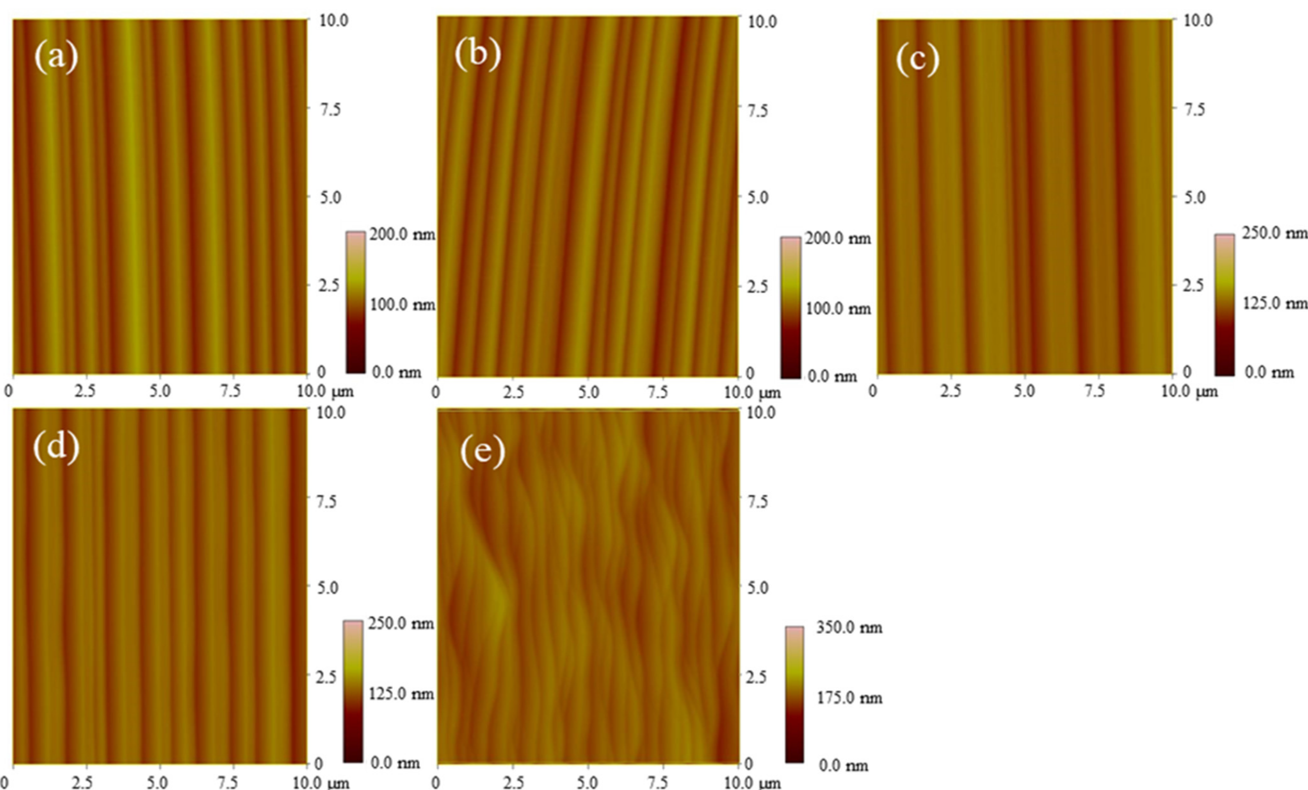

Figure 5. AFM images of 4H-SiC epitaxial wafers with C/Si ratios of (**a**) 0.6, (**b**) 1.0, (**c**) 1.2, (**d**) 1.5, and (**e**) 2.0.

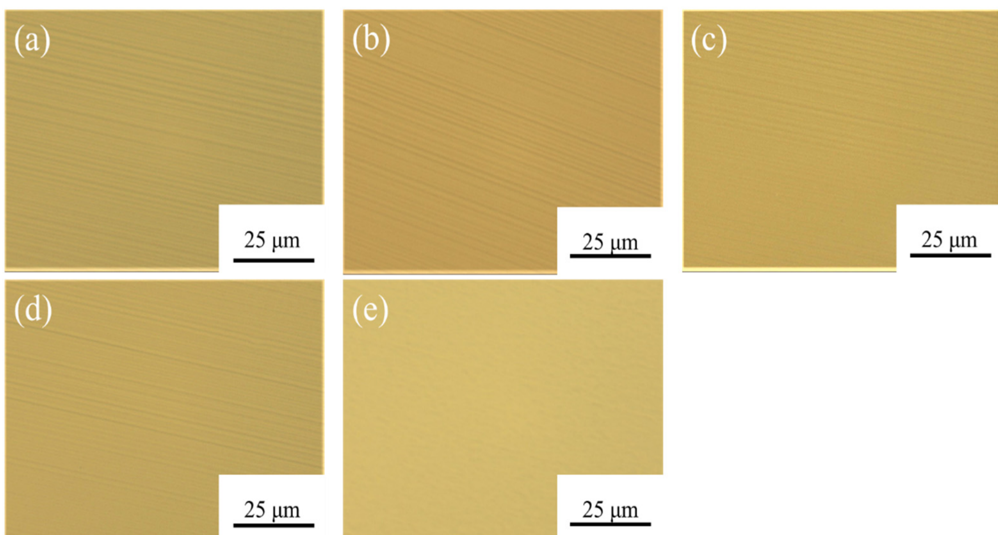

Figure 6. Optical microscope images of 4H-SiC epitaxial wafers with C/Si ratios of (**a**) 0.6, (**b**) 1.0, (**c**) 1.2, (**d**) 1.5, and (**e**) 2.0.

In order to study the effect of growth temperature, experiments were carried out under the condition of C/Si = 1, Si/H = 0.17%. Changing the temperature in the range of 1550 °C–1650 °C, the RMS change of the 4-inch wafers was obtained as shown in Figure 7. The changes of RMS and σ with temperature basically show opposite trends. With the increase of growth temperature, the RMS of the epitaxial surface shows a decreasing trend. As the temperature increases, the step bunching on the epitaxial surface is gradually obvious, and the size of the steps is greatly reduced. The height of the giant steps decreases

from about 60 nm to about 40 nm. In addition to increasing the diffusion length of atoms, increasing the temperature can also reduce the supersaturation degree of the adsorbed phase, which promotes the epitaxial growth of 4H-SiC in step-controlled mode. Although RMS and step size have decreased, σ has been increasing, which means that the intra-wafer uniformity is gradually deteriorating. This may be related to the uneven temperature gradient within the chip after the temperature rises. Local temperature changes can have an effect on the actual C/Si ratio of the surface, which in turn affects the surface topography [15]. Figure 8 is an optical microscope image of 4H-SiC epitaxial wafers as a function of temperature. Figure 9 is a schematic cross-sectional view of the epitaxial wafers along the [112(–)0] direction. It can be seen from the figures that the surface of the epitaxial wafer is somewhat rough and uniform when the temperature is low. The irregular undulations of the surface steps are large. After the temperature increased, step bunching began to appear on the surface, accompanied by the appearance of giant steps. The section curve becomes more regular, forming a smaller and regular distribution of steps. In addition, due to the large Si/H ratio in the experiments, it is believed that the RMS of the obtained surface is large at the growth temperature of less than 1600 °C, which is caused by the insufficient etching effect of hydrogen.

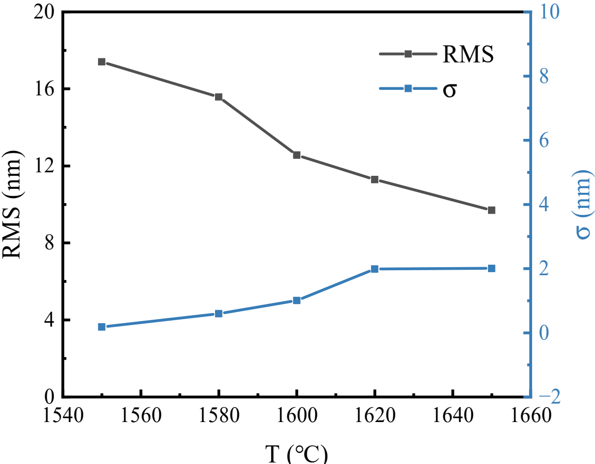

Figure 7. RMS and σ as a function of growth temperature, the growth temperature is 1550, 1580, 1600, 1620, and 1650 °C, respectively.

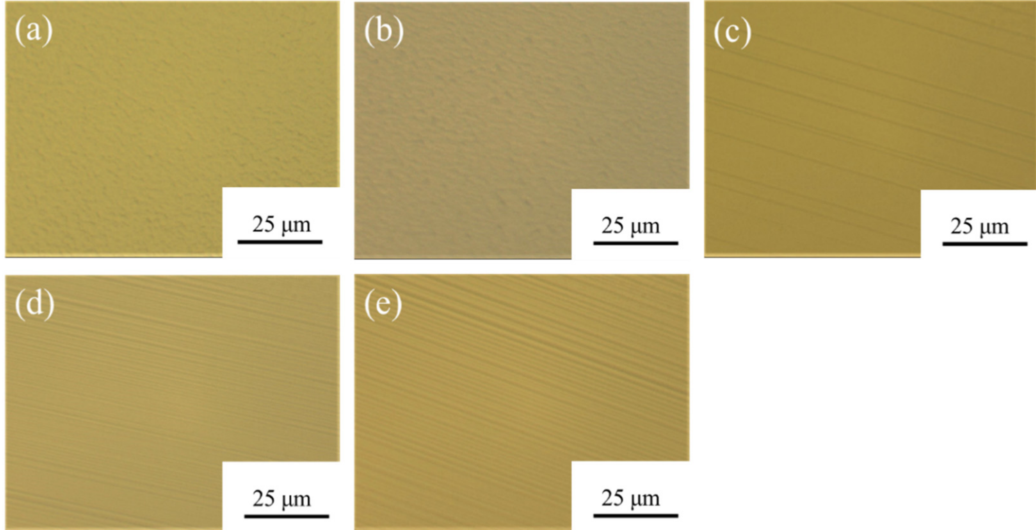

Figure 8. Optical microscope images of 4H-SiC epitaxial wafers with growth temperatures of (**a**) 1550 °C, (**b**) 1580 °C, (**c**) 1600 °C, (**d**) 1620 °C, and (**e**) 1650 °C.

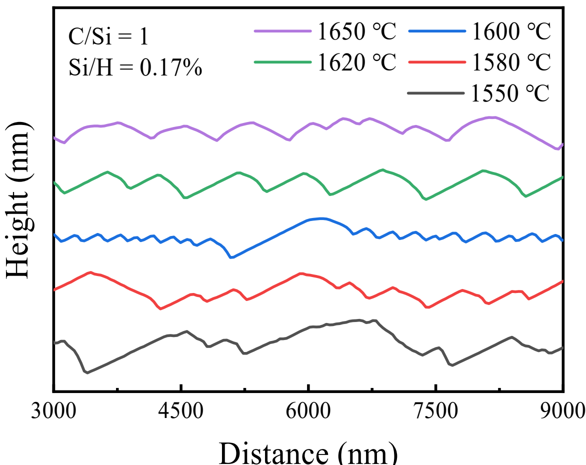

Figure 9. Line analysis of the 4H-SiC epitaxial wafers along the [112(–)0] direction.

3.3. Si/H Ratio

It can be seen from Figure 7 that the epitaxial wafer obtained at 1550 °C has the best uniformity within the experimental range. The experiment was carried out under the condition of C/Si = 1, T = 1550 °C, and the flow ratio of source gas was changed to make the Si/H ratio 0.08%, 0.10%, 0.12%, 0.13%, and 0.15%, respectively. The selection of RMS measurement points for 6-inch wafers is shown in Figure 10, and the results are shown in Table 1. The curves of RMS and σ of 6-inch 4H-SiC epitaxial wafers with Si/H ratio were shown in Figure 11. The value of σ is calculated by Equation (1).

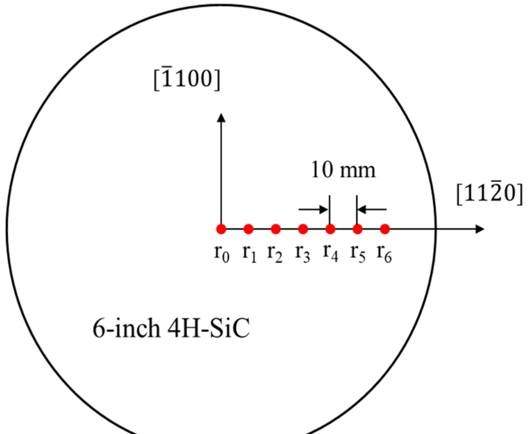

Figure 10. Locations of surface roughness measurements for 6-inch wafers.

Table 1. RMS measurement results of 6-inch 4H-SiC wafers as a function of Si/H ratio.

Samples	r_0 (nm)	r_1 (nm)	r_2 (nm)	r_3 (nm)	r_4 (nm)	r_5 (nm)	r_6 (nm)	σ
Si/H = 0.08%	3.359	3.241	3.022	3.394	3.168	2.949	2.510	0.304
Si/H = 0.10%	3.718	4.031	3.700	3.998	3.804	3.367	3.292	0.285
Si/H = 0.12%	3.76	3.37	3.702	3.535	3.54	3.41	3.02	0.246
Si/H = 0.13%	4.061	4.198	3.963	4.256	4.176	3.800	3.926	0.166
Si/H = 0.15%	3.272	2.84	3.29	3.036	3.138	3.04	2.944	0.165

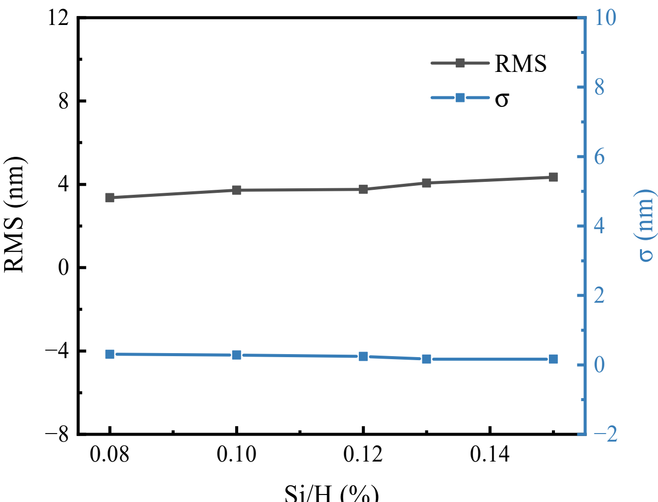

Figure 11. RMS and σ as a function of Si/H ratio, the Si/H ratio is 0.08%, 0.10%, 0.12%, 0.13%, and 0.15%, respectively.

With the increase of Si/H ratio, RMS and σ show increasing and decreasing trends, respectively, but the changes are small. The effect of Si/H ratio on RMS is considered to be related to the etching effect of H_2. When the Si/H ratio is large, a silicon-rich atmosphere is formed, and a gas-phase homogeneous reaction is likely to occur in the gas above the substrate to generate silicon droplets to improve the surface roughness. When the Si/H ratio is small, the etching effect of H_2 is sufficient, and defects such as silicon droplets or down falls on the surface can be removed in time to make the surface smooth, and at the same time reduce the formation sites of defects in the epitaxy process. With the increase of Si/H ratio, the proportion of H_2 in the gas gradually decreases, so the etching effect gradually weakens. At the same time, as the proportion of Si in the gas gradually increases, it is easy to form silicon droplets or silicon clusters attached to the surface of the substrate, which increases the RMS. In addition, in the surface etching process of 4H-SiC, since the etching effect of H_2 on C atoms is greater than that of Si atoms [13,19], when the Si/H ratio increases, the binding ability of H_2 and Si atoms is relatively weak, resulting in insufficient etching effect. On the other hand, the growth rate tends to be saturated at a high Si/H ratio, which is more likely to lead to rougher surface morphology and surface inhomogeneity [39]. Figure 12 is AFM images of the 4H-SiC epitaxial wafer as a function of Si/H ratio, where the step height is mostly less than 10 nm when the Si/H ratio is 0.08%. With the gradual increase of the Si/H ratio, the height of the steps mostly floated between 9 and 17 nm, and the surface was observed to be smooth under an optical microscope. In addition, the overall morphology of the epitaxial wafer does not change much. The uniformity is slightly improved with increasing Si/H ratio.

In addition, through linear fitting of the data in Table 1, it is found that, with the increase of the distance between the measurement point and the wafer center point, the RMS value shows a downward trend. This trend in RMS within a single wafer surface is believed to be epitaxy related. Inside the epitaxy equipment used in this experiment, the Si/H ratio in the entire wafer is not absolutely uniform due to the influence of airflow during epitaxy growth. The flow rate of SiH_4 is smaller than that of H_2, and it is more susceptible to airflow. The Si/H ratio at the edge of the wafer is slightly smaller than that at the center of the wafer, so the etching effect of H_2 is more sufficient and the surface roughness is lower. When the Si/H ratio increases, the flow rate of SiH_4 increases, and the non-uniformity of the Si/H ratio caused by the airflow is weakened, so the correlation coefficient also decreases gradually.

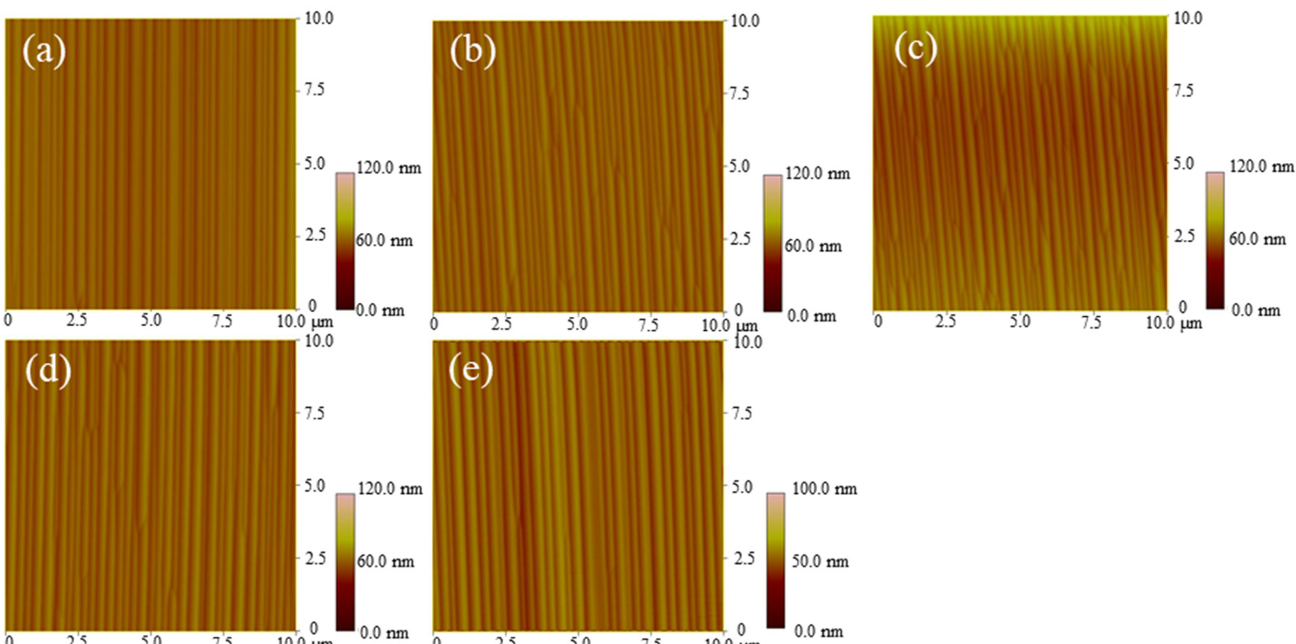

Figure 12. AFM images of 4H-SiC wafers with Si/H ratios of (**a**) 0.08%, (**b**) 0.10%, (**c**) 0.12%, (**d**) 0.13%, and (**e**) 0.15%.

4. Conclusions

By changing the gas flow rate and growth temperature, the effects of C/Si ratio, growth temperature, and Si/H ratio on the surface morphology and uniformity of wafer-sized 4H-SiC epitaxial layers were investigated. Through optical microscope and AFM observation of epitaxial wafers, it is found that the change of C/Si ratio has no obvious effect on RMS within the experimental range, and the minimum value of RMS is obtained at C/Si = 1. However, in a silicon-rich environment with a C/Si ratio of less than 1, better uniformity of the epitaxial surface can be obtained. With the change of growth temperature, RMS and σ show opposite trends. As the temperature increases, the RMS decreases, and the step bunching phenomenon gradually appears, and the intra-wafer uniformity also deteriorates to a certain extent. In contrast, the change of the process parameters Si/H ratio has no obvious effect on the RMS and uniformity of the surface of the 4H-SiC wafer-scale epitaxial layer.

Author Contributions: Conceptualization, S.Z.; methodology, S.Z. and J.W.; software, W.Z.; validation, S.Z., G.Y., Z.S. and L.W.; formal analysis, S.Z., J.W., G.Y., Z.S., W.Z., L.W. and X.L.; investigation, S.Z., J.W. and X.L.; resources, G.Y., Z.S. and X.L.; data curation, S.Z. and J.W.; writing—original draft preparation, S.Z.; writing—review and editing, S.Z. and X.L.; visualization, S.Z. and J.W.; supervision, X.L.; project administration, X.L.; funding acquisition, Z.S. and X.L. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Key Research and Development Program of China (Grant No. 2016YFB0400500) and the National Natural Science Foundation of China (Nos. 12175236 and 62104222).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available upon request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Kimoto, T. Material Science and Device Physics in SiC Technology for High-Voltage Power Devices. *Jpn. J. Appl. Phys.* **2015**, *54*, 040103. [CrossRef]
2. Zhao, Z.; Li, Y.; Xia, X.; Wang, Y.; Zhou, P.; Li, Z. Growth of High-Quality 4H-SiC Epitaxial Layers on 4° off-Axis C-Face 4H-SiC Substrates. *J. Cryst. Growth* **2020**, *531*, 125355. [CrossRef]
3. Kaloyeros, A.E.; Goff, J.; Arkles, B. Defect- and H-Free Stoichiometric Silicon Carbide by Thermal CVD from the Single Source Precursor Trisilacyclohexane. *Electron. Mater.* **2022**, *3*, 3. [CrossRef]
4. He, Y.; Yuan, Z.; Song, S.; Gao, X.; Deng, W. Investigation on Material Removal Mechanisms in Photocatalysis-Assisted Chemical Mechanical Polishing of 4H–SiC Wafers. *Int. J. Precis. Eng. Manuf.* **2021**, *22*, 951–963. [CrossRef]
5. Sako, H.; Kobayashi, K.; Ohira, K.; Isshiki, T. Microstructure of Stacking Fault Complex/Carrot Defects at Interface Between 4H-SiC Epitaxial Layers and Substrates. *J. Electron. Mater.* **2020**, *49*, 5213–5218. [CrossRef]
6. Niu, Y.-X.; Tang, X.-Y.; Jia, R.-X.; Sang, L.; Hu, J.-C.; Yang, F.; Wu, J.-M.; Pan, Y.; Zhang, Y.-M. Influence of Triangle Structure Defect on the Carrier Lifetime of the 4H-SiC Ultra-Thick Epilayer. *Chin. Phys. Lett.* **2018**, *35*, 077103. [CrossRef]
7. Nakamura, S.; Kimoto, T.; Matsunami, H. Rate-Determining Process in Chemical Vapor Deposition of SiC on off-Axis α-SiC (0001). *J. Cryst. Growth* **2004**, *270*, 455–461. [CrossRef]
8. Feng, X.; Chen, Z.; Ma, J.; Zan, X.; Pu, H.; Lu, G. Epitaxial Growth of Cubic Silicon Carbide on Silicon by Sublimation Method. *Opt. Mater.* **2003**, *23*, 39–42. [CrossRef]
9. Dhanaraj, G.; Dudley, M.; Chen, Y.; Ragothamachar, B.; Wu, B.; Zhang, H. Epitaxial Growth and Characterization of Silicon Carbide Films. *J. Cryst. Growth* **2006**, *287*, 344–348. [CrossRef]
10. Kakuta, A.; Moronuki, N.; Furukawa, Y. Surface Properties of SiC Layer Grown by Molecular Beam Epitaxy (MBE) with Helicon Sputtering Molecular Beam Source. *JSME Int. J. Ser. C Mech. Syst. Mach. Elem. Manuf.* **2004**, *47*, 123–128. [CrossRef]
11. Meli, A.; Muoio, A.; Trotta, A.; Meda, L.; Parisi, M.; La Via, F. Epitaxial Growth and Characterization of 4H-SiC for Neutron Detection Applications. *Materials* **2021**, *14*, 976. [CrossRef]
12. Leone, S.; Pedersen, H.; Henry, A.; Kordina, O.; Janzén, E. Improved Morphology for Epitaxial Growth on 4° Off-Axis 4H-SiC Substrates. *J. Cryst. Growth* **2009**, *311*, 3265–3272. [CrossRef]
13. Yazdanfar, M.; Ivanov, I.G.; Pedersen, H.; Kordina, O.; Janzén, E. Reduction of Structural Defects in Thick 4H-SiC Epitaxial Layers Grown on 4° off-Axis Substrates. *J. Appl. Phys.* **2013**, *113*, 223502. [CrossRef]
14. Tsuchida, H.; Kamata, I.; Miyazawa, T.; Ito, M.; Zhang, X.; Nagano, M. Recent Advances in 4H-SiC Epitaxy for High-Voltage Power Devices. *Mater. Sci. Semicond. Process.* **2018**, *78*, 2–12. [CrossRef]
15. Nishizawa, S.; Pons, M. Growth and Doping Modeling of SiC-CVD in a Horizontal Hot-Wall Reactor. *Chem. Vap. Depos.* **2006**, *12*, 516–522. [CrossRef]
16. Liu, X.F.; Yan, G.G.; Liu, B.; Shen, Z.W.; Wen, Z.X.; Chen, J.; Zhao, W.S.; Wang, L.; Zhang, F.; Sun, G.S.; et al. Process Optimization for Homoepitaxial Growth of Thick 4H-SiC Films via Hydrogen Chloride Chemical Vapor Deposition. *J. Cryst. Growth* **2018**, *504*, 7–12. [CrossRef]
17. Leone, S.; Pedersen, H.; Beyer, F.C.; Andersson, S.; Kordina, O.; Henry, A.; Canino, A.; La Via, F.; Janzén, E. Chloride-Based CVD of 4H-SiC at High Growth Rates on Substrates with Different Off-Angles. *Mater. Sci. Forum* **2012**, *717–720*, 113–116. [CrossRef]
18. Leone, S.; Beyer, F.C.; Pedersen, H.; Kordina, O.; Henry, A.; Janzén, E. Growth of Smooth 4H-SiC Epilayers on 4° off-Axis Substrates with Chloride-Based CVD at Very High Growth Rate. *Mater. Res. Bull.* **2011**, *46*, 1272–1275. [CrossRef]
19. Li, Y.; Zhao, Z.; Yu, L.; Wang, Y.; Zhou, P.; Niu, Y.; Li, Z.; Chen, Y.; Han, P. Reduction of Morphological Defects in 4H-SiC Epitaxial Layers. *J. Cryst. Growth* **2019**, *506*, 108–113. [CrossRef]
20. Shi, Y.; Zakharov, A.A.; Ivanov, I.G.; Vinogradov, N.A.; Yazdi, G.R.; Syväjärvi, M.; Yakimova, R.; Sun, J. A Patterning-Free Approach for Growth of Free-Standing Graphene Nanoribbons Using Step-Bunched Facets of off-Oriented 4H-SiC (0001) Epilayers. *J. Phys. Appl. Phys.* **2020**, *53*, 115102. [CrossRef]
21. Hu, J.; Jia, R.; Xin, B.; Peng, B.; Wang, Y.; Zhang, Y. Effect of Low Pressure on Surface Roughness and Morphological Defects of 4H-SiC Epitaxial Layers. *Materials* **2016**, *9*, 743. [CrossRef]
22. Zhao, L.; Wu, H. A Correlation Study of Substrate and Epitaxial Wafer with 4H-N Type Silicon Carbide. *J. Cryst. Growth* **2019**, *507*, 109–112. [CrossRef]
23. Daigo, Y.; Watanabe, T.; Ishiguro, A.; Ishii, S.; Moriyama, Y. Influence and Suppression of Harmful Effects Due to By-Product in CVD Reactor for 4H-SiC Epitaxy. *IEEE Trans. Semicond. Manuf.* **2021**, *34*, 340–345. [CrossRef]
24. Li, J.; Meng, C.; Yu, L.; Li, Y.; Yan, F.; Han, P.; Ji, X. Effect of Various Defects on 4H-SiC Schottky Diode Performance and Its Relation to Epitaxial Growth Conditions. *Micromachines* **2020**, *11*, 609. [CrossRef]
25. Hu, J.; Jia, R.; Niu, Y.; Zang, Y.; Pu, H. Study of a New Type Nominal "Washboard-like" Triangular Defects in 4H-SiC 4° off-Axis (0 0 0 1) Si-Face Homoepitaxial Layers. *J. Cryst. Growth* **2019**, *506*, 14–18. [CrossRef]
26. Sun, Y.; Feng, G.; Kang, J.; Zhang, J.; Qian, W. Analysis and Reduction of Obtuse Triangular Defects on 150-Mm 4° 4H-SiC Epitaxial Wafers. *J. Electron. Mater.* **2018**, *47*, 5109–5112. [CrossRef]
27. Yang, L.; Zhao, L.X.; Wu, H.W.; Liu, Y.; Ailihumaer, T.; Raghothamachar, B.; Dudley, M. Characterization and Reduction of Defects in 4H-SiC Substrate and Homo-Epitaxial Wafer. *Mater. Sci. Forum* **2020**, *1004*, 387–392. [CrossRef]
28. Yang, L.; Zhao, L.X.; Wu, H.W. Effect of Temperature on Conversion of Basal Plane Dislocations to Treading Edge Dislocations during 4H-SiC Homoepitaxiy. *J. Cryst. Growth* **2020**, *531*, 125360. [CrossRef]

29. Ito, M.; Storasta, L.; Tsuchida, H. Development of 4H–SiC Epitaxial Growth Technique Achieving High Growth Rate and Large-Area Uniformity. *Appl. Phys. Express* **2008**, *1*, 015001. [CrossRef]
30. Dong, L.; Sun, G.S.; Yu, J.; Yan, G.G.; Zhao, W.S.; Wang, L.; Zhang, X.H.; Li, X.G.; Wang, Z.G. 10 × 100 Mm 4H-SiC Epitaxial Growth by Warm-Wall Planetary Reactor. *Mater. Sci. Forum* **2013**, *740–742*, 239–242. [CrossRef]
31. Mauceri, M.; Pecora, A.; Litrico, G.; Vecchio, C.; Puglisi, M.; Crippa, D.; Piluso, N.; Camarda, M.; La Via, F. 4H-SiC Epitaxial Layer Grown on 150 Mm Automatic Horizontal Hot Wall Reactor PE106. *Mater. Sci. Forum* **2014**, *778–780*, 121–124. [CrossRef]
32. Das, H.; Sunkari, S.G.; Oldham, T.; Casady, J.R.B.; Casady, J.B. High Uniformity with Reduced Surface Roughness of Chloride Based CVD Process on 100 mm 4° Off-Axis 4H-SiC. *Mater. Sci. Forum* **2012**, *717–720*, 93–96. [CrossRef]
33. Sun, Y.Q.; Feng, G.; Li, Z.Y.; Lv, L.P.; Luo, J.Y.; Wu, J.B.; Li, Y.Y.; Zhang, J.H. 50 Mm-Thick 100 Mm 4H-SiC Epitaxial Layer Growth by Warm-Wall Planetary Reactor. *Mater. Sci. Forum* **2014**, *778–780*, 163–166. [CrossRef]
34. Wan, J.W.; Loboda, M.J.; MacMillan, M.F.; Chung, G.Y.; Carlson, E.P.; Torres, V.M. Scaling of Chlorosilane SiC CVD to Multi-Wafer Epitaxy System. *Mater. Sci. Forum* **2007**, *556–557*, 145–148. [CrossRef]
35. O'Loughlin, M.; Burk, A.; Tsvetkov, D.; Ustin, S.; Palmour, J.W. Advances in 3x150 Mm Hot-Wall and 6x150 Mm Warm-Wall SiC Epitaxy for 10kV-Class Power Devices. *Mater. Sci. Forum* **2016**, *858*, 167–172. [CrossRef]
36. Ferro, G.; Chaussende, D.; Tsavdaris, N. Understanding Al Incorporation into 4H-SiC during Epitaxy. *J. Cryst. Growth* **2019**, *507*, 338–343. [CrossRef]
37. Yan, G.G.; He, Y.W.; Shen, Z.W.; Cui, Y.X.; Li, J.T.; Zhao, W.S.; Wang, L.; Liu, X.F.; Zhang, F.; Sun, G.S.; et al. Effect of C/Si Ratio on Growth of 4H-SiC Epitaxial Layers on on-Axis and 4° off-Axis Substrates. *J. Cryst. Growth* **2020**, *531*, 125362. [CrossRef]
38. Zhao, L.X.; Yang, L.; Wu, H.W. High Quality 4H-SiC Homo-Epitaxial Wafer Using the Optimal C/Si Ratio. *J. Cryst. Growth* **2020**, *530*, 125302. [CrossRef]
39. Danielsson, Ö.; Karlsson, M.; Sukkaew, P.; Pedersen, H.; Ojamäe, L. A Systematic Method for Predictive in Silico Chemical Vapor Deposition. *J. Phys. Chem. C* **2020**, *124*, 7725–7736. [CrossRef]