*Article*

# SiC/Si Hybrid Substrate Synthesized by the Method of Coordinated Substitution of Atoms: A New Type of Substrate for LEDs

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**Abstract:** This paper proposes a new type of substrate for manufacturing LEDs based on AlInGaN heterostructures. Instead of depositing SiC layers on the surface of Si using the conventional method, a new method involving the coordinated substitution of atoms (MCSA) to form the SiC layer is proposed. This new approach enables the growth of epitaxial GaN layers with low defect content and facilitates transfer to any surface. The paper details the technology of manufacturing LEDs on SiC/Si substrates obtained by the MCSA and elaborates on the benefits of using these substrates in LED production. Additionally, the advantages of the growth interface between SiC and Si materials are discussed. Moreover, it is found that thinner SiC layers (<200 nm) contribute to the scattering of the LED's own radiation in the heterostructure waveguide, which decreases its absorption by silicon. For flip-chip LEDs with the substrate removed, substrates with thicker SiC layers (~400 nm) and a growth porous layer of several microns at the SiC-Si interface is utilized to simplify Si substrate removal and enhance the manufacturing process's cost-effectiveness.

**Keywords:** silicon-carbide LEDs on silicon; AlInGaN/GaN/SiC/Si heterostructures; wide-gap semiconductors; method of coordinated substitution of atoms

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## 1. Introduction

The development of blue light-emitting diodes (LEDs) has made remarkable progress since Nichia produced the first blue LED with a wavelength of 450 nm in 1992. In a little over 30 years, scientific teams have made significant strides with the use of AlInGaN heterostructures. Notably, they have not only replaced traditional light sources in areas such as general lighting, greenhouse, and decorative lighting, but the advancement also highlighted new niche applications. These new niches range from information visualization devices, such as displays, traffic lights, signs, and indicators, to instruments that use ultraviolet radiation for various purposes, including disinfection, purification, detection, and acceleration of polymerization. The development of micro-LEDs has further opened up prospects in various new areas, such as augmented reality, high-resolution microscopy, visible light communication, biomedical sensors and imaging systems, optoelectronic tweezers, optogenetics, and fluorescence-based sensors [1,2].

However, the rapidly growing commercial utilization of LEDs has created new challenges centered around cost efficiency and streamlining production processes. One crucial aspect is the selection of the substrate for the epitaxial growth of light-emitting heterostructures, which significantly influences the characteristics of the final LED product as well

as the technological processes involved in manufacturing. Unfortunately, only a limited number of substrates facilitate the epitaxial growth of gallium nitride (GaN) material due to the proximity required between the substrate material and the GaN material's lattice parameters [3]. Other factors, such as thermal conductivity, transparency at the wavelength of the heterostructure's radiation, and electrical conductivity, also play significant roles in chip design. Although silicon carbide substrates appear optimal in terms of these criteria, their high production costs have resulted in the widespread adoption of sapphire substrates. As a result, the vast majority of LEDs currently in production have chips grown on sapphire substrates.

Silicon wafers are a cost-effective option for LED production due to their good electrical and thermal conductivity and established processing methods. However, their use as substrates for GaN-based LEDs is hindered by a large mismatch between the crystal lattice parameters of silicon and GaN. This results in numerous defects, reduced light generation efficiency, and renders the substrate opaque and light-absorbing. Thus, it is unsuitable for use as a substrate.

One potential alternative is the manufacturing of silicon wafers with a thin layer of SiC/Si silicon carbide. This approach combines the benefits of both materials while avoiding the excessive costs of pure SiC substrates. A study has shown the feasibility of growing GaN on such substrates [4]; however, the growth of high-quality GaN requires the use of very thick SiC layers (>1 micron) [5]. Another study utilized amorphous SiC on $SiO_2$/Si substrates to create thin-film LEDs [6].

Despite the potential benefits of SiC layers as a buffer layer for GaN film growth on silicon substrates, there are significant challenges to overcome to produce low-defect-density layers. Standard growth methods result in a substantial lattice parameter mismatch between Si and SiC (~19%), producing numerous dislocations and growth defects. This is the first (and main) problem preventing the production of high-quality SiC epitaxial films on Si. At the film-substrate interface, this creates numerous mismatch dislocations and growth defects, and thicker SiC on Si films (>1 μm) show cracks. Additionally, the large difference in thermal expansion coefficients between Si and 3C-SiC presents significant challenges. According to data [7], the linear coefficient of thermal expansion is $3.9 \times 10^{-6}$ $K^{-1}$ for 3C-SiC and $2.6 \times 10^{-6}$ $K^{-1}$ for Si. Consequently, when Si plates with SiC layers cool from the growth temperature to room temperature, this creates bends and cracks. In the review [8], there is a picture of the deflection of the Si plate with epitaxial SiC film. Moreover, the low melting point of Si (1412 °C) restricts the growth of SiC films synthesized on Si to temperatures that are equal to or below 1500 °C. Beyond 1500 °C, the diffusion mobility of components and the rate of chemical reaction between component options increase, which allows for the oriented nucleation of two-dimensional SiC nuclei. To achieve SiC film growth below 1412 °C, researchers must pre-modify the Si surface. They have discovered that carbonizing the Si substrate before growth [8,9] results in a SiC buffer layer that serves as a seed for further epitaxy of 3C-SiC layers while significantly affecting their deformation. However, carbonization has not solved the problem of obtaining 3C-SiC layers with low defect content suitable for the creation of commercial semiconductor devices. This problem could not be solved by the pre-deposition of ultra-thin layers of Ge on the surface of the silicon substrate. The authors of [10] believed that if a thin layer of Ge is pre-deposited on the Si substrate surface and then SiC is deposited on top of this layer, a transition layer consisting of solid solutions of Si, Ge, and C will form between the Si substrate and SiC. They believed that the formation of this layer would reduce the elastic energy arising from the difference in the lattice parameters of SiC and Si. However, the authors were able to obtain only SiC films consisting of granules. In [11], $Si_{1-x}Ge_x$ solid solution layers obtained by molecular beam epitaxy were used as a buffer layer. In this case, the authors obtained solid SiC films; however, their degree of perfection was not sufficient for further use. The review [12] analyzed in detail the reasons why it is impossible to obtain highly perfect SiC layers on Si when precursors, from which SiC grows, are deposited directly on the Si surface.

Note that the formation of nanoscale SiC is also possible in the process of synthesis of silicon nitride-silicon carbide micronanocomposites. This synthesis is carried out by sintering grains $Si_3N_4$ in the presence of various kinds of polycarbosilanes which are precursors of silicon carbide. These processes are described in detail in the review [13]. However, the synthesis of silicon carbide using sintering methods [13,14] is not suitable for the production of high-performance single-crystal SiC layers on Si, suitable for applications in microelectronics and optoelectronics.

Several works [15–19] have been conducted on an alternative SiC growth method on Si that significantly differs from existing techniques. In this method, a SiC film is created by replacing half of the Si atoms within the near-surface Si layer with the formation of a continuous SiC layer instead of precursor introduction onto the Si surface and subsequent chemical reaction to form the SiC layer. Chemical interaction between gaseous carbon monoxide (CO) and the surface of the silicon substrate by reaction (1) replaces the atoms:

$$2\mathrm{Si}(cr) + \mathrm{CO}(gas) = \mathrm{SiC}(cr) + \mathrm{SiO}(gas) \uparrow . \quad (1)$$

During this reaction, one silicon atom transforms into SiO, which is in a gaseous phase at temperatures above 900 °C and exits the reaction zone. Consequently, the vacancy created by the removed silicon atom is occupied by carbon. The unique trait of reaction (1) is that it comprises two stages [16,18,19].

During the first stage of reaction (1), the CO molecule interacts with the silicon substrate's surface, disintegrating it into a carbon atom and an oxygen atom. The oxygen atom and Si atom then undergo a chemical reaction to form SiO gas, which is eliminated from the system, thereby creating a vacancy in place of the transformed substrate silicon atom. The carbon atom released from the CO molecule, being energetically excited, moves to an interstitial site in the silicon lattice [16,18]. This stage can be described as follows:

$$\mathrm{CO}(\boldsymbol{gas}) + \mathrm{Si}(\boldsymbol{crystal}) = \mathrm{C}(\boldsymbol{point\ defect\ in}\ \mathrm{Si}) + \boldsymbol{V}_{\mathrm{Si}} + \mathrm{SiO}(\boldsymbol{gas}), \quad (2)$$

where $V_{Si}$ is the silicon vacancy. During this stage, an intermediate phase called "pre-carbide" silicon emerges. This phase is saturated with defect pairs $C + V_{Si}$ in silicon. As indicated by (2), point defect pairs $C$ and $V_{Si}$ appear and vanish concurrently. Essentially, "pre-carbide" silicon features silicon where every other Si atom is replaced by a C atom via reaction (2). This results in each Si cell containing four pairs of dilatational defects $C + V_{Si}$. Consequently, "pre-carbide" silicon is prepared for the conversion of Si to SiC. This process occurs in the subsequent reaction stage, described by Equation (3):

$$\mathrm{Si}(\boldsymbol{crystal}) + \mathrm{C}(\boldsymbol{point\ defect\ in}\ \mathrm{Si}) + \boldsymbol{V}_{\mathrm{Si}} = \mathrm{SiC}(\boldsymbol{crystal}). \quad (3)$$

During this stage, carbon atoms shift towards silicon vacancies to create silicon carbide, which occurs in a coordinated manner [16]. The final topochemical reaction (1) represents the sum of stages (2) and (3).

The notable feature of reaction (1) is its conclusion with the formation of silicon carbide related to both stage (2) and stage (3). Reaction (2) necessitates "free space" in the silicon cell to contain a carbon atom. Only one carbon atom can occupy this cell, allowing for the replacement of just four out of eight silicon atoms; otherwise, a highly elastically stretched lattice of diamond would result, with much greater activation energy than can be overcome under the given conditions. Even the reaction of placing a carbon atom in each silicon crystal cell is infeasible, as such atoms can only be incorporated if a silicon atom is removed, i.e., if the cell has a silicon vacancy and the point defects (carbon and vacancy) must strictly lie along the Si <111> crystallographic axis. Along other crystallographic directions in Si, reaction (2) cannot progress. Therefore, (2) not only "selects" the four Si atoms it requires but also "assigns" the locations for the single crystallographic direction along which the future SiC crystal lattice develops. Reaction (2), however, is insufficient for Si-to-SiC transformation. Reaction (3) is responsible for completing the synthesis process

of SiC. During reaction (3), the five crystal cells of SiC formed almost exactly coincide with the four cells of Si, according to research [18]. Thus, the atom displacement occurring in reaction (3) necessitates minimal energy expenditure and completes the process of the "final docking" of crystal lattices.

The growth method employing the coordination of the substitution of atoms was named the MCSA method in [20], which we will refer to by its acronym MCSA hereafter. A schematic depiction of the growth of SiC layers on Si using MCSA is shown in Figure 1a. A comprehensive explanation of the method and its accompanying circumstances can be found in previously published reviews [17,18].

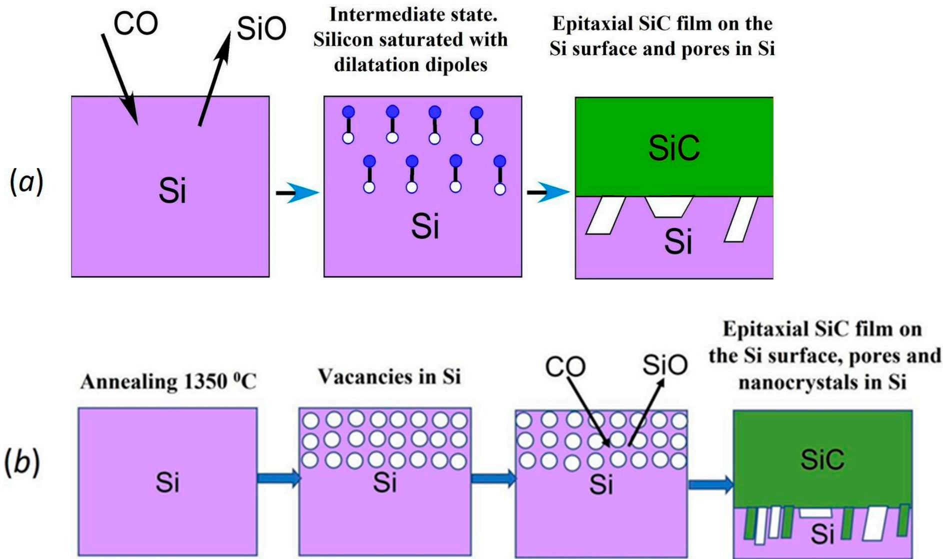



**Figure 1.** Schematic of SiC growth on Si by the methods of coordinated substitution of atoms. (**a**) Scheme of SiC growth by MCSA. (**b**) Scheme of SiC growth by VMCSA.

The principal contrast between the MCSA method and others is that the SiC layer does not grow in a conventional manner on the topmost layer of Si. Rather, it is formed right within the volume of the silicon substrate as a result of the chemical reaction (1).

The formation of pores and vacancies in the silicon matrix when removing SiO gas from the system is helpful in relaxing the elastic stresses caused by discrepancies between the Si and SiC lattice parameters. According to calculations [11,12,14], the ordering and formation of the SiC layer are significantly aided by specific stable entities–dilatational dipoles that entail two dilatational centers. One center expands the Si lattice, which is the SiC molecule, while the other center compresses it by means of the silicon vacancy. The mutual attraction of these two dilatational centers effectively reduces elastic stresses at the initial nucleation stage and encourages the organization of formed SiC molecules, mimicking steps and fractures on the crystal surface. Electron microscopy research has demonstrated that the concentration of mismatched lattice dislocations is truly negligible in this growth mechanism; thus, GaN, AlN, and AlGaN layers grown on such templates, specifically SiC nanolayers on Si substrates, will also exhibit a minimal mismatch dislocation density [18].

The MCSA method [15–19] has a primary drawback in that it physically constrains the thickness of the grown SiC layer. It is impossible to produce SiC layers thicker than 200 nm with this method. As the surface layers of silicon transform into silicon carbide, the penetration of reagent gas to the reaction front in the silicon volume becomes less feasible, and when the critical thickness is achieved, the reaction stops. This is due to the distance between the atoms in the crystal cell of the produced SiC being smaller than in the original Si, which also leads to a decreased diameter of the interatomic distances in SiC through which CO gas enters and SiO gas exits. Consequently, as SiC is formed, the gas velocity decreases. Ultimately, CO gas struggles to penetrate more deeply, and SiO gas

halts, being eliminated from the system, reaching chemical equilibrium and bringing the reaction to a stop.

Furthermore, while growing SiC with this method, the SiC layers, despite having pores beneath them, firmly adhere to the Si surface. Consequently, when depositing LED heterostructures on this surface, separating them from the silicon substrate becomes challenging. This can hinder maximizing efficiency values on those chips since the SiC layer's part bordering the Si is opaque.

In [21], the MCSA method [15–19] was notably advanced with the proposal and implementation of the vacancy-coordinated atom substitution method. The technique facilitates a considerable increase in the thickness of the silicon carbide layer during atom substitution. The SiC synthesis with this method enables the separation of silicon carbide from the silicon substrate when the SiC layer thickness surpasses 400 nm. The primary disparity between this synthesis method and the one described above is that, from the outset, silicon is annealed in a vacuum at a temperature between 1250–1390 °C in the near-surface layer of initial silicon, even before adding CO gas to the reaction chamber, for 5–30 min. This process enables the formation of a group of silicon vacancies in the near-surface Si layer. In the diffusion zone where the concentration of "thermal" (non-equilibrium) silicon vacancies is raised, chemical bonds within the silicon weaken considerably. The silicon lattice enters into an unstable state. Gases can readily penetrate deep into the silicon, similar to the absorption of moisture by a compressed porous sponge. The early vacuum creation process vaporizes all the silicon from the surface of the silicon substrate instead of allowing it to settle and "close" the vacancy channels forming. Hollow, vertically oriented chains of vacancies are formed inside the silicon. Throughout the silicon evaporation process, even while in a vacuum, the vacancies lead to elastic compression of the silicon surface layer when some of the silicon atoms evaporate. It is worth mentioning that since vacancies alter the volume of the crystal, it is "more beneficial" for them to form in a coordinated fashion, forming lines or chains of vacancies along the crystal surface. In the second stage of synthesis, CO gas is introduced. Once CO gas enters the system, it rapidly saturates the elastically stressed layer, comparable to a squeezed sponge absorbing moisture. The elastic stresses relax, but the silicon structure prepared with this annealing already contains the gas that penetrated it, and the chemical reaction (1) commences. In contrast to the MCSA method described above, in this case, the chemical reaction initiates at a significant depth and occurs uniformly throughout the initially compressed silicon layer. The Si layer thickness (0.5–5.0 microns) transforms into a silicon carbide layer with the formation of a decompressed contact at the interface due to the creation of flattened lacunas that are two to three times the size of the pores. The SiC layer thickness is dependent on the silicon evaporation rate, which is determined by the temperature and the degree of vacuum depth. The SiC layer produced using this method can be readily separated from the silicon substrate and transferred to other materials. Figure 1b presents a schematic description of the vacancy-matched coordinated substitution of atoms method, which will be abbreviated as VMCSA from hereon. Note that the structure and properties of SiC films grown on Si by MCSA and VMCSA methods have been studied in detail previously. The composition, structure, thickness, and properties of the films were characterized by XRD, RHEED, Raman spectroscopy, and spectroscopic ellipsometry. Data obtained by the TEM method were also taken and analyzed. In addition, X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy, Rutherford backscattering (RBS), X-ray reflectometry, and IR spectroscopy were used. The SiC layers were also studied by photoelectron spectroscopy using synchrotron radiation in the energy range of 80–450 eV. These studies were summarized in reviews [12,18,19,22].

This paper outlines the primary technological benefits derived from utilizing SiC/Si substrates grown via both the MCSA and VMCSA methods in manufacturing LEDs based on AlInGaN heterostructures. The article will elucidate the LED production process based on AlInGaN heterostructures grown on SiC substrates obtained using the MCSA and VMCSA techniques.

To illustrate the possibility of producing LEDs on new hybrid substrates, two LED chip configurations were selected. The first design is the face-up geometry of the chip. This configuration emphasizes that both contact pads (n- and p- regions) of the heterostructure are positioned on the same surface of the heterostructure, and most of the light is extracted out to the GaN p-region through the transparent contact elements. It is the simplest design to produce and is employed in mass production for most LEDs on sapphire substrates. The obvious disadvantage of this design is the light absorption while passing through the upper light output and the contact surface concurrently. Since LEDs necessitate homogeneous current distribution across the active area surface, it becomes necessary to compromise between the conductivity and transparency of p-contacts and construct additional metal, opaque current-carrying bars on the chip surface. Additionally, this chip design requires the creation of contact pads on its surface to attach current-carrying wires. However, the primary issue with the face-up chip design is insufficient heat dissipation from the active chip area, particularly when the LEDs operate at high currents. This is mainly due to the sapphire substrate's low thermal conductivity, which acts as a barrier between the active chip area and the heat sink. Sapphire's thermal conductivity is inferior to many other materials, including silicon. Consequently, if we consider crystals with the face-up design, growing them on SiC/Si substrates is advantageous in terms of LED "thermal management" compared to growth on sapphire. Nevertheless, a significant disadvantage of designing chips with this configuration on a SiC/Si substrate is their opacity, leading to a loss of some of the generated radiation.

An alternative design for LED chips on a sapphire substrate that avoids these drawbacks is called the reverse or flip-chip design. In this configuration, the LED crystal is mounted on the heat sink's front side (i.e., epitaxial layers), and the light is guided through a transparent sapphire substrate. P-contact materials, such as metals with high reflectivity in the blue-violet region of the spectrum (e.g., silver or aluminum), are used in this design. This eliminates several issues typical of the face-up chip design, such as ensuring the current flow uniformity over the p-area surface and using any required thickness of p-contact metals. The active region is in close proximity to the heat sink (separated by a p-layer with a thickness of one-tenth of a micron and high thermal conductivity p-contact metals). To use this design for LEDs grown on a SiC/Si substrate, the opaque silicon part of the substrate must be removed.

The practice of removing the growth substrate is also utilized for sapphire growth wafers, despite their transparency in the entire visible wavelength range of radiation. In this case, the primary aim is to minimize losses caused by light reflection at the sapphire-heterostructure interface. The high contrast of the refractive index of the materials at this interface results in substantial reflection anomalies, decreasing the quantum efficiency of LEDs. To mitigate this effect, the substrate is eliminated, and the heterostructure surface is structured through liquid [23,24] or plasma-chemical [25–27] or a combination of both [28] etching processes. This generates a nanoscale pattern that facilitates light extraction from the LED chip's surface.

To remove the growth substrate from the LED flip-chip design, they are placed on a subcrystal board, and after removing the substrate, a relief is formed on the exposed surface of the chip. In the case of LED chips on a sapphire substrate, its elimination is conducted under the influence of a powerful ultraviolet pulse, typically an excimer laser [26–29], leading to a considerable number of defects in the light-emitting heterostructure due to the applied shock loads. The heterostructure becomes highly prone to significant deformations caused by the removal of internal stresses from the growth process between the heterostructure and substrate. Furthermore, subsequent operations are undertaken to generate a light-emitting surface on the heterostructure's outer boundary, which also facilitates the development of defects in the heterostructure.

Flip-chip LEDs with the growth substrate removed, often referred to as thin-film flip-chip (TFFC), are in demand when creating UV LEDs with low-conductivity buffer layers as part of the heterostructure [26,28–31].

## 2. Materials and Methods

The first type of SiC/Si substrate was produced through the MCSA method on a 2-inch diameter p-type conductivity silicon orientation substrate (111) with a resistance of 10 Ω·cm. The growth temperature during the process was 1270 °C, and the CO pressure was 2 Torr with a flux of 12 sccm for 15 min. Typically, a 25% silane ($SiH_4$) concentration is added to the CO gas to enhance the SiC layer's smoothness in the MCSA method. The thickness of the resulting SiC layer (111) was 100 nm.

The second type of SiC/Si substrate was produced using the VMCSA method. The SiC layer growth was carried out on a 2-inch diameter p-type conductivity silicon orientation substrate (111) with a resistance of 10 Ωcm. Before CO injection, the Si substrate was pre-annealed in a vacuum at 1300 °C for 10 min following the method's conditions. Then, the CO gas was introduced, and the synthesis time was 30 min. The CO pressure was 2 Torr with a flow of 12 sccm, with no silane introduced into the reaction chamber.

The LED structures were grown on an Aixtron 2000HT, Aachen, Germany machine using the hydride vapor phase epitaxy (HFE MOS) method with an inductively heated graphite substrate. The growth practice employed standard sources, including trimethyl gallium, triethyl gallium, trimethylaluminum, trimethylindium, and ammonia for layer growth, along with monosilane and magnesocene for doping. The process employed nitrogen, hydrogen, or a combination of both as the carrier gas.

The growth process began with the deposition of an AlN layer, followed by the growth of five layers of solid solutions $Al_xGa_{1-x}N$ using the HFE MOS method. The layers exhibited a stepwise decrease in Al content from 0.8 ($Al_{0.8}Ga_{0.2}N$) to 0.2 ($Al_{0.2}Ga_{0.8}N$). The process also included the growth of a superlattice containing 22 periods of 6 nm GaN/7 nm AlGaN and a 1.3 μm thick GaN:Si layer. Next, an active region was formed, which included a short-period superlattice (SPSL) composed of 12 periods of 1 nm InGaN/1 nm GaN, a 25 nm thick GaN layer, a series of three ~2 nm wide InGaN quantum wells, with each well separated by 7 nm thick GaN barriers, and a 15 nm $Al_{0.15}Ga_{0.85}N$:Mg electron blocking layer. Finally, a 130 nm thick GaN:Mg contact layer was grown.

The details of the growing technology and data on the structural properties of the structures are given in [32]. In [32], detailed TEM images of the end chipping of all heterostructure layers are given, and a detailed analysis of them is performed. In the experiments, a LED heterostructure on silicon substrates without a SiC layer was grown in a similar way. A schematic representation of the fabricated face-up chip is shown in Figure 2a, and its cross-section is shown in Figure 2b.

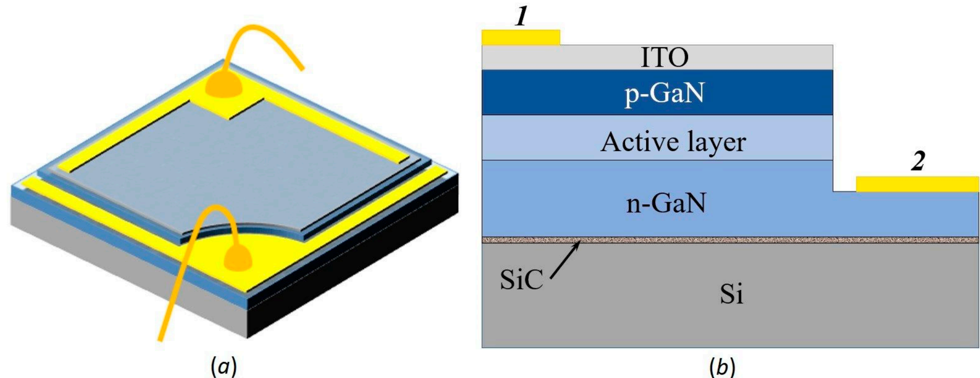



**Figure 2.** Schematic representation of the design of the LED chip with the upper translucent contact (**a**); its cross-section (**b**). 1—metallization of the p-contact, 2—metallization of the n-contact.

The LED chip has a contact surface area of 500 × 500 $\mu m^2$, with a mesa structure etched into the n-layer on two adjacent sides and metal bars on the n-contact. The remaining larger surface area of the chip areas the p-contact, which is primarily composed of a transparent conductive layer of indium tin oxide (ITO) that guides the light out of the chip. The chip's active region, which is the p-n junction area, was 0.1 $mm^2$.

To simplify the flip-chip design's technological processes, a straightforward configuration of contact arrangements on the heterostructure surface was selected, where a rectangular p-region with a contact located on it was situated on the chip's centerline (refer to Figure 3). On two opposite sides of it, narrow rectangular mesa-structures were etched into the heterostructure until the n-layer level, intended for n-contact placement. For ease of mounting the chip to the subcrystal board, the n-pin pads were raised in height on the edges of the chip to the same level as the p-region. The LED chip has dimensions of 0.7 mm × 0.56 mm, and its active area is 0.13 $mm^2$.

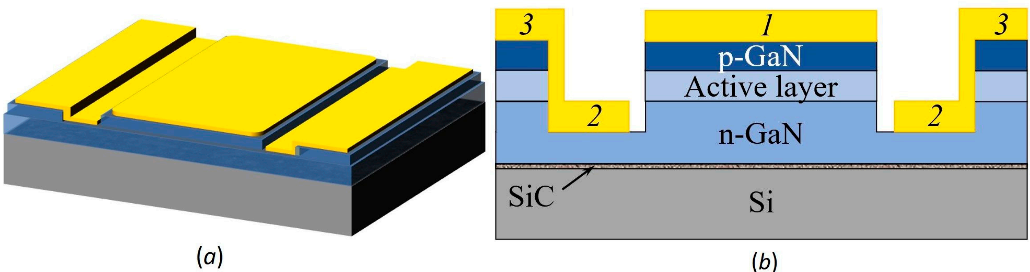



**Figure 3.** Schematic representation of the flip-chip LED design (**a**); cross-section (**b**). 1—metallization of the p-contact, 2—n-contact, 3—metallization of the n-contact, brought to the level of the p-region.

The LED production process was composed of several technological operations. Etching of the mesa-relief in the AlInGaN epitaxial layers was performed to open the area for n-contact with a depth of 0.3 µm by reactive ion etching in an atmosphere of $Cl_2$:$BCl_3$:Ar, at a pressure of approximately 1 Pa, for the chips of both designs.

The p-region face-up chip contact fabrication began with the deposition of an ITO film using electron-beam evaporation at a substrate temperature of 500 °C. The use of this temperature allowed for obtaining films with nanowires, providing a gradient of the effective refractive index in the plane perpendicular to the substrate plane [33]. It led to the absence of a pronounced refractive index contrast at the film's boundary with the external environment, resulting in an enlightening effect. Since the film structure contained a significant number of voids, its thickness was 700 nm. The mass content of the substance in the film corresponded to its mass content in an unstructured dense film with a thickness of 200 nm. Conductive metal bars were placed on opposite sides of the n-contact square's ITO layer for a more uniform current flow in the p-contact plane. A combination of Ti/Au metals with layer thicknesses of 25 nm and 200 nm, respectively, was utilized as the p-contact bus material.

To make contact, a combination of Ni/Au layers with thicknesses of 20 nm and 100 nm, respectively, was applied to the p-region of the flip-chip design. Further, in order to obtain contact with the n-GaN surface, the contact pads of the chips of both designs were made of a combination of Ti/Au metals.

It is recommended to use metals with high reflectance at the LED's emission wavelength in metal contacts in both regions of the heterostructure to improve the quantum yield of flip-chip design LEDs. However, since the primary objective of this study was to perform the fundamental manufacturing operations of TFFC chips on SiC/Si substrates, the simplest metal combinations in manufacturing were selected.

The chip plates of both configurations were cut using 20 µm thick diamond disks. The individual chips of the face-up design were positioned on the LED body using a thermally conductive adhesive, and the positive and negative contacts of the LED body were connected to the p- and n-contact pads of the chip, respectively, via gold wires. The chip was subsequently covered with an epoxy compound lens.

To organize the radiation output from the flip-chip design, the opaque substrate had to be removed. To do so, the chips were placed on specially made submounts, which are ceramic plates of AlN composition with metal conductive rails applied to them. The pattern of metallization areas formed on the submounts and designed to place the chip and

bring electric current to it, determined by the shape of the contacts of the chip itself. The chips were placed on the submount with the opaque silicon part of the substrate facing up, using contactol, because it is more resistant to the various chemical solutions used as an etchant, which is necessary for the successful subsequent removal of the opaque part of the substrate. The removal of the substrate was carried out using a liquid method, wherein the chip placed on the submount was submerged in a specially formulated etchant consisting of HF. The etchant was hydrogen peroxide and hydrofluoric acid solution with a ratio of H2O2:HF = 1:1, along with the addition of several drops of Br. Figure 4 displays a schematic illustration of the chip on the submount after the substrate's removal.

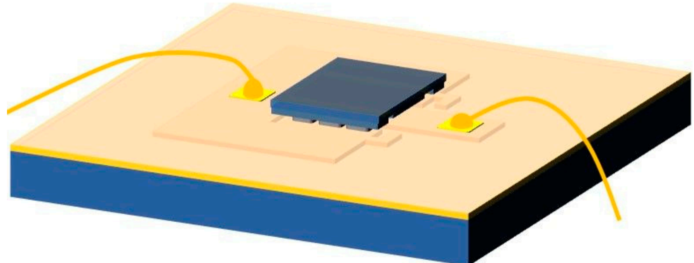


**Figure 4.** Schematic representation of the design of a flip-chip LED crystal placed on a submount.

## 3. Results

In Figure 5, microphotographs obtained with a scanning electron microscope (SEM) raster display the end chips of two types of SiC/Si (111) substrates. Figure 5a depicts an image of the SiC layer synthesized through the MCSA method [18], while Figure 5b displays an image of the SiC layer synthesized through the VMCSA method [21]. These images clearly demonstrate substantial differences between the structures of the SiC layers and the SiC-Si interfaces of the SiC films obtained through these methods. The SiC layer grown via the MCSA method tightly adheres to the Si surface, where pores exist beneath the SiC layer. The film grown through the VMCSA method is isolated from the silicon substrate by a layer of randomly arranged silicon columnar carbide crystals.

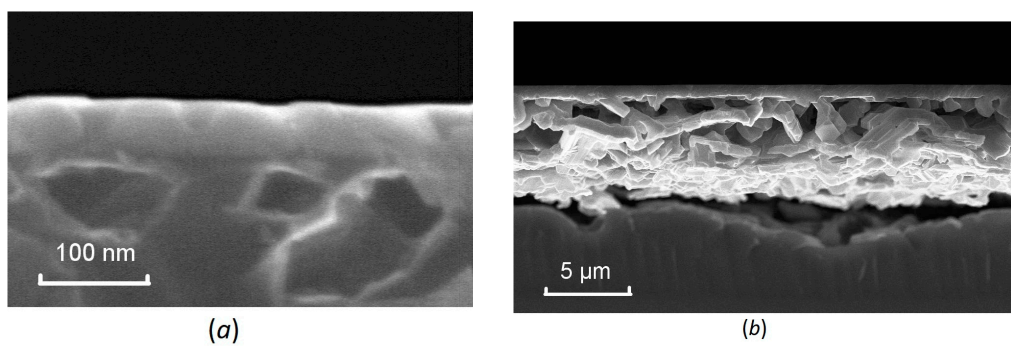



**Figure 5.** SEM images of the end chips of the substrates obtained by the MCSA (**a**) and VMCSA methods (**b**).

In [34], the thermal resistance of Si wafers with both thin and thick SiC layers was investigated. As a result, it was found that the thermal conductivity of wafers containing thin SiC layers up to 200nm thick corresponds to the thermal conductivity of silicon wafers. Consequently, the inclusion of a minimum-thickness SiC layer does not lead to overheating of the active part of the chip face-up design. In addition, the overall thermal resistance of the p-n junction heat sink circuit for the chip located on hybrid wafers is significantly lower than that of sapphire wafers. Since the conventional value of thermal conductivity of silicon at 300 K is 149 W/(mK), and the thermal conductivity of leucosapphire at the same temperature is 23 W/(mK) for the same substrate thickness, LEDs on silicon substrate will be more than six times more efficient in heat removal from the active area of the chip, which, in turn, leads to minimized overheating of the active area of the chip. Accordingly,

chip operation at lower temperatures means higher quantum efficiency, as well as less degradation of chip parameters during operation. In the same study [34], it was found that the thermal resistance of thick SiC layers separated from the Si substrate corresponds to the thermal resistance of pure silicon carbide layer of 3C-SiC polytype, i.e., the thermal conductivity of the layer is 360 W/(mK).

The growth of AlInGaN LED heterostructures was successfully performed on SiC/Si substrates with SiC layers of different thicknesses. The wafer processing of light-emitting diode heterostructures highlighted several advantages of applying SiC/Si substrates in comparison to sapphire substrates. As mentioned earlier, the use of standard technology for silicon and cost-effective methods of separating wafers into individual chips significantly simplifies the chip production process. It is worth noting that the hardness of a sapphire substrate requires expensive equipment for grinding and cutting wafers. As one knows, the hardness of silicon and sapphire is seven and nine on the Mohs scale, respectively. Hence, the procedure for thinning the silicon substrate, which is used to reduce thermal resistance between the p-n junction and the heat sink, will proceed at high speeds; in the case of silicon, it becomes possible to use a wider range of abrasives (including less expensive ones) than for sapphire. In the case of sapphire, as a rule, expensive laser cutting machines are used for cutting wafers into individual chips, while cutting silicon wafers can be easily carried out using cheaper methods such as scribing or cutting with diamond disks.

The presence of a growth interface at the interface of the SiC and Si layer plays a positive role in the fabrication of chips of both considered designs. It is common knowledge that during the manufacture of light-emitting devices, surfaces with relief are often utilized to reduce Fresnel reflection at the interface of the chip with the external environment. This is because the high refractive index of the material that makes up the chip causes most of the generated radiation to be absorbed in the chip itself, reflecting many times from its interfaces. To combat the negative effects of total internal reflection in blue wavelength range LED chips, the most commonly used approach is growing heterostructures on pre-profiled sapphire substrates [35–37]. Similar to the inconsistencies on profiled sapphire, the pores characteristic of wafers with thinner SiC layers create a light-scattering relief at the interface of the optical waveguide formed by the heterostructure together with a thin SiC layer (as shown in Figure 5a). Figure 6 demonstrates the scattering relief principle's operation at the heterostructure-substrate interface in a schematic representation.

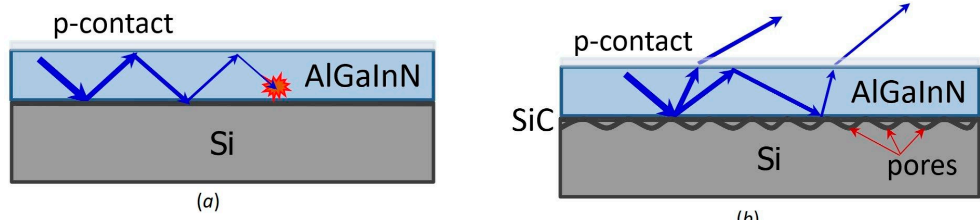



**Figure 6.** Schematic representation of the principle of scattering relief operation. The beam propagating in the waveguide of the heterostructure: (**a**) is absorbed in its active layer and in the substrate itself in the case of Si substrate, (**b**) is scattered on the rough heterostructure-substrate interface, as a result of which part of the radiation with an angle smaller than that of total internal reflection is extracted from the chip.

In comparison to the non-absorbing sapphire substrate, the situation in silicon is worsened by the fact that light is not only absorbed in the heterostructure's active layer but also by the substrate itself. Therefore, light rays scattering on the interface irregularities will have a more significant impact. Furthermore, the existence of pores at the substrate/heterostructure interface creates a medium with a reduced effective refractive index since the refractive index of the pore containing no embedded material is unity. Thus, the light reflection coefficient from such an interface will be higher than in the case of a substrate without pores. As a result, the pores provide two positive effects simultaneously, scattering light and minimizing light absorption by the substrate. Figure 7 presents

optical microscope images of chips grown on SiC/Si and Si substrates. The photo was taken after cutting the wafer into individual chips. The structures on the hybrid substrates demonstrated efficient light scattering on the growth pores.

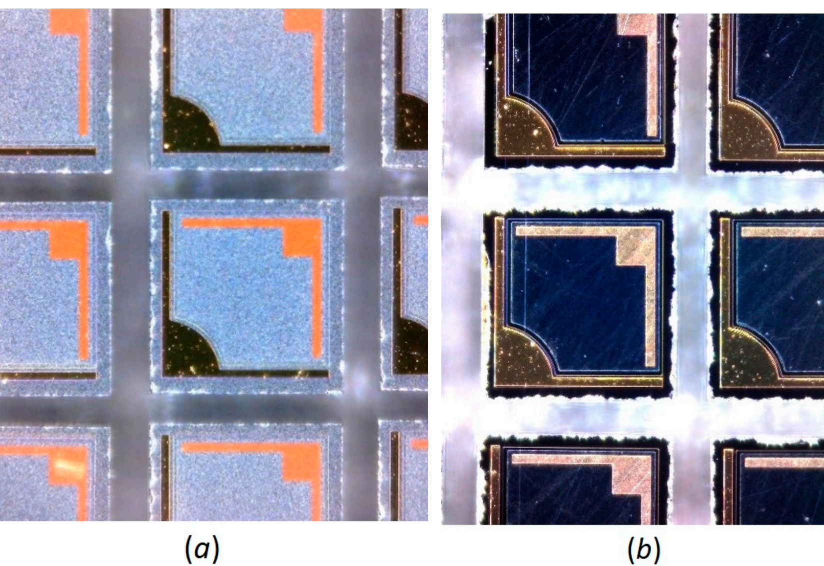



**Figure 7.** Photographs of finished chips made on substrates: (**a**) SiC/Si, (**b**) Si.

The scattering nature of the growth pores is also evident when comparing the emission spectra of the chips measured on the wafers before they were separated into individual chips (as shown in Figure 8). The peak wavelength of the chips on SiC and Si substrates was 470 nm. However, since the measurements were made on the wafer and not in the integral sphere, the graph corresponding to the chip on the silicon substrate distinctly reveals interference maxima and minima resulting from its own radiation interference within the heterostructure. The emission spectrum of chips on a hybrid substrate exhibited an entire absence of interference extremes due to light scattering on the growth pores of the substrate.

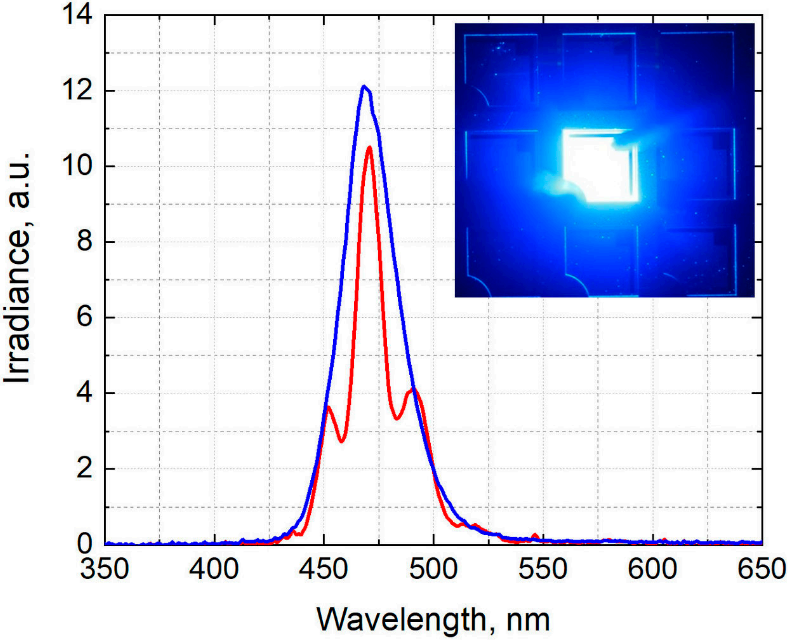



**Figure 8.** Emission spectra of LEDs: SiC/Si-blue curve, Si-red curve, in the inset photo of the lit-up chip on the wafer.

## 4. Discussion

Contrary to SiC/Si substrates with a SiC layer of relatively limited thickness in which the formation of individual pores is observed, promoting the alignment of lattice parameters of SiC and Si, growing silicon carbide with a thickness greater than 200 nm leads to a continuous porous SiC layer that is several microns thick (as depicted in Figure 5b). The presence of such a layer should positively impact the quantum yield of face-up LED, as it increases reflection from the heterostructure/silicon interface, reducing light absorption in silicon. However, as demonstrated in Figure 5b, the substrate's thermal resistance significantly rises [32] due to the layer's near-complete isolation from the Si substrate, equating to virtually no heat dissipation. Thus, for better heat dissipation, it is necessary to transfer this layer, along with the heterostructure on its surface, to a well-heat-dissipating substrate or to silicon without SiC synthesis. As a result, the use of this kind of substrate presents numerous advantages in creating an alternate LED chip design–TFFC.

Firstly, the porous layer makes separation of the substrate from the chip much easier by providing direct access of the chemical etchant to the silicon/heterostructure interface, eliminating the need to etch the entire silicon substrate, which typically occurs during chip production on silicon substrates. Selective etchants capable of etching the silicon without affecting the heterostructure are required for this process, however. Utilizing the initially selected alkaline etchant, an aqueous solution KOH (40%)/$C_2H_6O$ (10%), resulted in significant degradation of the heterostructure itself, as demonstrated in Figure 9. The formation of hexagonal pyramidal structures from etching along selective planes with KOH solutions for GaN as the etchant is a well-known process used to create light-emitting surfaces in LEDs with the substrate eliminated [23,24], as discussed earlier.

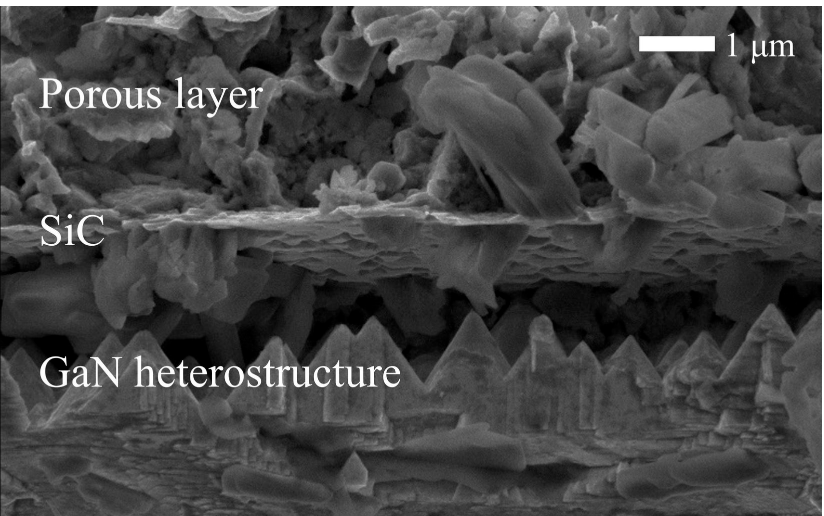
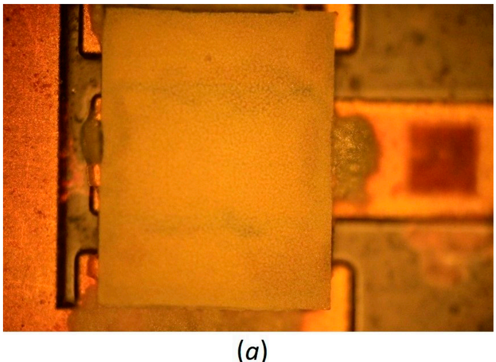



**Figure 9.** SEM image of the substrate-heterostructure interface after etching in KOH (40%)/$C_2H_6O$ (10%) solution.

However, such etching can lead to undesirable thinning of the heterostructure, necessitating an adjustment of its design to prevent etching of the active region. As a result, the use of a three-component mixture of hydrogen peroxide and hydrofluoric acid solution, H2O2:HF = 1:1, with the addition of several drops of Br, resulted in the effective removal of the bulk portion of the Si substrate. To separate the silicon substrate, it is sufficient to etch a thin layer of silicon bordering the porous layer composed of elongated crystallites of silicon carbide. Due to the developed surface of the silicon/silicon carbide interface, etching in this area is faster than the bulk material, resulting in the removed part of the silicon substrate remaining virtually intact. This approach is more cost-effective since it requires fewer reagents to remove the substrate. In turn, the smaller amount of reaction products accomplish methodological superiority regarding environmental safety.

Figure 10 displays images of chips located on the submount after the removal of the silicon part of the SiC/Si substrate, obtained using both optical and scanning electron microscopes. The acquired images indicate the absence of chips, cracks, or other damages resulting from the process of laser removal of sapphire substrates wherein abrupt release of gaseous nitrogen from the decomposition of GaN material at the interface with the substrate occurs under the influence of a powerful nanosecond pulse of laser radiation. Furthermore, when the growth substrate is removed, the heterostructure grown on a hybrid substrate displays less deformation from the relaxation of residual stresses compared to structures grown on sapphire substrates.



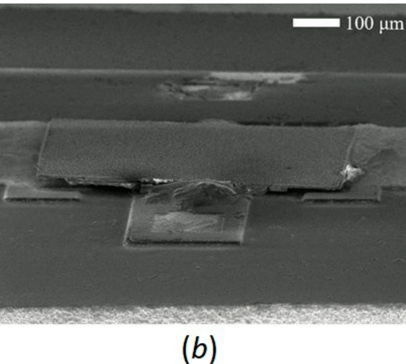




**Figure 10.** View of LED chip with removed silicon substrate: (**a**) in an optical microscope, (**b**) in an electron microscope.

The second advantage of using hybrid substrates with a SiC layer thicker than 200 nm, as demonstrated in the manufacture of TFFC, is the presence of a porous layer consisting of crystallites of silicon carbide with characteristic sizes ranging in the hundreds of nanometers, creating structures with complex shapes. Figure 11 displays an SEM image of the chip after removing the silicon portion of the substrate, with higher magnification applied. The porous layer's overall thickness is several microns, and since the silicon etching occurred at the layer of the interface, it contains no silicon wafer remnants and is transparent to visible radiation. This layer covers the entire chip surface exposed after removing the silicon part of the substrate. Given that the dimensions of the components that make up the layer are comparable to or greater than the LED's wavelength of radiation, the surface scatters light at the chip-environment interface, promoting the light from the heterostructure. As a result, once the substrate is eliminated, there is no requirement for additional topography to combat total internal reflection in the heterostructure waveguide, guaranteeing that the chip does not necessitate further modifications. Consequently, the porous layer's presence eliminates the expense and time required for heterostructure etching, which is typical for chips on sapphire substrates. Moreover, this method helps prevent damage to the heterostructure's active region and unwanted leakage, which, as previously discussed, could be caused by etching while also obviating the modification of the heterostructure's thickness and design.

The chips produced in the experiments, including face-up and flip-chip designs, exhibited stable luminescence. The primary electro-optical features of one of the encapsulated LEDs of the face-up design are shown in Figure 12. The completed LED's appearance is depicted in Figure 13a. Furthermore, to demonstrate the LEDs' capability for emitting white light, a phosphor-containing polymer lens covered the LEDs. Figure 13b exhibits the ability to generate white light using this method.

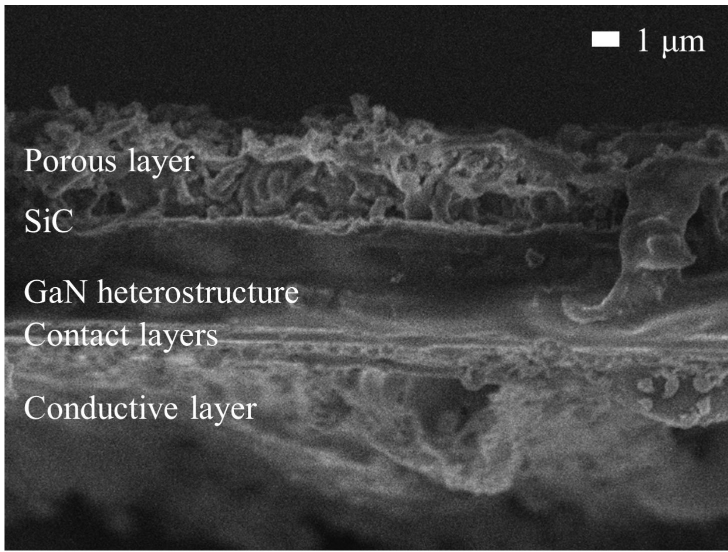



**Figure 11.** SEM image of the LED chip with the removed part of the silicon substrate, side view.

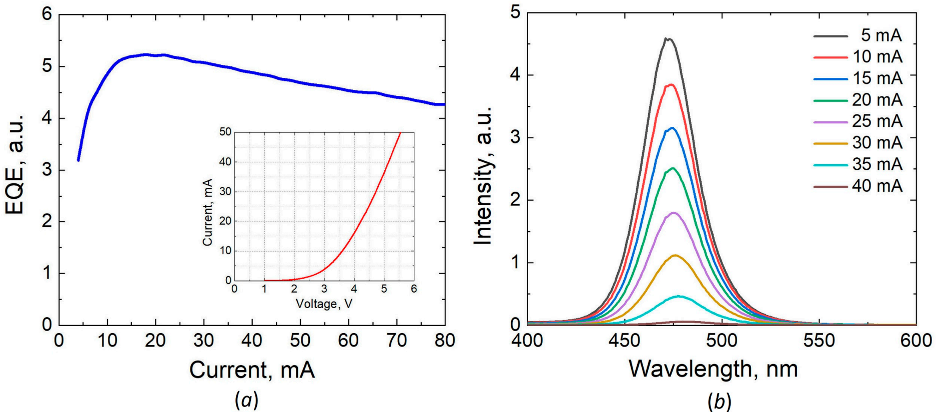



**Figure 12.** Dependence of the external quantum efficiency (EQE) on the value of current (the tab shows the volt-ampere characteristic) (**a**), spectra of intrinsic emission at different values of current (**b**) for one of the fabricated LEDs.

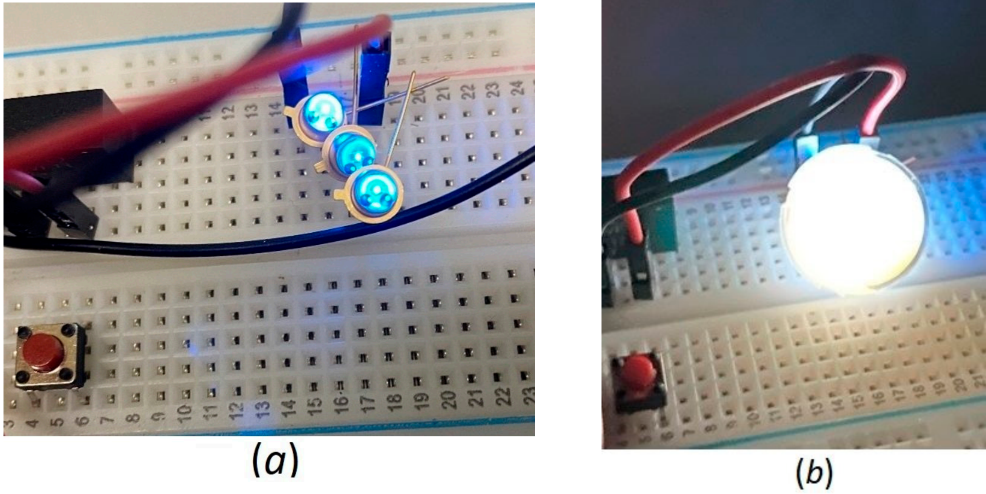



**Figure 13.** The appearance of the finished LED: three LEDs without phosphor coating **(a)** and an LED with a polymer lens containing phosphor in its composition **(b)**.

## 5. Conclusions

In summary, this study details the fabrication of AlInGaN heterostructures on novel SiC/Si substrates obtained via the method of coordinated substitution of atoms (MCSA) from silicon substrates. LEDs with chips of two distinct configurations were manufactured, and in both cases, the method presented several advantages compared to conventional sapphire and silicon substrate production technologies, particularly in relation to the SiC-Si interface formed during the SiC substrate layer's growth stage. When producing face up chips, substrates with a 100 nm thick SiC layer were utilized. The growth pores found at the SiC/Si interphase have a beneficial effect by scattering and increasing the reflection of the LED's self-radiation at this interphase. It is common knowledge that an opaque and absorbing substrate in LEDs on silicon substrates must be removed. However, pore geometry and density optimization during hybrid substrate manufacturing can produce an acceptable value of LED quantum efficiency without resorting to substrate removal. Consequently, eliminating substrate removal from the LED production process would result in a cost-effective chip production with an optimal price-quality ratio.

Flip-chip LEDs with removed substrate were produced from heterostructures grown on hybrid substrates with a 400 nm thick SiC layer. The porous layer comprising SiC crystallites was created during SiC layer growth in hybrid substrates with this thickness, simplifying the separation of the opaque silicon substrate and making it more cost-effective and environmentally friendly. Additionally, the presence of SiC crystallites on the liberated chip surface eliminates the expensive and time-consuming process of creating light-emitting surfaces at the outer interface of the heterostructure. The use of hybrid SiC/Si substrates introduces fundamentally new approaches to TFFC fabrication, demonstrating several advantages compared to conventional technologies for such chip production. These new approaches can be adapted to develop a technological process for constructing efficient LEDs, including micro-LEDs. Nonetheless, the optimization of numerous technological operations used in their production is necessary to achieve maximum quantum efficiency values for these devices.

In conclusion, we present Table 1, which shows some of the properties of SiC/Si hybrid substrates grown by the MCSA and VMCSA methods for LEDs and their comparison with the properties of sapphire substrates.

**Table 1.** Properties of SiC/Si hybrid substrates.

| Substrate Type | SiC Polytype | Orientation | Thicknesses of SiC Layers, nm | Specific Thermal Conductivity at 300 K, W/cm K | Mohs Hardness | Scattering Relief on the Interface |
|---|---|---|---|---|---|---|
| Sapphire | — | (0001) | — | 0.23 \| \| c-axis | 9 | Relief is artificially created on a substrate |
| | — | $(10\bar{1}0)$ | — | 0.25 \| \| a-axis | 9.5 | |
| SiC/Si, MCSA | 3C-SiC | (111) | 10–100 | 1.56 | 7 | Formed naturally in the process of synthesis |
| SiC/Si, VMCSA, not separated from Si | 3C-SiC | (111) | 300–500 | 1.49 | 7 | Formed naturally in the process of synthesis |
| SiC/Si, VMCSA, separated from Si | 3C-SiC | (111) | 500–1000 | 3.6 | — | Formed naturally in the process of synthesis |

## 6. Patents

There are two patents resulting from the work reported in this manuscript.

1. Grashchenko, A.S.; Kukushkin, S.A.; Markov, L.K.; Nikolaev, A.E.; Osipov, A.V.; Pavlyuchenko, A.S.; Sviatets, G.V.; Smirnova, I.P.; Tsatsulnikov, A.F. Light-emitting diode on silicon substrate. Patent RF: No. 2755933. Publ. 1 February 2021; bul. No. 27 (In Russ).
2. Grashchenko, A.S.; Kukushkin, S.A.; Osipov, A.V.; Redkov, A.V. Functional element of a semiconductor device and method of its manufacture. Patent RF: No. 2787939. Publ. 11 April 2022; bul. No. 2 (In Russ).

**Author Contributions:** Conceptualization, S.A.K., A.V.O., L.K.M. and A.F.T.; methodology, L.K.M. and A.F.T.; investigation, A.S.G., A.V.O., L.K.M., A.S.P., I.P.S., A.E.N. and A.V.S.; writing—original draft preparation, S.A.K., A.V.O., L.K.M. and A.F.T.; writing—review and editing, S.A.K. and A.V.O.; supervision, S.A.K.; funding acquisition, G.V.S. All authors have read and agreed to the published version of the manuscript.

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