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Surrogate Assisted Optimization for Low-Voltage Low-Power Circuit Design

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Abstract: Low-voltage low-power (LVLP) circuit design and optimization is a hard and time-consuming task. In this study, we are interested in the application of the newly proposed meta-modelling technique to alleviate such burdens. Kriging-based surrogate models of circuits' performances were constructed and then used within a metaheuristic-based optimization kernel in order to maximize the circuits' sizing. The JAYA algorithm was used for this purpose. Three topologies of CMOS current conveyors (CCII) were considered to showcase the proposed approach. The achieved performances were compared to those obtained using conventional LVLP circuit sizing techniques, and we show that our approach offers interesting results.

Keywords: LVLP; CCII; surrogate modeling; kriging models; JAYA; PSO; Wilcoxon Signed-Rank Test

1. Introduction

Low-power low-voltage (LVLP) circuits are of paramount importance in analog, mixed-signal and radiofrequency (AMS/RF) systems. Decreasing voltage supply and reducing power consumption is a real challenge for AMS/RF applications [1–8]. As examples, we can mention the fact that such circuits can overcome some classical circuit limitations, such as the gain-bandwidth (GBW) product limitation [1], and they are also very necessary due to ceaseless technology scaling. However, such circuit design is complex, tedious and very time consuming.

MOSFETs operating in weak inversion mode have been largely considered to implement low power circuits [9]. LVLP current conveyors have been used in many electronic applications [10], such as sensor interfaces [10], inductance simulation [11], oscillators [12] and filters [3,13], among others. However, and as aforementioned, the complexity of such designs and the impact of technology variations in analog integrated circuits operating in weak inversion have pushed (and continue to push) engineers, designers and researchers to develop computer-aided design (CAD) tools for automating this process as much as possible [9,14]. Two main approaches have been used so far: (i) the so-called knowledge-based technique [9], which is very time consuming and mainly depends on the experience of the skilled designer; (ii) the optimization-based design, which consists of using an optimization algorithm for optimally sizing the considered circuit/system [9]. Two evaluation approaches can be used. The first considers the symbolic equations of the circuit/system performances/constraints [15–17]. This approach is known to be rapid but lacks accuracy. The second approach is the in-loop based approach, also called the simulation-based technique [18–21]. It consists of making the appeal to use an electric simulator as an evaluator. In this way, accurate results can be obtained; however, the approach is time consuming due to the number of calls to the simulator.

A few years ago, a new modeling technique, (i.e., surrogate modeling) was proposed in the mathematical literature. The technique is also called "metamodeling". In short, the approach consists of generating accurate performance models that can be rapidly evaluated. In other words, this new technique offers advantages of both conventional approaches: accuracy and rapid evaluation. Different variants of metamodeling approaches are nowadays available in the literature, such as the regression method [22], the Kriging model [23], and the radial basis function (RBF) [24]. Surrogate modeling has already been adopted in the electronic domain (see, for instance, [25–27]). In a previous work [21], the authors used the RBF model combined with particle swarm optimization (PSO) to optimize the performances of CMOS analog circuits.

In this work, the Kriging model was applied to the accurate modeling of the main parasitic error source (the X-port input resistance (Rx)) of second-generation current conveyors (CCIIs) operating in weak inversion under different biases. Constructed models were used within a metaheuristic-based optimization kernel for minimizing the aforementioned parasitic source. The newly proposed Jaya algorithm was considered [28,29].

The rest of this paper is organized into four sections. In Section 2, an overview on the metamodeling techniques is offered. The considered metaheuristic-based algorithms are detailed in Section 3. Section 4 presents the considered applications and highlights the achieved results. Finally, conclusions are offered in Section 5.

2. Metamodeling Technique: An Overview

Surrogate modeling is a newly conceived interpolation technique for the efficient approximation of linear and non-linear functions [25]. Many variants have been considered and introduced in the specialized literature, such as the regression method [22], the Kriging method [23] and the RBF method [24]. The main objective of this technique is to approximate complex non-linear functions with an accurate and simple model [25–27]. This technique has already been used in a broad range of engineering applications, such as in geostatistics [26], electronic circuits [27,30,31], and electromagnetic devices [25,32–34].

The construction of surrogate models requires three main steps: design sampling, function evaluation, and model construction, as shown in Figure 1.

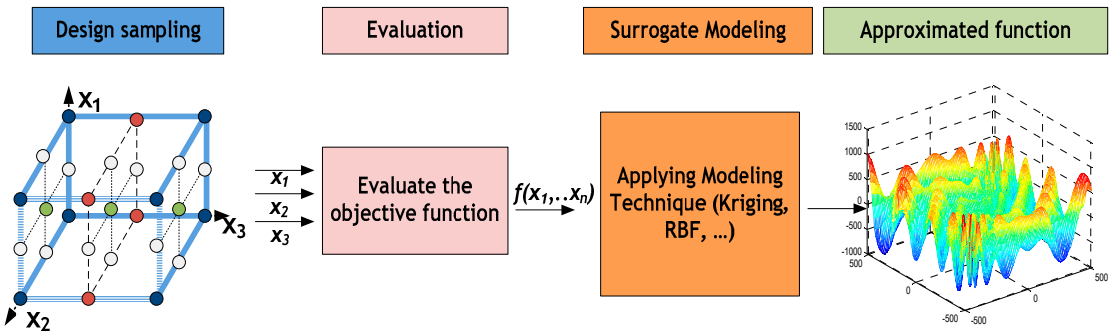

Figure 1. Steps to construct surrogate models.

In this work, we consider the Kriging technique which uses the interpolation function $Y(x)$, represented as follows [25–27]:

$$Y(x) = \sum_{j=1}^{N} \beta_j f_j(x) + Z(x) \quad (1)$$

where N is the number of sample points, $f_j(x)$ represents the j^{th} regression function model, β_j is the corresponding weighting coefficient, and $Z(x)$ is a stochastic process. The latter has a mean value equal to zero, and the covariance between two sampling points, x_i and x_j, is expressed as in [25–27]:

$$Cov(Z(x_i), Z(x_j)) = \sigma^2 R(R(\theta, x_i, x_j))i, j = 1 \ldots\ldots.., N \quad (2)$$

where σ^2 is the variance coefficient of $Z(x)$ and $R(\theta,x_i,x_j)$ is the correlation function.

The exponential correlation function, based on the Kriging technique, is considered in this work.

3. The Optimization Kernel

It has already been shown that analog circuit sizing/optimization can be considered as a hard problem to overcome [35–37]. Metaheuristics bid interesting solutions to solve such problems that can be formulated as presented in Equation (3). A plethora of metaheuristics have already been used for sizing AMS/RF circuits and systems, such as Genetic Algorithms (GA) [38], Ant Colony Optimization (ACO) [39], Bacterial Foraging Optimization (BFO) [40], Firefly Optimization (FFO) [41] and Simulated Annealing (SA) [42], to name a few. Among these metaheuristics, PSO [43] has been widely used due to the fact that it is robust, rapid and easy to be implemented. However, similar to most other metaheuristics, weighting coefficients (constriction and inertia) have to be fixed by the user for the metaheuristic tradeoff between exploration and intensification. This highly depends on the experience of the designer and the handled problem itself. Recently, a new metaheuristic has been proposed in the specialized literature which does not need any a prior coefficients to be fixed, it is called the JAYA algorithm [29], and it is applied herein as the optimization algorithm. A comparison with PSO will be performed to argue this choice. In the subsections below, we respectively present a brief overview of PSO and the details regarding the JAYA algorithm.

$$\begin{cases} Maximize\ or\ Minimize\ f(x) \\ \\ Subject\ to\ h_k(x) \leq 0,\ k = 1 \ldots m \end{cases} \quad (3)$$

where $x = (x_1, \ldots, x_n) \in X$, $X \subset \mathfrak{R}^n$ is the decision space for the variables, $f(x_i)$: $\mathfrak{R}^n \longrightarrow \mathfrak{R}$, is the objective function and $h_k(x) \leq 0$, $k = 1 \ldots m$ is a set of constraints that limit the values of the variables.

3.1. The Particle Swarm Optimization Algorithm

The Particle Swarm Optimization (PSO) algorithm is widely used in the literature, since it is a simple, robust and rapid metaheuristic. It is inspired by the social behavior of animals, namely fishes and birds [16,43,44]. Its mechanism works on updating each particle velocity and position at each iteration, according to the following equations:

$$\vec{v}_i(t+1) = \left| \begin{array}{l} \omega \vec{v}_i(t) \\ +c_1 rand(0,1)(\vec{x_{Pbesti}}(t) - \vec{x_i}(t)) \\ +c_2 rand(0,1)(\vec{x_{Gbesti}}(t) - \vec{x_i}(t)) \end{array} \right. \quad (4)$$

$$\vec{x}_i(t+1) = \vec{x}_i(t) + \vec{v}_i(t) \quad (5)$$

With x_{Pbest} is the best position, x_{Gbest} is the global best position, w is the inertia weight of the particle, and c_1 and c_2 are the construction parameters.

Figure 2 shows a flowchart of the PSO algorithm [43].

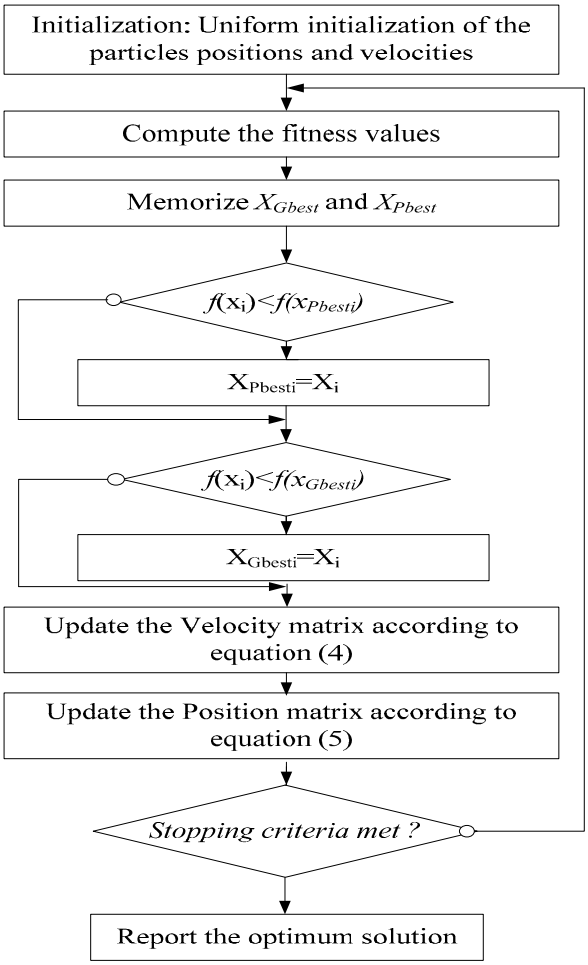

Figure 2. The PSO algorithm flowchart.

3.2. The JAYA Algorithm

Evolutionary algorithms (EA), such as GA and swarm intelligence (SI) based algorithms, such as PSO, need specific parameters to be fixed, such as mutation probability and crossover probability for GA, inertia weight and cognitive social parameters for PSO. In this context and in order to avoid such a rule-of-thumb-based approach for fixing values of such weighting parameters, a new metaheuristic, inspired from the teaching-learning-based optimization (TLBO), was proposed, as detailed in [29,45–48]. TLBO works according to two phases (teacher phase and learner phase) [48]. On the other hand, the JAYA algorithm encompasses only a unique phase [29]. Both algorithms require only common control parameters (population size and iteration number). It is comparatively much simpler to apply than conventional metaheuristics [29,44,45].

The JAYA algorithm mechanism works on updating each solution at each iteration, according to the following equations:

$$X\prime_{j,k,i} = \left| \begin{array}{l} X_{j,k,i} \\ +r_{1,j,i}(X_{j,best,i} - \left|X_{j,k,i}\right|)Term1 \\ -r_{2,j,i}(X_{j,worst,i} - \left|X_{j,k,i}\right|)Term2 \end{array} \right. \quad (6)$$

where i is the number of iterations, $K = 1,2, \ldots n$, n is the number of candidate solutions, $J = 1,2, \ldots m$, m is the number of design variables, $X_{j,best,i}$ is the value of the variable j for the best candidate and $X_{j,\,worst,i}$ is the value of the variable j for the worst candidate. $X'_{j,k,i}$ is the update value of $X_{j,k,I}$ and $[r_{1,j,i}, r_{2,j,i}]$ are the random numbers for the j^{th} variable during the i^{th} iteration and varies between [0, 1]. Term 1 in Equation (6) specifies the trend of the solution to move closer to the best solution, whereas

Term 2 specifies the trend of the solution to avoid the worst solution. $X'_{j,k,i}$ is accepted if it gives a better function value. At the end of the iteration, all the accepted function values have been used as inputs to the next iteration.

Figure 3 shows the flowchart of the JAYA algorithm [29].

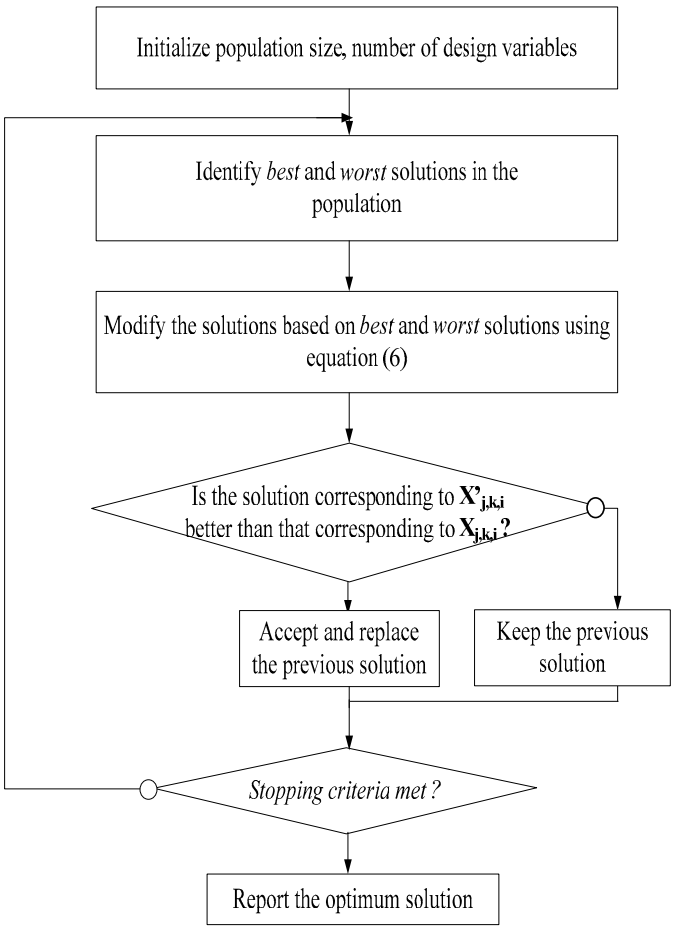

Figure 3. The JAYA algorithm flowchart.

4. The Proposed Approach and Application Examples

Current conveyors are used as basic building blocks for the synthesis of analog circuits and systems. Due to their flexibility, the CCIIs operating in weak inversion are utilized in different applications [11], especially in high frequency circuits, sensor interfaces, filters and mobile communication applications [11]. A CCII is composed of two input ports (X and Y) and one output port (Z). The behavior of an ideal CCII can be summarized as follows [9–12], where positive (CCII+) and negative (CCII-) current conveyors are obtained for $a = 1$ and $a = -1$ [12], respectively:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (7)$$

Parasitic input resistance (Rx) at port X can greatly affect the performances of the current conveyor and has to be minimized [49].

In the following section, we deal with modeling and then minimizing the aforementioned performances (i.e., Rx) of CMOS current conveyors operating in the weak inversion mode. For the sake of comparison, three different topologies are considered, namely, a class AB CCII+, a differential-based

Class AB CCII and an OTA-based CCII+. These circuits have already been considered in [9] and [49] and have been sized/optimized for operating in the weak inversion mode.

4.1. The Proposed Approach

The proposed approach consisted of generating a model of the Rx performance of each of the three topologies of CMOS CCIIs operating in weak inversion using the Kriging technique, then, using the JAYA algorithm, minimizing the corresponding value.

Initially, a database was generated using the Latin hypercube sampling (LHS) technique [50]. Four variables were considered (i.e., the channel widths and the channel lengths of the MOS transistors). For comparison with [9] and [49], we considered that all NMOS transistors' channels have the same widths (Wn) and the same lengths (Ln). Ditto for PMOS transistors. This database was used as an input for the Kriging modeling technique. This database consisted of the geometric variables of the considered circuits. In total, 1200 samples were considered. The HSPICE simulator was used to evaluate these samples. The simulations were performed using Level 49 standard CMOS technology of 0.35 µm, where transistors operate in the weak inversion mode. The model was constructed using the Kriging technique with the exponential correlation function. A second database, consisting of 100 test samples and their performance evaluated by the Hspice simulator, was used to validate the model. The relative error metric was considered to check the accuracy of the constructed models and its equation is given by (8), where *yi* and *Yi* are the simulated and the estimated (modeled) performance values, respectively. *N* is the number of sample points.

$$Relative\_Error = \frac{1}{N}\sum_{i=1}^{N}\frac{y_i - Y_i}{y_i} \tag{8}$$

4.2. Application 1: A Class AB CMOS CCII+

The considered circuit [49] is shown in Figure 4. The objective was to model the parasitic X-port resistance for different bias current (I_{bias}) values: 15 µA, 20 µA, 26 µA, 30 µA and 45 µA. The voltage power supply was $V_{dd}/V_{ss} = \pm 1$ V. Five models were constructed and validated. Table 1 gives the relative error of the model created for the different bias currents of the class AB CMOS CCII+, where the accuracy of the constructed models can be easily interpreted.

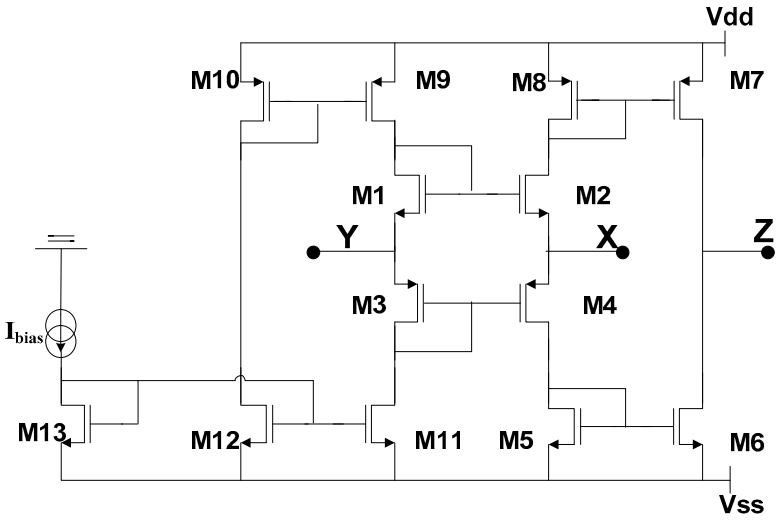

Figure 4. A class AB CMOS CCII+.

Table 1. Relative Error of the class AB CMOS CCII+.

I_{biais} (µA)	Relative Error (%)
15	0.042
20	0.046
26	0.005
30	0.007
45	0.009

Subsequently, the constructed models were used within a metaheuristic-based optimization routine. The JAYA algorithm was used, as aforementioned. The obtained results were compared to those of [9,49], where the in-loop optimization technique is used. Further, and in order to highlight the JAYA algorithm performances, optimization using the PSO technique was also carried out for comparison regarding accuracy, rapidity and robustness.

Table 2 presents the optimization results obtained using the constructed Kriging-based models as performance evaluators within the JAYA and PSO–based optimization kernel (denoted as Kriging-PSO and Kriging-JAYA, respectively). Hspice simulations were performed for evaluating the relative error.

Table 2. Results of the Rx performances of the Class AB CMOS CCII+.

	I_{biais} (µA)	Ln (µm)	Wn (µm)	Lp (µm)	Wp (µm)	Optimized Rx (Ω)	Simulated Rx (Ω)	Relative Error (%)
Kriging-PSO	15	0.746	318.810	0.644	499.340	1242.500	1240.800	0.137
	20	0.751	324.456	0.641	498.337	962.780	960.070	0.282
	26	0.834	276.812	0.689	500.000	764.250	765.820	0.205
	30	0.746	318.629	0.644	499.351	673.974	673.470	0.074
	45	0.503	453.117	0.546	497.754	476.360	476.350	0.002
Kriging-Jaya	15	0.663	499.910	0.665	500.000	1211.400	1208.000	0.281
	20	0.681	496.242	0.667	500.000	936.972	934.490	0.265
	26	0.713	498.740	0.665	500.000	743.120	741.480	0.221
	30	0.715	499.375	0.664	500.000	655.792	654.434	0.207
	45	0.714	500.000	0.664	500.000	463.960	462.938	0.220

Figure 5 shows a comparison between the Hspice simulations of Rx performances obtained via Kriging-PSO and Kriging-Jaya for I_{bias} = 26 µA. (In order to not overload the paper, a unique case is presented.)

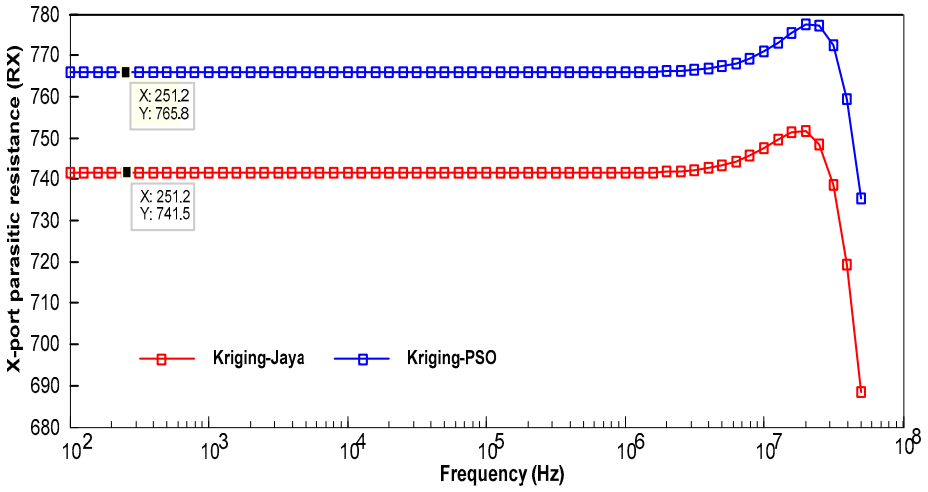

Figure 5. HSPICE simulations of Rx of Class AB CMOS CCII+: Kriging-PSO vs. Kriging-Jaya (I_{bias} = 26 µA).

Figure 6 gives a whisker boxplot relative to 50 executions of the Kriging-PSO and Kriging-Jaya of Rx performances.

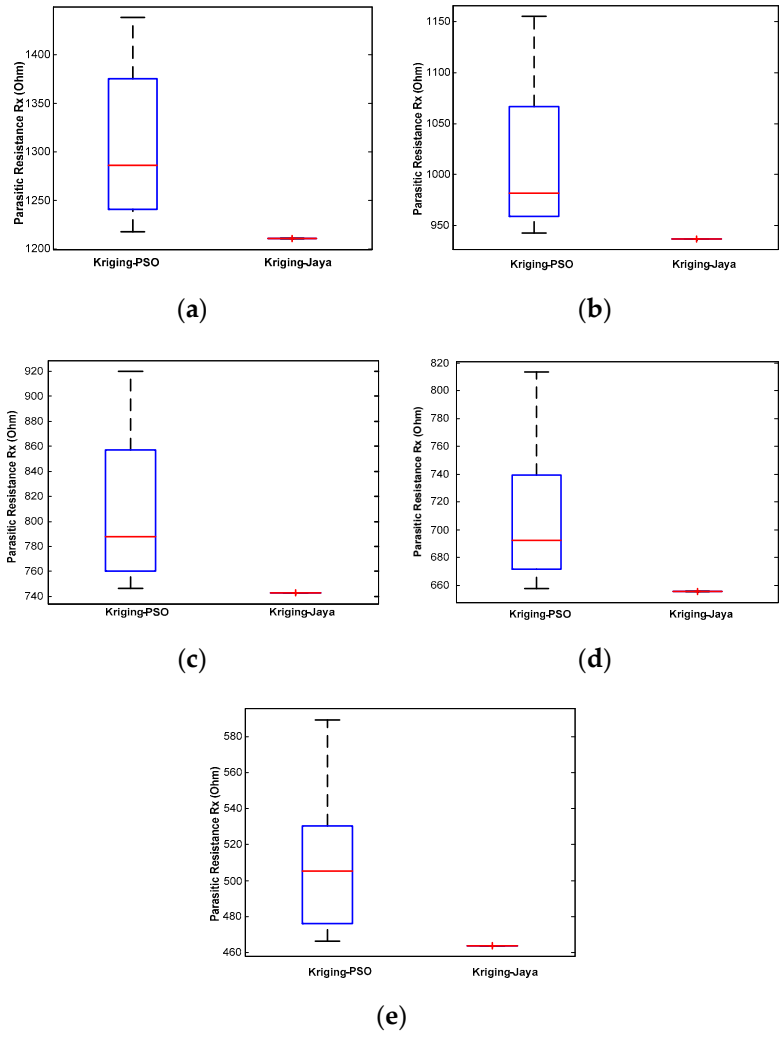

Figure 6. Boxplot of the 50 execution results for Kriging-PSO and Kriging-Jaya regarding Rx performances of the Class AB CMOS CCII+. I_{bias} = (**a**) 15 µA, (**b**) 20 µA, (**c**) 26 µA, (**d**) 30 µA, (**e**) 45 µA.

4.3. Application 2: A Differential-Based Class AB CMOS CCII

The schematic of the considered differential-based class AB CMOS CCII [49] is shown in Figure 7. Similar to Application 1, the objective was to model and then minimize the parasitic X-port resistance in different bias current (I_{bias}) values: 100 nA, 250 nA, 1 µA and 10 µA. To this end, four models were constructed and validated. The same sizes for both databases were considered. The voltage power supply was V_{dd}/V_{ss} = ± 0.6 V.

Table 3 shows the relative errors of the models constructed for different bias currents, and Table 4 summarizes the Kriging-PSO, the Kriging-Jaya and the Hspice simulation results for the four cases of the bias current.

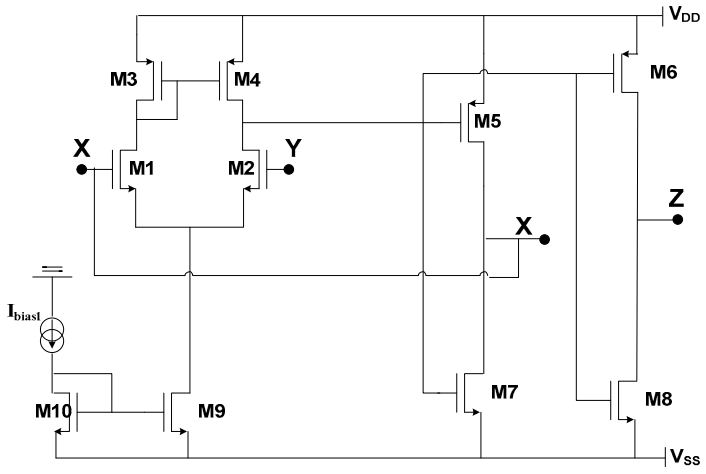

Figure 7. Differential-based class AB CMOS CCII.

Table 3. Relative Error of the differential-based Class AB CMOS CCII.

I_{biais} (µA)	Relative Error (%)
0.10	0.829
0.25	0.386
1	0.092
10	0.007

Figure 8 shows a comparison between the Hspice simulations of Rx obtained via the Kriging-PSO and Kriging-Jaya techniques, and Figure 9 gives a boxplot relative to 50 executions of the Kriging-PSO and Kriging-Jaya approaches.

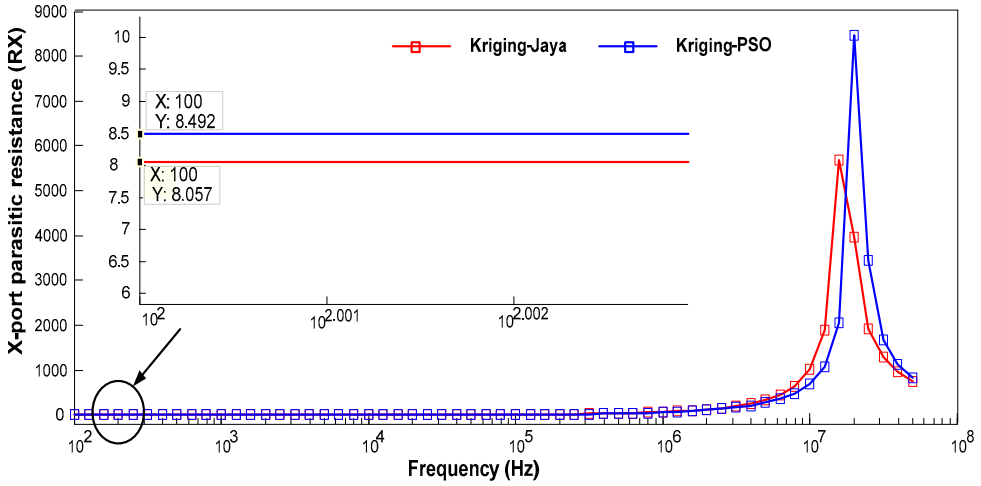

Figure 8. HSPICE simulation of Rx of the differential-based class AB CMOS CCII: Kriging-PSO vs. Kriging-Jaya (I_{bias} = 10 µA).

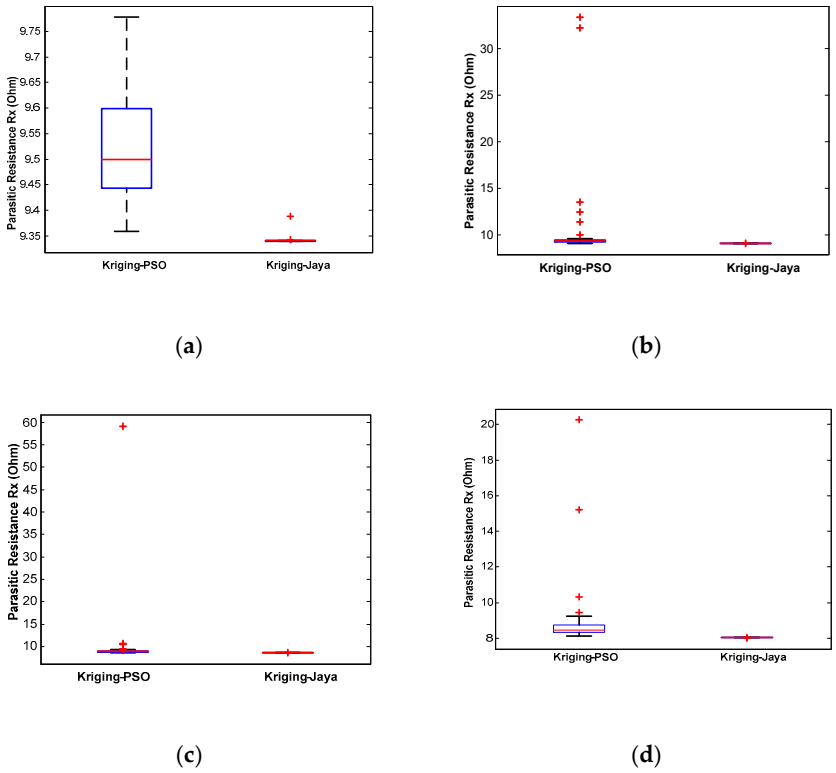

Figure 9. Boxplot of the 50 execution results for Kriging-PSO and Kriging-Jaya regarding Rx performances of the differential-based class AB CMOS CCII. I_{bias} = (**a**) 100 nA, (**b**) 250 nA, (**c**) 1 µA, (**d**) 10 µA.

Table 4. Obtained results for the Rx performance of the differential-based class AB CMOS CCII.

	I_{biais} (µA)	Ln (µm)	Wn (µm)	Lp (µm)	Wp (µm)	Optimized Rx (Ω)	Simulated Rx (Ω)	Relative Error (%)
Kriging-PSO	0.10	693.521	31.530	848.132	746.120	9.265	9.487	2.340
	0.25	444.361	32.237	769.656	261.891	9.946	10.084	1.360
	1	283.484	30.710	832.148	124.233	9.037	8.953	0.930
	10	498.060	31.583	824.740	276.939	8.530	8.492	0.450
Kriging-JAYA	0.10	99.160	35.000	849.576	474.915	9.340	9.377	0.400
	0.25	562.035	26.702	849.958	451.720	9.093	9.088	0.050
	1	648.526	33.385	849.958	49.618	8.662	8.750	1.000
	10	850.000	27.006	849.958	48.875	8.050	8.057	0.090

4.4. Application 3: An CMOS OTA-Based CCII+

A CMOS OTA-based CCII+ [49] is shown is Figure 10. In this application, the objective was to model and minimize the parasitic X-port resistance for different bias current (I_{bias2}) values: 500 nA, 1 µA, 10 µA and 30 µA, where I_{bias1} = 3 µA. Four models were constructed and validated, as shown in Table 5. The voltage power supply was V_{dd}/V_{ss} = ±1V. The obtained optimization results corresponding to the application of the Kriging model as an evaluator within the Jaya/PSO sizing kernel are given in Table 6. A comparison with the results given in [9,49] is also provided.

Table 5. Relative Error of the CMOS OTA based CCII+.

I_{biais2} (µA)	Relative Error (%)
0.5	0.365
1	0.366
10	0.507
30	0.378

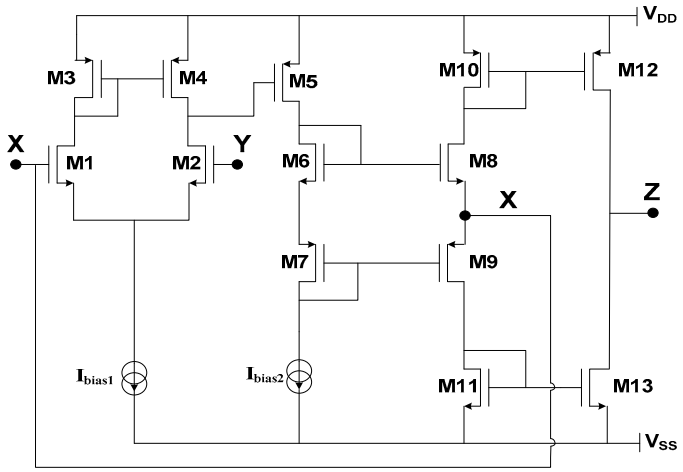

Figure 10. A CMOS OTA based CCII+.

Figure 11 shows the Rx Hspice simulations corresponding to the sizing obtained by the application of the Kriging-PSO and Kriging-JAYA approaches for I_{bias2} = 10 µA. Figure 12 gives boxplots relative to 50 applications of the Kriging-PSO and Kriging-Jaya approaches.

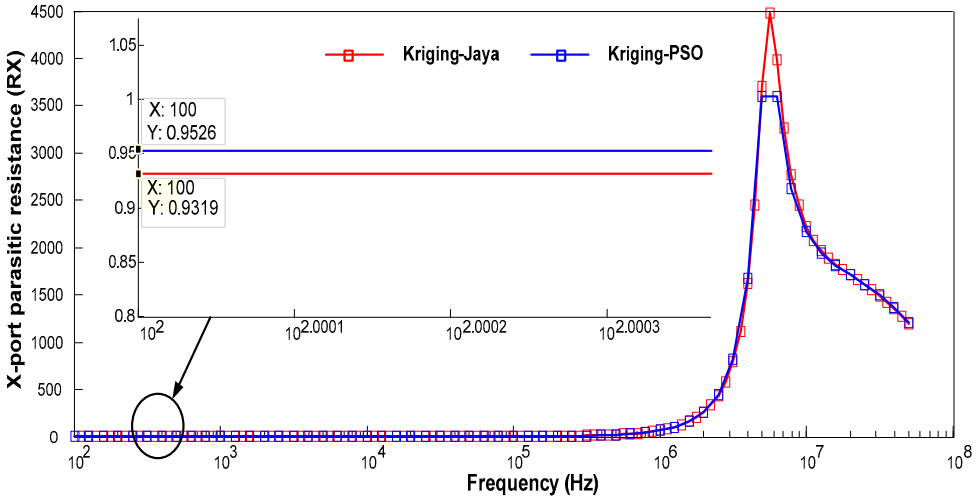

Figure 11. HSPICE simulation of Rx of CMOS OTA based CCII+: Kriging-PSO vs. Kriging-JAYA (I_{bias2} = 10 µA).

Table 6. Obtained results for the Rx performances of the CMOS OTA based CCII+.

	I_{biais2} (µA)	Ln (µm)	Wn (µm)	Lp (µm)	Wp (µm)	Optimized Rx (Ω)	Simulated Rx (Ω)	Relative Error (%)
Kriging-PSO	0.5	385.211	13.468	377.879	401.654	15.000	15.007	0.047
	1	333.942	11.767	360.872	365.650	7.817	7.802	0.191
	10	402.660	17.227	418.236	417.988	0.947	0.952	0.493
	30	437.826	11.018	403.388	371.282	0.367	0.369	0.515
Kriging-JAYA	0.5	356.367	11.297	440.913	404.515	14.802	14.830	0.189
	1	347.074	11.384	441.399	422.708	7.681	7.698	0.220
	10	343.585	11.572	448.640	417.206	0.928	0.932	0.429
	30	356.406	11.419	443.569	411.998	0.362	0.364	0.549

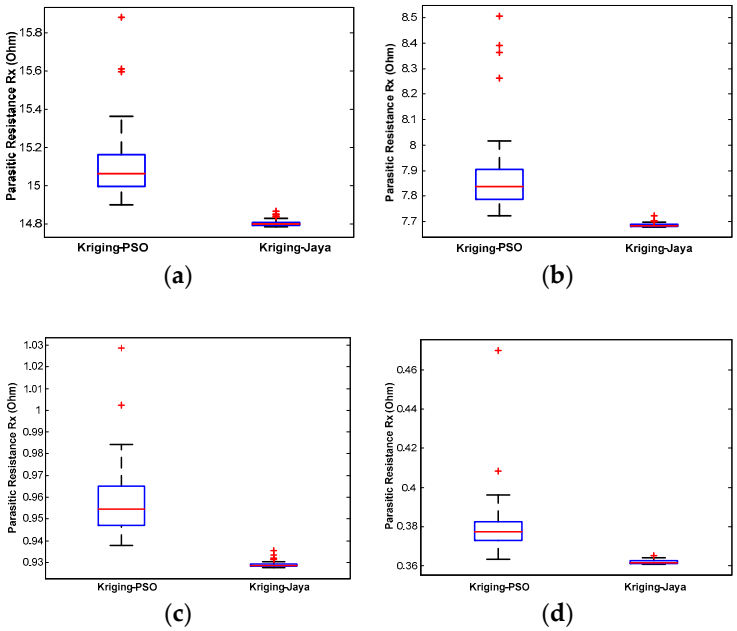

Figure 12. Boxplot of the 50 execution results for Kriging-PSO and Kriging-Jaya regarding Rx performances of CMOS OTA based CCII+. I_{bias2} = (**a**) 500 nA, (**b**) 1 µA, (**c**) 10 µA, (**d**) 30 µA.

5. Comparisons and Discussion

Tables 1, 3 and 5 show the viability of the proposed modeling technique.

For comparison, the same circuits, as well as the same simulation conditions and the same operating mode adopted in [9] and [49], were considered. The same technology in [9], and the same bias conditions in [9] and [49] were adopted. Table 7 summarizes the results obtained using the constructed models within a PSO and a JAYA-based optimization kernel. The proposed approach allows for the same performances as when adopting the conventional in-loop technique but within a much-reduced computing time, as shown in see Table 7. It is to be mentioned that model generation and training takes approximately ten minutes. However, this is performed only once. Then, the model is used as it is within sizing/optimization loops, where its evaluation takes a couple of seconds. On the contrary, when using a simulator-based technique, each time the corresponding approach restarts from scratch.

Table 7. Rx values (for the three circuits) obtained by different approaches.

	I_{bias}	V_{dd}/V_{ss}	Kriging-PSO	Kriging-JAYA	[9]	[49]
Application #1	26 µA	± 1 V	765.82 Ω	741.48 Ω	725.00 Ω	990.00 Ω
Application #2	10 µA	± 0.6 V	8.50 Ω	8.06 Ω	8.50 Ω	12.00 Ω
Application #3	10 µA	± 1 V	0.95 Ω	0.93 Ω	0.90 Ω	1.30 Ω
Computation Time (s)	–	–	3.69	3.88	400.00	–

It is worth mentioning that the proposed Kriging-based optimization technique is more suitable for integration within a CAD tool, since it allows the computation time to be reduced approximately 100-fold.

Tables 2, 4 and 6 show that the JAYA algorithm performs results as accurate as those obtained using the well-known PSO metaheuristic. On the other hand, the robustness tests shown in Figures 6, 9 and 12, which were performed due to the intrinsic stochastic aspect of the metaheuristics, prove that JAYA is more robust than PSO. In order to further compare both metaheuristics, the Wilcoxon Signed-Rank Test [51] was preformed, with the statistical significance value a = 0.05, for 50 runs. Table 8 summarizes the obtained results where it is clear that, for the three cases, the JAYA algorithm's statistical performances outperform those of PSO.

Table 8. The results of the Wilcoxon Signed-Rank Test for the three CCII+ circuits.

JAYA vs. PSO	*p*-Value	T+	T-	Winner
Application #1	7.5569×10^{-10}	0	50	**Jaya**
Application #2	7.5569×10^{-10}	0	50	**Jaya**
Application #3	7.5569×10^{-10}	0	50	**Jaya**

It is to be mentioned that the null hypothesis is considered for the Wilcoxon Signed-Rank test. For comparing both of the metaheuristics' performances, the alternative hypothesis was valid, and the ranks' sizes provided by the Wilcoxon test (i.e., T + and T- as defined in [51]) were examined.

6. Conclusions

It has been shown that Kriging-assisted JAYA-based LVLP circuit design offers an interesting approach that can be integrated within a CAD tool. This has been showcased via three CMOS current conveyors operating in the weak inversion mode. It has been shown that the proposed approach accurately models the performances of such circuits. Comparisons with Hspice simulations were performed for evaluating the accuracy of the established models. These models were then used as performance evaluators within an optimization kernel. The newly proposed JAYA algorithm was used for computing optimal parameters' values (mainly transistors' sizes). It has been shown that the JAYA algorithm, which does not need any predefined parameters, is much more robust than the PSO metaheuristic, while providing similar accurate performances.

The performances of the proposed approach have been compared to those proposed in the literature where the in-loop sizing technique is adopted. Comparable results have been obtained within a much-reduced computing time; an approximate 100-fold reduction.

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