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Power Management Circuits for Low-Power RF Energy Harvesters

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Abstract: The paper describes the design and implementation of power management circuits for RF energy harvesters suitable for integration in wireless sensor nodes. In particular, we report the power management circuits used to provide the voltage supply of an integrated temperature sensor with analog-to-digital converter. A DC-DC boost converter is used to transfer efficiently the energy harvested from a generic radio-frequency rectifier into a charge reservoir, whereas a linear regulator scales the voltage supply to a suitable value for a sensing and conversion circuit. Implemented in a 65 nm CMOS technology, the power management system achieves a measured overall efficiency of 20%, with an available power of 4.5 µW at the DC-DC converter input. The system can sustain a temperature measurement rate of one sample/s with an RF input power of −28 dBm, making it compatible with the power levels available in generic outdoor environments.

Keywords: RF energy harvester; low-power; CMOS; DC-DC converters; low-dropout regulators

1. Introduction

Energy Harvesting from the Electro-Magnetic (EM) field in the Ultra-High frequency (UHF) range is one of the most promising techniques that will further push the penetration of wireless sensor nodes (WSN) in several environments [1–4]. One the one hand, harvesting from RF sources requires neither movements, like in piezoelectric and mechanical harvesters, nor thermal gradients, like in thermo-electric harvesters that can limit the system lifetime and the harvesting efficiency. On the other hand, the large variability in space and time of the available EM power represents a significant challenge for the complete enabling of this source in the WSN scenario [5–8]. The front-end block of any RF harvester is the RF rectifier connected to the antenna terminals and used to perform the AC-to-DC power conversion [9]. Considering the large variability of the RF source, an energy reservoir is also usually included in the system to accumulate the collected energy. In the RF harvesting for WSN contest, a Power Management Unit (PMU) is mandatory to stock the energy harvested from the environment in the reservoir and also to supply the circuits of the sensor node. The main purposes of the PMU are the contemporary maximization of the amount of energy transferred from the antenna to the reservoir, and the proper and efficient regulation of the supply voltage of the sensor node from the harvested energy.

A PMU acting as interface between a generic RF rectifier and an integrated temperature sensor is presented in this paper. The system is composed by a DC-DC converter, for the optimization of the energy transfer from the output of the RF rectifier to the accumulator, and a low drop-out linear voltage regulator (LDO), for the generation of the voltage supply of the sensor. The former circuit is an input-driven boost converter specifically designed for intermittent energy sources and is thus well matched with the RF energy harvesting contest. The LDO, based on an integrated bandgap

reference and an operational amplifier, scales the voltage of the accumulator to a suitable value for the WSN circuits [10]. The control strategy sets the DC-DC input voltage, which corresponds to the output voltage of the rectifier. This feature, together with the extreme low power consumption of the whole PMU, allows the positive energy transfer to the reservoir for very low value of RF incoming power. Moreover, the adoption of this control strategy permits including in the system a Maximum Power Point Tracking circuit acting on the input voltage of the DC-DC converter, which is fundamental for the maximization of the collected energy from discontinuous energy sources [11]. The PMU and the temperature sensor were implemented in a test chip in 65 nm CMOS technology.

Measurement results demonstrate that the proposed PMU achieves a temperature measurement rate of 1 Sample/s, with an RF input power of -28.8 dBm, if interfaced to an RF rectifier featuring 30% of power efficiency [12,13], corresponding to 395 nW delivered to the DC-DC converter. Therefore, this PMU can be effectively used in the context of RF harvesting thanks to its inherent low power consumption and the suitable power efficiency.

This paper is organized as follows. In the next section, the generation of the voltage supply for an integrated sensor from the EM power is discussed, focusing both on the circuits composing the architecture of the PMU and on the fundamental equations. Measurement results on silicon samples in 65-nm CMOS technology are reported in Section 3.

2. System Description

The black-box schematic of a typical WSN with RF energy harvesting is shown in Figure 1. At the resonance frequency, the antenna is modeled with a lumped-elements circuit including a voltage source and a series resistance R_{ANT}. A matching network between the antenna and the input terminals of the harvester is mandatory to match the impedance of the two circuits and achieve the power matching condition. In the model of Figure 1, the matching reactance X_{ANT} is introduced in series with the input impedance of the harvester, Z_{IN}. The full and reactive power matching conditions at the center-band signal frequency f_0 are:

$$Full\ Power\ Matching \quad : \quad \Gamma_{IN}^{M}(f_0) = 0 \tag{1}$$

$$Reactive\ Matching \quad : \quad Im\left[\Gamma_{IN}^{M}(f_0)\right] = 0 \tag{2}$$

where Γ_{IN}^{M} is the reflection coefficient at the left terminal of the matching reactance X_{ANT}:

$$\Gamma_{IN}^{M} = \frac{Z_{IN} + j\,X_{ANT} - R_{ANT}}{Z_{IN} + j\,X_{ANT} + R_{ANT}} \tag{3}$$

The condition in (2) corresponds to the power matching limited to only the reactive part of the input impedance.

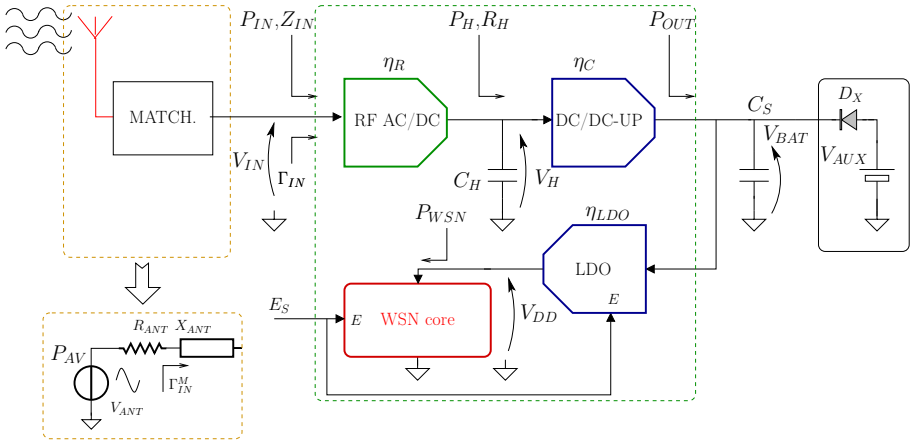

Figure 1. Black-box schematic of a WSN with RF energy harvesting and power management circuits.

The front-end block of the harvester is an RF-rectifier, which performs the AC-to-DC power conversion [9,12,14,15]. Thus, considering a single-tone with frequency f_0 at the antenna terminal, the DC voltage at the rectifier output is:

$$V_H = V_{INp} - \Delta_R \tag{4}$$

where V_{INp} is the amplitude of the sine wave at the rectifier input, and Δ_R is the rectifier threshold. Across a typical RF power range, Z_{IN} exhibits a negative reactance [9], which may be matched with an equivalent series inductance $L_{ANT} = X_{ANT}/2\pi f_0$. It is worth noticing that such tuning equivalent inductance can be synthesized by slightly shifting the center frequency of the antenna from the signal frequency. Assuming reactive matching, the following analytic expressions are obtained from circuit analysis [8]:

$$P_{IN} = P_{AV} \cdot \left[1 - \frac{(R_{IN} - R_{ANT})^2}{(R_{IN} + R_{ANT})^2}\right] \tag{5}$$

$$V_{INp} = Q_{LC} \cdot \sqrt{8\, P_{AV}\, R_{ANT}} \tag{6}$$

where $R_{IN} = Re\,[Z_{IN}]$ is the rectifier input resistance, and Q_{LC} is the quality factor of the R-L-C series network involving the antenna and rectifier resistance, R_{ANT} and R_{IN}, respectively, the rectifier input capacitance C_{IN}, and the matching inductance L_{ANT}:

$$Q_{LC} = \frac{|X_{IN}|}{R_{ANT} + R_{IN}} \tag{7}$$

where $X_{IN} = Im\,[Z_{IN}]$. The equivalent input capacitance at the frequency f_0 is:

$$C_{IN}(f_0) = -\frac{1}{2\,\pi\, f_0\, X_{IN}(f_0)} \tag{8}$$

In RF energy harvesters, the center-band frequency f_0 must be tuned to compensate for the variability of the Electro-Magnetic spectrum with the location and the time. The reactive matching condition can be obtained by means of a programmable bank of integrated capacitors connected to the rectifier input terminals [16,17].

In the calculation of the power delivered by the rectifier P_H, and of the DC output voltage V_H, it has to be considered that the rectifier input power P_{IN} depends on the rectifier input resistance R_{IN}, assuming that the reactive matching condition in (2) is satisfied. Furthermore, the power delivered by the rectifier to the DC/DC converter is set by P_{IN} and by the rectifier efficiency η_R. The influence of P_H on η_R is due to the internal power consumption effects into the rectifier. At low values of

input power, the efficiency is mainly set by the nonlinearity of the series resistance of the rectifying device [18] and by the internal consumption of the threshold compensation circuits, when present [19]. On the contrary, at high power levels, η_R is mainly limited by the voltage drop across the rectifying device and its series resistance [11]. Moreover, the average output voltage V_H at the steady-state has a significant impact on both R_{IN} and η_R values [8,11]. Therefore, with the lumped-elements model in [11] P_H, V_H, and η_R are obtained from P_{AV}, R_{ANT}, and R_H as independent variables, where R_H is the equivalent load resistance of the rectifier.

In the design of the RF scavenging system, the large variability of the EM power in the considered frequency band must be taken into account. Indeed, the largest amount of EM power in the UHF bands is provided by the discontinuous transmissions from base stations of the cellular phone services, which also exhibits the higher density in the urban environment [6–8]. Therefore, the harvester must properly handle the case of intermittent available RF power that may fall below the minimum value required to supply the WSN circuits. These events can occur several times per day and for long-lasting periods of time. Thus, in the system of Figure 1, the harvested RF energy is transferred to an energy reservoir, corresponding to an off-chip large capacitor C_S. In a fully-autonomous scavenging system, the WSN circuits (analog, digital, and RF) are supplied with the energy accumulated in the reservoir, provided that V_{BAT} is higher than the minimum operative supply voltage of those circuits. If an auxiliary battery V_{AUX} is added to the system, as in the box on the right side of Figure 1, the RF harvester will extend the battery lifetime, provided sufficient RF power is available. In the latter scenario, when V_{BAT} drops below $V_{AUX} - V_{DX}$, V_{DX} being the forward voltage of diode D_X, the auxiliary battery supplies the WSN circuits and inhibits the further discharge of the reservoir. A more power-efficient solution could be implemented with a series switch and a low-power comparator.

In the system of Figure 1, the harvested energy is maximized with the simultaneous maximization of the output voltage V_{BAT}. Due to this constraint and to the large variability of the available RF power, the RF rectifier should not be directly connected to the main reservoir. Indeed, with a low input power, the rectifier is not able to transfer energy to the reservoir, whereas the maximization of the rectifier efficiency η_R requires to set the rectifier output voltage V_H at the optimum value, which depends on the input power P_{IN} [11]. Therefore, a DC-DC converter with an intermediate energy reservoir C_H is introduced between the rectifier and the main reservoir C_S.

2.1. DC-DC Converter with Input-Control

The proposed RF energy harvesting system is shown in Figure 2. The RF rectifier is modeled with the Norton equivalent, based on the short-circuit current source I_{Hs} and the small-signal output resistance R_{Hs}. It has to be noticed that this model is valid at constant input power P_{IN} and output voltage V_H. As it is explained below, the latter condition can be achieved with good approximation in the system of Figure 2, with no dependency on the RF input power value. The on-chip capacitor C_H at the input of the DC-DC converter is the intermediate energy reservoir. The step-up converter is controlled by means of the hysteretic comparator COMP that monitors the voltage at the rectifier output V_H and drives the switch S_H. In the proposed system, as long as the rectifier output voltage is lower than the set-point value V_{REF}, the DC-DC converter is disabled and disconnected from the rectifier. Therefore, if P_{IN} is higher than the internal power consumption of the rectifier, the charge flux from the rectifier to the intermediate reservoir pushes up the output voltage V_H. When the threshold voltage is crossed, the DC-DC converter is enabled and connected to the intermediate charge reservoir C_H. Thus, a packet of energy is transferred to the main reservoir C_S and the voltage at the rectifier output drops suddenly, unless the incoming power P_{IN} can fully sustain the average input current I_{IN-C}. The activation of the converter requires that the asymptotic value of V_H in the open-load condition is higher than the comparator threshold, introducing a lower bound for the RF input power to enable a net energy transfer from the antenna to the DC-DC converter.

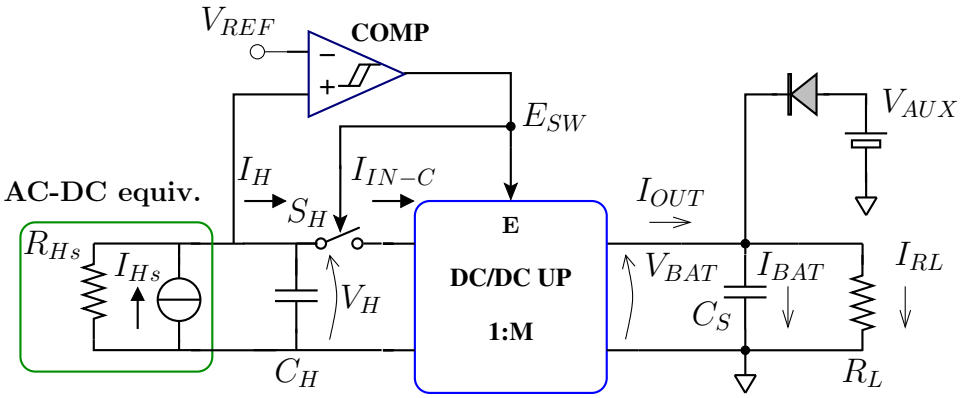

Figure 2. RF Energy harvester system based on a RF rectifier and an input-controlled DC-DC converter.

The waveforms of V_H and of the control signal E_{SW} for an autonomous energy harvesting system, without an auxiliary battery, are shown in Figure 3. Here, T_S is the time period of a complete cycle that is divided into the energy transfer phase (converter on), with length T_{TP}, and the C_H recharging phase (converter off), with length T_{CP}. The input–output voltage ratio of the DC-DC converter in open-load condition (M) must be optimized on the basis of the following design constraints:

- Maximization of the DC-DC converter efficiency
- Maximization of the energy that can be stored in the reservoir C_S.

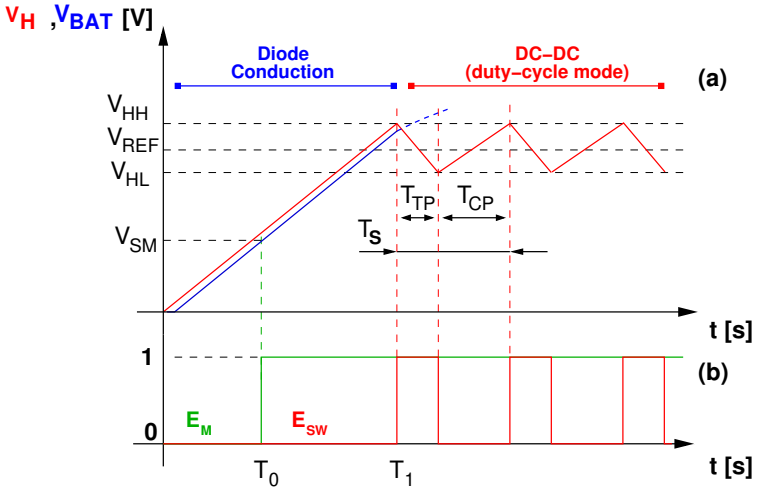

Figure 3. (**a**) time graph of the output voltage of the rectifier output V_H (red trace) and of V_{BAT} (blue trace) for moderate-to-low input power; (**b**) control signal of switch S_H in Figure 2 (green trace) and enables the signal of the DC-DC converter (red trace).

The second constraint requires the maximization of the output voltage V_{BAT} at the steady-state. However, the maximum voltage that can be tolerated at the converter output depends on the breakdown voltage of the MOS devices connected to the output port. In a sub-100 nm technology, the available thick-oxide devices usually exhibit a breakdown voltage within 3.3 V. Furthermore, it is worth noticing that the converter efficiency usually decreases at increasing values of the voltage ratio, thus setting a further constraint on the maximum output voltage.

In the schematic view of the harvester in Figure 2, the output voltage V_{BAT} can be considered approximately constant and not dependent on the power delivered by the DC-DC converter. This assumption holds in a time window that includes several recharge-and-transfer periods of the converter, provided that the rate-of-change of V_{BAT} is sufficiently low. The low derivative of the

battery voltage is due to the high value of the reservoir capacitance, which can be either a multilayer surface-mounting (SMD) ceramic capacitor or a super-capacitor, and it holds considering the ultra-low value of RF available power in generic environments. Cost and size are fundamental parameters for the choice of the energy reservoir, as well as the value of the insulation resistance, setting the self-discharge current. Low-leakage super capacitors exhibit a leakage current in the microampere range [20], whereas the insulation resistance of an SMD ceramic capacitor, with X7R dielectric, is higher than 100 Ω·F, leading to a discharge current lower than 100 nA at 2.5 V output [21]. It is worth noticing that SMD ceramic capacitors in the 1-to-10 µF range are available in the 0603 size. Considering the low average value of the available RF power, the recharge output current may be lower than the self-discharge current of a super capacitor for a large fraction of the time, thus nullifying the benefits of the RF energy scavenging. Therefore, a ceramic capacitor is the preferred choice, given that the energy required by the WSN, when it is enabled, can be provided by a microfarad capacitor with an acceptable voltage drop.

Since the DC-DC converter is loaded by a large capacitor and thus operates with an almost constant output voltage, a reverse energy flow from C_S to the rectifier output occurs if the converter is activated with V_H lower than V_{BAT}/M. Therefore, the following condition must be fulfilled for the lower threshold of the hysteretic comparator:

$$V_{HL} > \frac{V_{BAT}}{M} \tag{9}$$

An approximate analytic expression of the input resistance R_{LH} of a converter with controlled input voltage is obtained from the assumption of a negligible voltage ripple affecting $V_H(t)$, shown in Figure 3:

$$R_{LH} \approx \frac{\overline{V_H}}{\overline{I_H}} \approx \frac{V_{REF}^2}{\eta_R \cdot P_{IN}} \tag{10}$$

where V_H has been approximated with its average value. Therefore, with the input control, the equivalent input resistance of the DC-DC converter is dynamically adapted to the RF input power. It is worth noticing that the equivalent load resistance R_{LH}, at a given RF input power level, depends on the set-point control voltage V_{REF}. Thus, the rectifier efficiency can be maximized at each input power condition by setting the optimum value of V_H and by changing the converter voltage ratio M accordingly. This optimization must be implemented in real-time mode and requires a maximum power point tracking (MPPT) system [11].

The circuit schematic of the DC-DC converter in the proposed harvester implementation is shown in Figure 4, where the only off-chip component is the inductor L_S. A boost converter with external high-Q inductance and working in the Continuous Conduction Mode (CCM) was preferred for the higher efficiency and the smaller silicon area than switched-capacitors' converters. It is worth noticing that, in spite of the higher switching frequency compared to boost converters working in the Discontinuous Conduction Mode (DCM) or Boundary Mode [22], the control circuit of CCM converters exhibits lower complexity and power consumption.

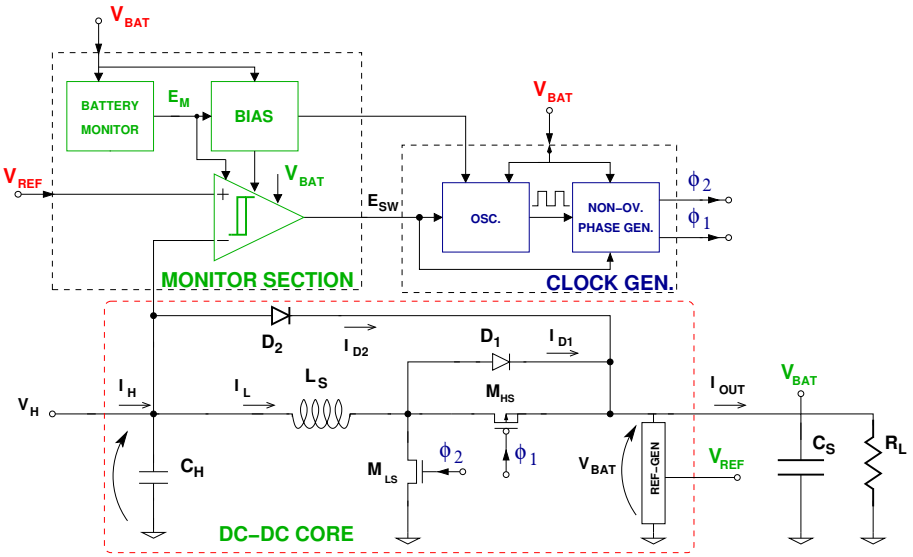

Figure 4. Circuit schematic of the DC-DC converter with input control.

The converter is based on the sections shown in Figure 4: the monitor, the clock generator, and the core converter. In the first block, at the top-left of the circuit schematic, a battery monitor circuit enables the comparator and the bias current generator only if the battery voltage is higher than the minimum value that is required by the control circuits (i.e., comparator, bias generator, and oscillator), V_{SM} in Figure 3.

The battery monitor is the only circuit, with the REF-GEN in the converter core, is always supplied by the charge reservoir C_S, and it must be designed for the minimum current consumption. In the circuit schematic of Figure 5, V_{BAT} is shifted down by the forward voltage of D_B, i.e., V_{DB}, and compared to the threshold voltage of the CMOS inverter IN_1, V_{TH1}. Thus, an approximate analytic expression for V_{TH1} is obtained:

$$V_{TH1} \approx \frac{V_{DB}}{1 - V_{TH1}/V_{BAT}} \tag{11}$$

$$\frac{V_{TH1}}{V_{BAT}} = K_1 \approx const. \tag{12}$$

where K_1 in (12) depends on the aspect ratios of the PMOS and NMOS device in IN_1. The hysteresis $\Delta V_{PM} \equiv V_{PMH} - V_{PML}$ is introduced with transistor M_H. By shorting R_H, M_H increases the diode bias current. Consequently, the voltage drop V_{DB} also increases when the voltage V_X is higher than the threshold of the CMOS inverter.

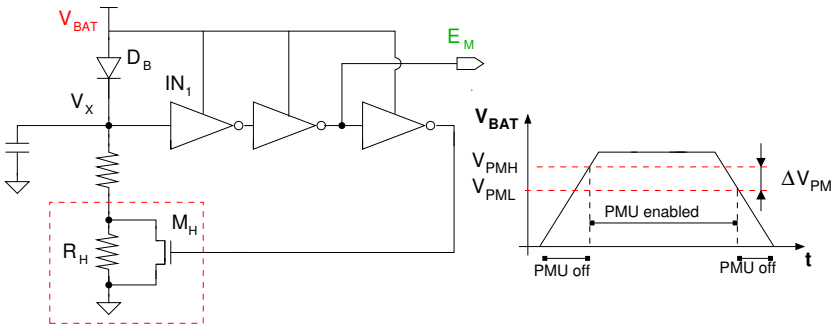

Figure 5. Circuit schematic of the supply monitor.

The comparator is based on a differential CMOS amplifier with cross-coupled load and a class-AB complementary output stage. If the battery-monitor returns a low output signal, $E_M = 0$,

the comparator is driven in power-off mode and its output E_{SW} is set low, as shown in the time graph at the bottom of Figure 3. On the contrary, with the voltage of the main reservoir higher than the threshold set by the voltage monitor, the comparator is activated. If V_H is lower than the set-point voltage V_{REF}, the clock generation circuits are driven in power-down mode with the outputs ϕ_1 and ϕ_2 set high and low respectively, in order to switch off both M_{LS} and M_{HS} in the converter core. Thus, in this configuration, the converter is disconnected from both reservoirs C_H and C_S.

The clock generation section includes a ring oscillator, based on current starved CMOS inverters, and a generator of clock signals with non-overlapped phases, driving the MOS switches in the converter section, i.e., M_{LS} and M_{HS}, respectively. The non-overlapping condition is mandatory to ensure that the main reservoir is never shorted to the ground potential through M_{LS} and M_{HS}. The voltage ratio of the converter is set by the duty-cycle of the clock signal, whereas the efficiency is limited by the series resistance of the off-chip inductor L_S, by the on-resistance of the MOS switches, and by the power consumption of the monitor and clock-generation circuits.

Two diodes are added to the circuit: D_1 is the free-wheeling diode for the inductor L_S, whereas D_2 connects the RF rectifier to the external charge reservoir, and it is activated when V_H is higher than the voltage of the reservoir C_S. This occurs in the case of an excessive available power at the rectifier input or with a battery voltage lower than the threshold of the battery monitor. In the former case, D_2 implements the function of voltage limiter at the rectifier output and protects the RF circuit against the over-voltage condition by steering the RF power directly to the main charge reservoir. In the latter case, the power delivered by the rectifier is steered to the main reservoir, bypassing L_S and the series switch. This situation corresponds to the "Diode Conduction" condition in Figure 3.

The REF-GEN block is a voltage divider based on a stack of diode-connected MOS transistors biased in the deep weak-inversion region. Thus, the set-point voltage of the input-control tracks the voltage of the main reservoir. This is mandatory to always comply condition (9) in order to inhibit the reverse energy flow.

The component values of the integrated DC-DC converter are reported in Table 1. The SMD inductor L_S exhibits a series resistance of 40 Ω and a minimum self resonance frequency (SRF) of 2 MHz [23]. The frequency of the DC-DC oscillator, f_{DCDC}, is set to 750 kHz with a 50% duty-cycle. This leads to an open-load input–output voltage ratio M equal to 2. The value of the integrated capacitor C_H is sized to have at least one converter switching period, $T_{DCDC} = 1/f_{DCDC}$, over the process and temperature corner space. Finally, the comparator is designed for 250 mV of hysteresis width $\Delta V_H = V_{HH} - V_{HL}$, whereas the circuit generating the set-point reference V_{REF} is sized for a typical V_{REF}-over-V_{BAT} ratio of 0.65 V/V.

Table 1. DC-DC converter: design specifications and values of components.

	Value	Unit
L_S	3.9	mH
f_{DCDC}	750	kHz
C_H	600	pF
ΔV_H	250	mV
V_{REF}/V_{BAT} emphV/V	0.65	
M	2	V/V
$(W/L)_{LS}$	12/0.4	µm/µm
$(W/L)_{HS}$	12/0.4	µm/µm

2.2. Linear Regulator

A voltage regulator is usually required to supply the WSN circuits with the available energy of the main reservoir. Indeed, in the system of Figure 1, V_{BAT} may decrease down to the threshold voltage for the activation of the auxiliary supply, i.e., $V_{AUX} - V_{DX}$. Furthermore, if the WSN circuits are implemented with core MOS devices, their breakdown voltage is approximately 1.2 V or even

lower in sub-100 nm technology nodes. Therefore, the WSN circuits cannot be directly supplied by means of the main reservoir and a step-down DC-DC down converter is required.

A DC-DC buck converter would lead to the maximum power efficiency, but it requires an additional off-chip inductor, leading to higher costs and increased area of the printed circuit board (PCB). For this reason, in this prototype, a low-dropout linear regulator (LDO) was preferred.

As shown in the circuit schematic of Figure 6, the LDO is based on a bandgap reference, a two-stage operational amplifier without Miller compensation, and the on-chip capacitor C_R. The schematic of the bandgap reference is shown in the dashed box of Figure 6. The voltages at the emitter of Q_1 and at the upper terminal of R_1 are held approximately equal by M_1 and M_2, which exhibit the same aspect ratio and equal currents, considering the 1:1 current ratio of the M_3-M_4 mirror. Since the emitter area of pnp bipolar junction transistor (BJT) Q_2 is N times, the emitter area of Q_1, the voltage across R_1, and thus the drain current of M_4 are proportional to the absolute temperature (PTAT). This PTAT current is mirrored in the left branch of the circuit where a PTAT voltage is generated across resistor R_2 and summed up to the emitter-base forward voltage of Q_3 to generate a reference voltage with zero temperature coefficient at the room temperature (RT). The circuit highlighted in the red box in Figure 6 is the start-up circuit. At the power-on, the MOS capacitor M_7 is fully discharged and, consequently, M_9 provides a supplementary bias current to M_1. Thus, the circuit bias is moved far from the undesired condition, i.e., M_1 and M_2 with negligible drain currents. Furthermore, the gate voltage of M_4, V_{BIAS}, is used to locally generate the opamp bias current. The large on-chip capacitor is mandatory to achieve the required stability margin for the LDO and to limit the ripple affecting the regulated voltage, if the LDO drives circuits with a significant switching activity, like logic gates and switched-capacitors' circuits.

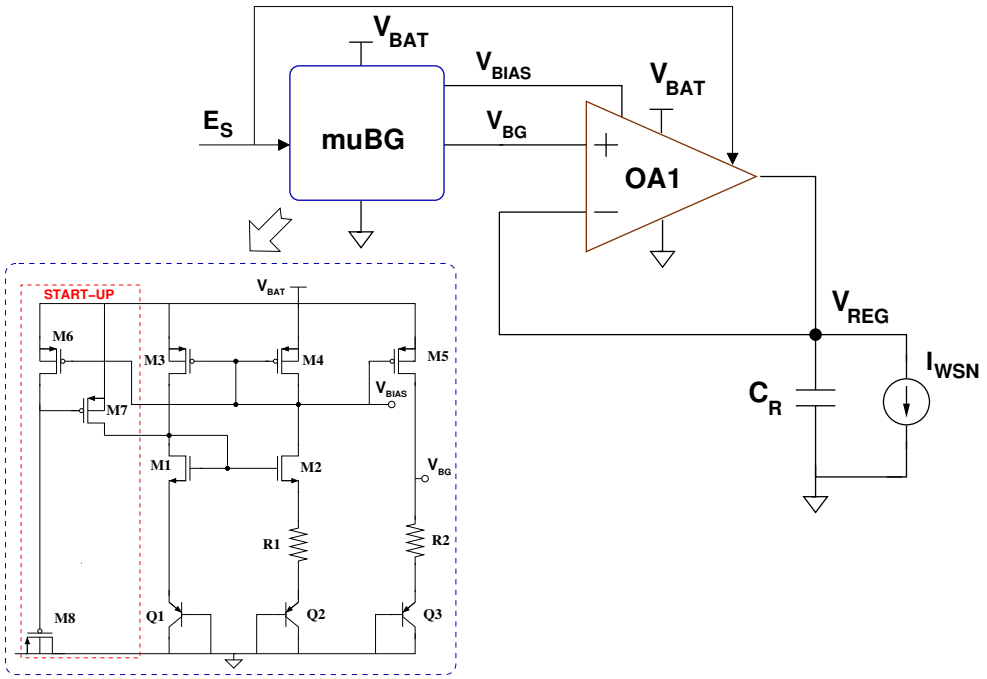

Figure 6. Circuit schematic of the 1.2 V low-dropout regulator with bandgap reference (dashed blue box).

3. Silicon Implementation and Measurements' Results

The proposed power-management modules were implemented in 65 nm CMOS technology. The photograph of the test chip is shown in Figure 7 together with the layout.

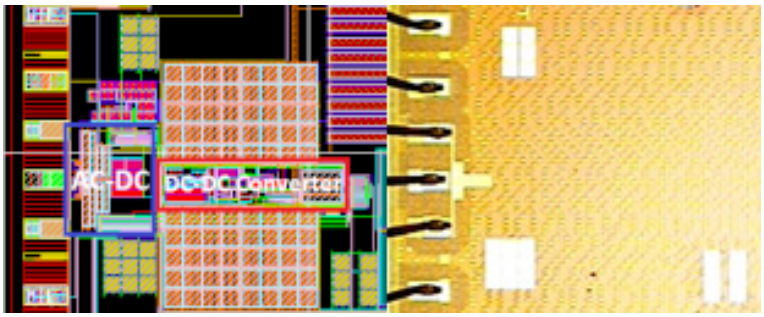

Figure 7. (**Left**) layout of the test chip; (**Right**) photograph of the test chip. The AC-DC and the DC-DC converters are highlighted with the blue and red boxes, respectively.

In order to characterize the DC-DC converter, the output voltage V_{BAT} and current I_{OUT} were, respectively, forced and measured by a Keithley Source and Measurement Unit (SMU) [24]. A linear power supply generator combined with a 500 kΩ series resistor replaced the RF rectifier and was used to supply the converter. The value of the resistor was upper limited by the maximum output voltage of the supply generator, and it is close to the typical values of output resistance of RF rectifiers available in literature. The measured voltage waveforms at the DC-DC converter input in the case of V_{BAT} = 1.3 V and V_{BAT} = 2.0 V are shown in Figure 8a,b, respectively. The trace in Figure 8a was obtained with a low available input power, with an average output power P_{OUT} equal to 310 nW, whereas the measurement of Figure 8b was carried out with a higher input power, corresponding to 2.9 µW delivered power. It is worth noticing that, in the former case, the recharging phase of the intermediate reservoir is longer, due to the lower available input power, thus leading to a lower frequency of the E_{SW} signal in Figure 2. The average value of V_H tracks the value of the main reservoir voltage, as required to fulfill condition (9).

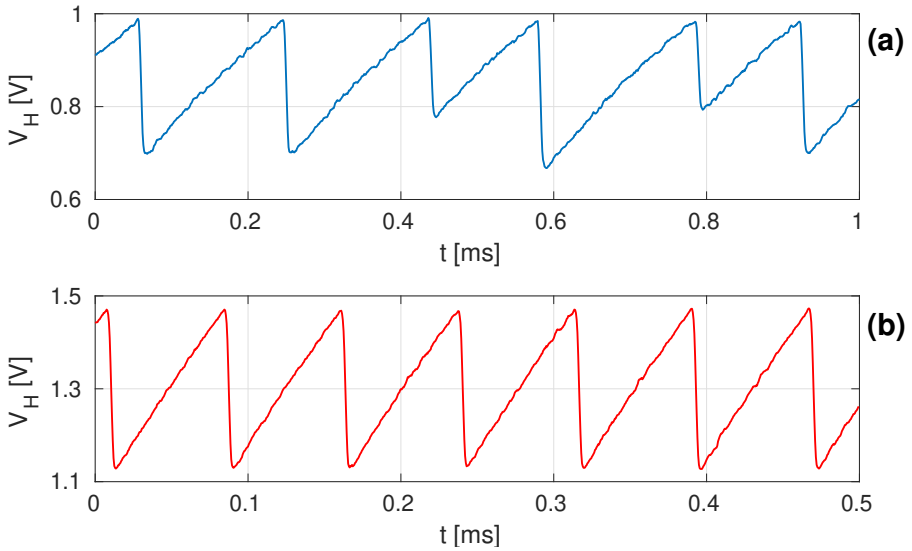

Figure 8. Measured voltage waveforms at the DC-DC converter input. (**a**) V_{BAT} = 1.3 V, P_{OUT} = 310 nW; (**b**) V_{BAT} = 2 V, P_{OUT} = 2.9 µW.

The measured efficiency of the DC-DC converter, $\eta_C \equiv P_{OUT}/P_H$ is shown in the plot of Figure 9, in the cases of a main reservoir voltage V_{BAT} of 1.4 V and 2 V. In both cases, η_R vs. the input power P_H exhibits an absolute maximum. Indeed, at low input power, the internal power consumption is dominated by the static contribution of the control circuit and by the circuit driving the MOS switches, M_{LS} and M_{HS}, whereas, at higher input power levels, the most relevant contributions are the series resistance of the switches in on-state and the series resistance of L_S.

The simulated current consumption at 1.4 V of the monitor section I_{mon}, and of the clock-generator section I_{sw} are reported in Table 2 for the recharging and the energy-transfer phases.

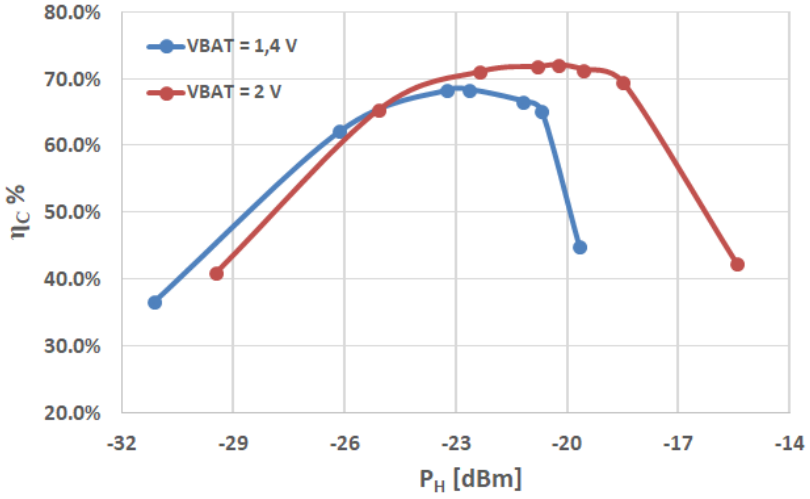

Figure 9. Measured DC-DC converter efficiency vs. input power at V_{BAT} = 1.2 V (blue line) and V_{BAT} = 2 V (red line).

Table 2. Current consumption of the DC-DC converter blocks.

	C_H Charging		Energy-Transfer
Temp	$I_{cc,mon}$	$I_{cc,sw}$	$I_{cc,sw}$
27 °C	290 nA	2.5 nA	346 nA
−40 °C	305 nA	1.4 nA	369 nA
85 °C	230 nA	4.8 nA	335 nA

The LDO and the bandgap reference exhibit an overall current consumption of 4.7 µA at the room temperature, with 1.9 µA required by the LDO. The silicon area without capacitor C_R is 25.5 µm × 27.75 µm. C_R is implemented with a thin-oxide MOS device and exhibits a typical value of 1 nF. In order to characterize the bandgap reference and the LDO, both circuits were disconnected from the main reservoir and supplied by a programmable power supply generator. In Figure 10a, the LDO output and the reference voltage are measured over a large range of the unregulated supply V_{BAT}. The test was carried out with a DC load current equal to 10 µA. The measured load regulation LR is shown in Figure 10b, where $LR \equiv \Delta_{V_{REG}} / \Delta_{V_{BAT}}$ and $\Delta_{V_{REG}}$ is the shift of the LDO output with respect to the case of V_{BAT} = 2.5 V.

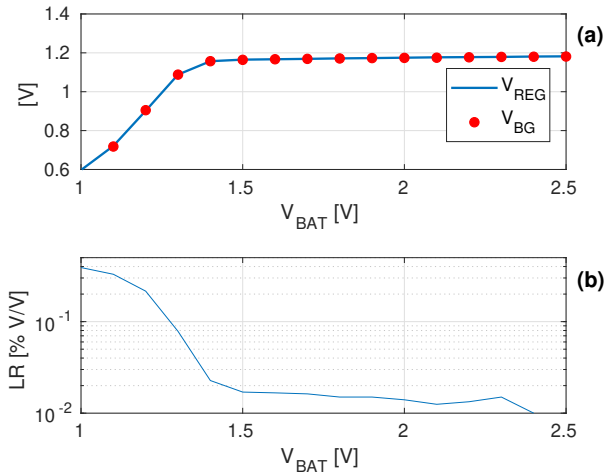

Figure 10. (**a**) measured bandgap reference voltage V_{BG} (red circles), and regulated voltage V_{REG} (solid blue line) vs. V_{BAT}. (**b**) LDO line regulation at V_{BAT} = 2.5 V.

A low-power temperature sensor with a dedicated Analog-to-Digital converter (ADC) was integrated in the test chip [25]. Thus, the sensor with the power-management circuit and an RF rectifier compose the structure of an autonomous sensor node, as in Figure 1. The temperature sensor is based on a pair of p-n junctions with the same size and different bias currents. The sensor output, which is the difference of the bias voltage of the two p-n diodes, exhibits PTAT behavior. The conversion of the sensor output to the digital domain is performed by a Sigma-Delta ADC [25,26]. The digital filter is not integrated in the test chip. Thus, the decimation and filtering of the ADC serial output are performed off-chip. With an optimized digital filter, a nominal resolution higher than 10-b is obtained with an acquisition time of about 15 ms, corresponding to a temperature resolution lower than 0.1 °C over 100 °C of temperature range. The measured current consumption of the whole temperature sensing circuit composed by the sensor, the ADC, and the clock chain, is 4.5 µA at room temperature.

The energy harvesting system in Figure 1, except the RF rectifier, was characterized together with the temperature sensor working in duty-cycle mode. Taking into account that the performance of the proposed power management does not depend on the RF rectifier topology used for the energy harvesting from the tuned antenna, the rectifier was replaced with an SMU [24] configured as a constant current generator and voltage meter. This test-setup allows for measuring the power efficiency of the power management block, including the DC-DC converter with input control, the off-chip charge reservoir, and the LDO. It is worth noticing that the DC-DC converter is always active if the reservoir voltage V_{BAT} is higher than 1.1 V, whereas the LDO with the bandgap reference is enabled only during each temperature measurement phase. In order to limit the time span of the oscilloscope acquisition, the activation frequency of the sensor was set to 6.6 sample/s corresponding to a time lapse between two successive temperature measurements T_{sens} of 150 ms. This activation frequency is significantly higher than the typical values used in WSN applications, where T_{sens} is usually on the order of several seconds. The acquisition time T_{mis} of the ADC bit stream was set to 25 ms, thus higher than the minimum achievable value with an optimized digital filter. Therefore, this set-up corresponds to a worse case in terms of energy consumption, but to a simpler implementation of the digital filter, with a smaller silicon area. In the test, the data were acquired by an FPGA and processed by MATLAB scripts running on a laptop to obtain 12-b data for each temperature measurement.

The oscilloscope traces in Figure 11 correspond to the voltage of the main reservoir V_{BAT} (top graph, blue trace), and to the ADC serial output (bottom graph, red trace), with 6.9 µA current supplied by the SMU to the DC-DC converter, with an average input voltage $\overline{V_H}$ equal to 1.44 V. In the test, the charge reservoir was pre-charged to 2.1 V and the diode in Figure 1 replaced by a switch disconnecting the auxiliary battery before the oscilloscope acquisition. The ripple of the reservoir voltage is due to the activation of the sensing circuits and of the LDO, which require 135 nJ and 246 nJ,

respectively, for each measurement. In this test, the energy supplied to the DC-DC converter leads to an average balanced condition on the amount of charge stored into the main reservoir. Therefore, this is the minimum energy required to supply the sensor with the LDO without draining a supplementary energy from an auxiliary battery. The measurement results in Figures 12 and 13 are obtained with an average input power P_H respectively lower and higher than the minimum value. In the former case, the reservoir voltage progressively decreases until the threshold voltage of 1.1 V is reached and the DC-DC converter is disabled, since the energy supplied to the converter is not enough to sustain the sensor with the LDO at the measurement rate of 6.6 Sample/s. On the contrary, in the measurement of Figure 13, the excess energy is stored in the reservoir.

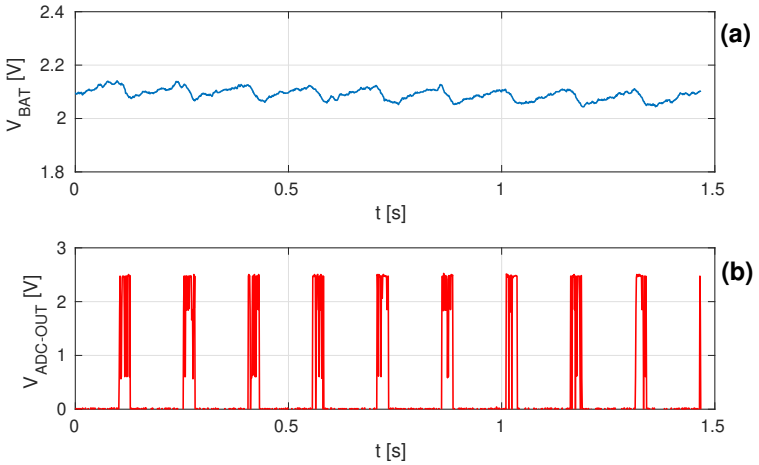

Figure 11. Oscilloscope measurements of the system in Figure 1 with the rectifier replaced by a constant current generator I_H = 6.9 µA, the charge reservoir pre-charged at V_{BAT} = 2.1 V, and the auxiliary battery disconnected. (**a**) V_{BAT} trace; (**b**) ADC serial output.

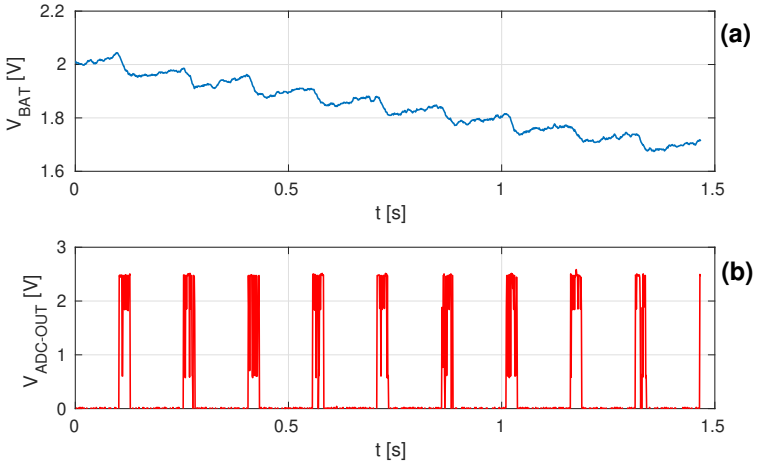

Figure 12. Oscilloscope measurements with the same set-up of Figure 11. Input power lower than the minimum value to sustain the sensing circuits. (**a**) V_{BAT} trace; (**b**) ADC serial output.

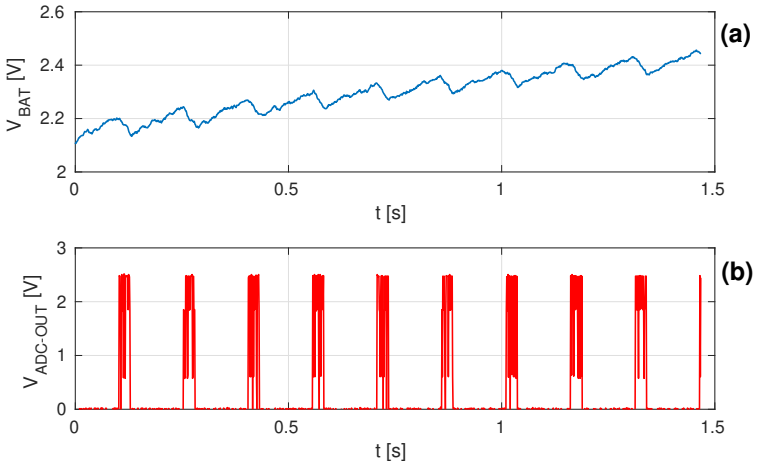

Figure 13. Oscilloscope measurements with the same set-up of Figure 11. Input power higher than the minimum value to sustain the sensing circuits. (**a**) V_{BAT} trace; (**b**) ADC serial output.

The efficiency of the whole power management system is calculated for the balanced condition in Figure 11, which requires 4.46 µW at the DC-DC converter input. Considering the measured current consumption of the sensing circuit and of the LDO are 4.5 µA at 1.2 V and 4.7 µA at 2.1 V V_{BAT}, respectively, with the sampling rate of 6.6 Sample/s an overall PMU efficiency of 20% is obtained.

Starting from the energy consumption of the internal blocks composing the power management, the minimum RF available power required to supply the sensor at lower measurement rates can be estimated. In the following analysis, a measurement rate of 1 Sample/s is assumed with an optimized ADC digital filter that allows for limiting the measurement time to 15 ms, thus leading to 80 nW of average power required by the sensing circuits. The efficiency of the LDO depends on the reservoir voltage and on the current consumption of the bandgap and the amplifier in Figure 6:

$$\eta_{LDO} \equiv \frac{P_{WSN}}{P_{OUT}} = \frac{V_{DD}}{V_{BAT}} \cdot \left(1 - \frac{\overline{I_{LDO}}}{\overline{I_{LDO}} + \overline{I_{WSN}}}\right) \tag{13}$$

where I_{LDO} is the internal current consumption of the LDO with the bandgap reference, and I_{WSN} is the supply current of the temperature sensor with the ADC. It is worth noticing that, in the system of Figure 1, the sensor with the ADC and the LDO with the bandgap are activated by means of the enable signal E_S with a programmed acquisition rate of 1 Sample/s. At the end of the measurement, all the blocks are driven in power down mode. Thus, the current consumption of the LDO and the bandgap must be averaged over the time interval between two successive measurements. Given a measurement rate of 1 Sample/s, I_{LDO} = 4.7 µA, I_{WSN} = 4.5 µA, and V_{BAT} = 2 V, an LDO efficiency of approximately 30% is obtained, with 138 nA of average current I_{OUT} supplied by the reservoir.

The measured efficiency of the DC-DC converter allows for computing the minimum power that must be delivered by the rectifier, i.e., P_H = 395 nW. Finally, the RF power required to supply the sensor is affected by the efficiency η_R of the RF rectifier. A typical range of 20–40% is found for the power efficiency of CMOS UHF rectifiers reported in literature [9,12]. Considering η_R = 30%, a minimum RF power level of −28.5 dBm is obtained. Given the matching of the antenna with the input impedance of the rectifier, this power value corresponds to the available RF power required at the antenna terminal to supply the sensor without draining energy from the auxiliary battery V_{AUX}. The analytic expression of the minimum available power required to supply the sensor is obtained considering the power efficiency of the involved blocks and the reflected power at the RF input due to the residual impedance mismatch:

$$Min\,(P_{AV}) = \frac{\overline{P_{WSN}}}{(1 - |\Gamma_{IN}|^2) \cdot \eta_R \cdot \eta_C \cdot \eta_{LDO}} \tag{14}$$

Thus, in case of impedance mismatch at the antenna–rectifier interface, the value of −28.5 dBm must be increased accordingly to obtain the minimum available RF power. It is worth noticing that the RF power levels obtained in this analysis are available in both urban and semi-urban environment in the 900 MHz frequency bands actually allocated for the 4G and the 3G mobile phone services [8]. The results of the power budget calculation are summarized in Table 3.

Table 3. Power budget of the power harvesting and management system.

SENS		LDO		DC-DC		RF-RECT	
V_{DD}	1.2 V	V_{BAT}	2.0 V	η_C	70%	η_R	30%
I_{WSN}	4.5 µA	I_{LDO}	4.7 µA	P_H	395 nW	P_{IN}	1.3 µW
T_{meas}	15 ms	η_{LDO}	29.4%			P_{IN}	−28.8 dBm
Meas rate	1 Sample/s	I_{OUT}	138 nA				
P_{WSN}	81 nW	P_{OUT}	280 nW				

Table 4 shows the maximum and average P_{IN} values in different urban environments and frequency bands [6–8,13].

Table 4. RF available power in urban environments.

Frequency Band	$\overline{P_{IN}}$	Max$[P_{IN}]$	Ref.
0.7–1 GHz	−21.3 dBm	−19.2 dBm	[8]
1.8–1.9 GHz	−32.3 dBm	−31.3 dBm	[8]
2.2–2.2 GHz	−36 dBm	−34 dBm	[8]
1.7–1.9 GHz 1.9–2.2 GHz 2.5–2.7 Ghz		−7 dBm	[13]
869–894 MHz	−4.5 dBm		[7]
869–894 MHz	−24.7 dBm		[7]
925–960 MHz	−44 dBm/cm^2	−27 dBm/cm^2	[6]
1.8–1.9 GHz	−40 dBm/cm^2	−22 dBm/cm^2	[6]

4. Conclusions

A power management system for the generation of the power supply of WSNs from RF energy harvesting has been presented. A DC-DC boost converter is used to recharge an energy reservoir, while a linear regulator scales down the output voltage for an integrated temperature sensor. The input driven DC-DC converter makes the power management inherently independent of the rectifier design, and it achieves in measurement a peak efficiency of 70%, with an input power of 395 nW. The measurement results of the fundamental blocks make the system suitable for the generation of the power supply of WSNs. Particularly, with an input RF power of −28.5 dBm, the power management sustains a measurement rate of 1 Sample/s with a temperature sensor and an analog-to-digital converter.

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