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Design of an Ultra-Low Voltage Bias Current Generator Highly Immune to Electromagnetic Interference †

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Abstract: The paper deals with the immunity to Electromagnetic Interference (EMI) of the current source for Ultra-Low-Voltage Integrated Circuits (ICs). Based on the properties of IC building blocks, such as the current-splitter and current correlator, a novel current generator is conceived. The proposed solution is suitable to provide currents to ICs operating in the sub-threshold region even in the presence of an electromagnetic polluted environment. The immunity to EMI of the proposed solution is compared with that of a conventional current mirror and evaluated by analytic means and with reference to the 180 nm CMOS technology process. The analysis highlights how the proposed solution generates currents down to nano-ampere intrinsically robust to the Radio Frequency (RF) interference affecting the input of the current generator, differently to what happens to the output current of a conventional mirror under the same conditions.

Keywords: Electromagnetic Interference (EMI); Ultra-Low-Voltage (ULV) ICs; current mirrors; current generators; current-splitter; current correlator

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1. Introduction

Ubiquitous electronics systems require low power consumption to reduce the dependence on batteries through energy harvesting techniques [1,2]. Thus, the electronic circuits need to properly operate at an ultra-low supply voltage [3–6]. This reduces the logic threshold and the noise margin accordingly, making the Integrated Circuits (ICs) more vulnerable to Electromagnetic Interference (EMI) [7–17]. Thus, the robustness of Ultra-Low-Voltage (ULV) ICs in any electromagnetic-polluted environment is an even more demanding task to be guaranteed in a safety-critical device where the need for ultra-low power consumption merges with the request of properly operate in any condition [18–20].

ICs for implanted devices can include on-chip bias current generators operating in sub-threshold to improve current matching as well as allow easy bias current tuning [21,22]. For this reason, among the basic on-chip requirements, the current generation for ICs operating in sub-threshold in the presence of Radio Frequency Interference (RFI) is addressed in this paper.

To this purpose, the EMI robustness of conventional current mirrors operating in the saturation region is first briefly recalled in Section 2. Then, the properties of specific IC topologies operating in the sub-threshold region are summarized in Section 3. Based on such properties, a new current generator with an EMI immunity higher than those of existing current-mirror based schemes is proposed in Section 4. The respective EMI robustness is discussed and evaluated by means of time-domain computer simulations referring to the 180 nm technology process. The conclusions are finally drawn in Section 6.

2. RFI Effect on Current Mirrors

The susceptibility of current mirrors has been investigated, and some solutions to increase their EMI-robustness have been proposed in the literature [23–30]. The typical approach is based on capacitors properly placed to implement a filter and attenuate the EMI [23–28]. Anyhow, all these solutions refer to transistors nominally operating in the saturation region (above threshold).

Figure 1 represents the conventional N and P-type current mirrors. The input current I_{IN} is nominally translated into the output current I_{OUT} according to the ratio $K = \frac{(\frac{W}{L})_1}{(\frac{W}{L})_0}$. The presence of an EMI current i_{emi} superimposed on the input current I_{IN} affects the output current I_{OUT}. A low-pass filter ($R_F C_F$) has been placed to highlight the EMI-induced (DC offset) current named $I_{EMI_{OFFSETn}}$ and $I_{EMI_{OFFSETp}}$ in Figure 1a,b respectively. Notice that along with the paper, the capitalization and lower cases used to name the currents refer to their DC and time-continuous signal values respectively.

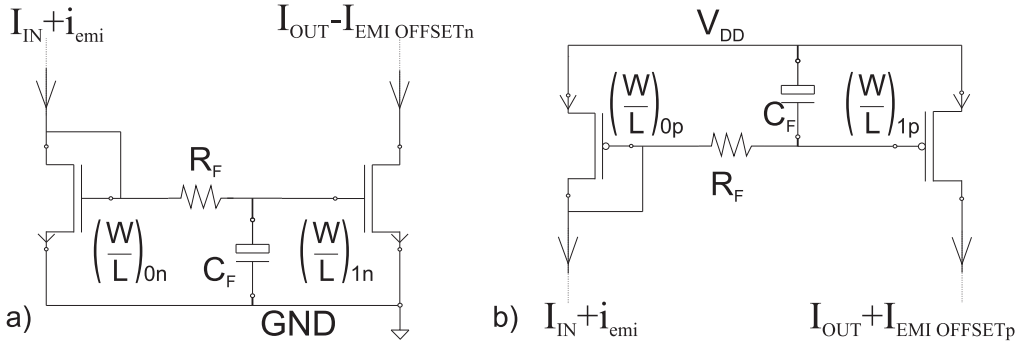

Figure 1. N-type (**a**) and P-type (**b**) current mirrors.

In the presence of interference, the total current through the first branch of the current mirror can then be modeled as the sum of a Continuous Wave (CW) Radio Frequency (RF) current i_{emi} and the proper DC current I_{IN}. This results in an output current affected by EMI $i_{out_{emi}}$ for an N-type mirror [28]:

$$i_{out_{emi}} = K\left[I_{IN} - C_F\sqrt{\frac{1}{\frac{\mu C_{ox}}{2}\cdot(\frac{W}{L})_0}}\cdot\frac{d}{dt}(\sqrt{I_{IN}+i_{emi}})\right] \quad (1)$$

where $K = \frac{(\frac{W}{L})_1}{(\frac{W}{L})_0}$ is the ratio of the transistors' size, μ is the charge-carrier effective mobility, and C_{ox} is the gate oxide capacitance per unit area.

Equation (1) shows that for an N-type mirror (P-type mirror), the DC level of the output current is lower (higher) than it should be, owing to the loading of the input node by capacitor C_F. This means that, in turn, the output current $i_{out_{emi}}$ can be modeled as the sum of the desired DC current I_{OUT} and a negative (positive) current offset named as $-I_{EMI-OFFSET_n}$ ($+I_{EMI-OFFSET_p}$) as reported at the output branches of the current mirrors in Figure 1a,b. In other words, Equation (1) can be rewritten as

$$i_{out_{emi}} = I_{OUT} + i_{error} \quad (2)$$

where $I_{OUT} = K \cdot I_{IN}$ is the nominal output current with no EMI presence and i_{error} represents the effect of the EMI on the output current.

Thus,

$$i_{error} = i_{emi-induced} = KC_F\sqrt{\frac{1}{\frac{\mu C_{ox}}{2}\cdot(\frac{W}{L})_0}}\cdot\frac{d}{dt}(\sqrt{I_{IN}+i_{emi}}) \quad (3)$$

which implies an EMI-induced offset on the output current $I_{\mathrm{EMI-OFFSET}} = |i_{\mathrm{error}}| = |i_{\mathrm{emi-induced}}|$ so that Equation (2) can be rewritten referring to the DC values as:

$$I_{\mathrm{OUT_{EMI}}} = I_{\mathrm{OUT}} + I_{\mathrm{EMI-OFFSET}} \tag{4}$$

These analytic results are valid under the assumption that in the N-type (P-type) current mirror both the transistors M_{n0} (M_{p0}) and M_{n1} (M_{p1}) operate in the saturation region.

3. Ultra-Low-Voltage Current Generators

To reduce the overall power consumption of any System-on-Chip, the trend in reducing the power supply moves towards ICs operating in sub-threshold and thus towards a range of current below micro-amperes. This means that the mirroring ratio K could convert currents in the range of micro-amperes into mirrored currents in the nano-amperes range.

To move towards Ultra-Low-Voltage current generators, the properties of transistors operating in sub-threshold [31] are explored to build an IC solution more robust to EMI. For this reason, the properties of the current-splitter [32,33] and the current-correlator [34] are summarized, respectively, in Sections 3.1 and 3.2.

3.1. Current-Splitter

Figure 2 represents N- and P-type current-splitters (Figure 2a,b respectively). Such circuits are capable of providing sourced or sunk currents in the order of nano-amperes or even below through a splitting technique. The size ratio of the transistors Ma, Mb and Mf are $(W/L)_a = N-1$, $(W/L)_b = N/(N-1)$ and $(W/L)_f = 1$ respectively [32]. The current provided by each output branch is progressively divided by a factor N [32]. In other words, the currents provided by each branch comes from a resistive-like partition of the reference current. Indeed, for $N = 2$ the current-splitter behaves like an M2M ladder network which can be controlled digitally by means of switches to produce any combination of binary-weighted currents. Differently, in the current-splitter, N can be chosen higher than two to rapidly scale down (with the factor N) the reference (input) current I_{REF}. By lowering the operating currents, both noise and mismatch will remain constant and independent by the current level for the complete weak inversion regime [32].

Figure 3 compares how to scale a current I_{IN} with a current mirror by a factor $K_{\mathrm{M}} = \frac{\left(\frac{W}{L}\right)_0}{\left(\frac{W}{L}\right)_1}$ (see Figure 3a) and with a current-splitter by a factor $K_{\mathrm{CS}} = N^2$ (see Figure 3b). Such a factor is originated by the sum of the N-weighted currents provided by the enabled branches of the current-splitters [32].

Based on these characteristics, the current-splitter perfectly matches the needs of current scaling to bias Ultra-Low-Voltage ICs. In fact, the current-splitter is already used in critical scenarios like neural implants where low power consumption and high reliability are tight constraints [22,35]. This makes further valuable the investigation of ULV current generators robust to EMI.

Referring to Figure 3, assuming $K_{\mathrm{M}} = K_{\mathrm{CS}} = N^2 = 100$ and accordingly to the sizing reported in Table 1, the overall area of the proposed solution is 2.5× larger than that of the current mirror. Moreover, to properly set the M2M-ladder division, the current I_{IN} has to be mirrored. This results in doubled overall power consumption. Anyhow, such a current scaling joint with the current correlator properties (in Section 3.2) allows to dramatically increase the EMI robustness of current bias for ICs operating in sub-threshold solution without any additional (external) capacitance as shown in the following.

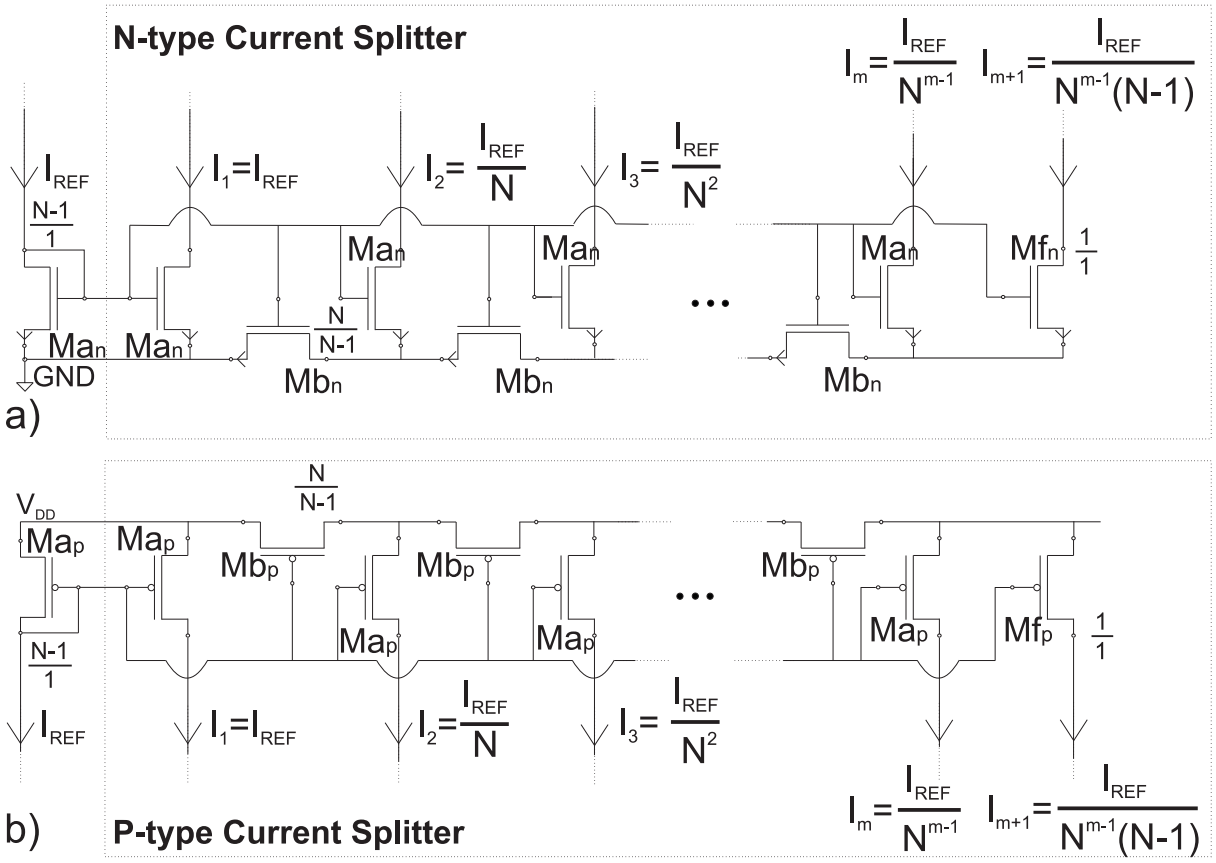

Figure 2. Schematic of the N-type (**a**) and P-type (**b**) current-splitter [32].

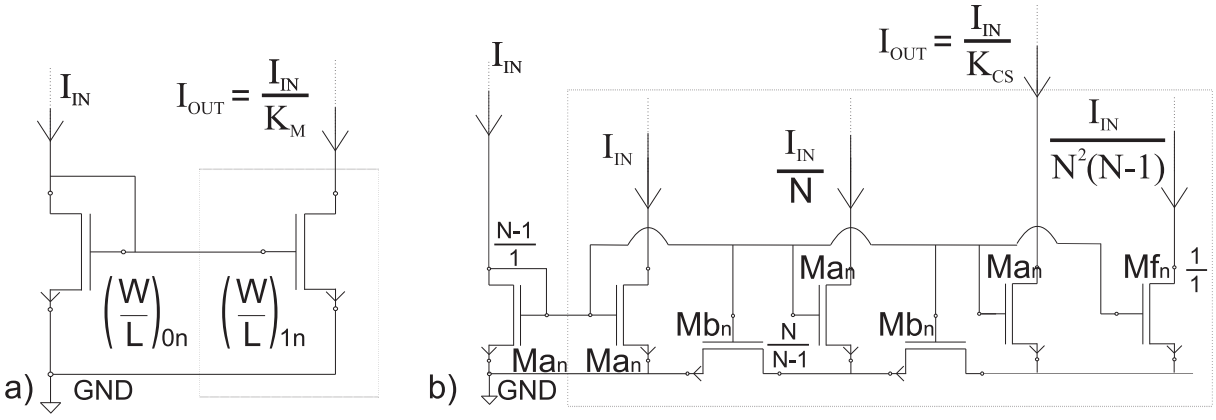

Figure 3. (**a**) N-type current mirror with a current scaling $K_M = \frac{\left(\frac{W}{L}\right)_0}{\left(\frac{W}{L}\right)_1}$ and (**b**) Current-Splitter [32] with a current scaling $K_{CS} = N^2$.

Table 1. Sizing of the transistor in Figure 3.

Parameter	Value	Units
$(W/L)_0$	100/1	µm/µm
$(W/L)_1$	1/1	µm/µm
$(W/L)_{a_{n,p}}$	9/1	µm/µm
$(W/L)_{b_{n,p}}$	10/9	µm/µm
$(W/L)_{f_{n,p}}$	1/1	µm/µm

3.2. Current Correlator

Another valuable circuit topology that operates in the sub-threshold region is the current-correlator shown in Figure 4 [34]. This circuit computes a measure of the correlation between its two input currents named I_A and I_B. More precisely, the output current I_{OUT} is proportional to the product of the two input currents, divided by the sum of the inputs:

$$I_{OUT} = K_{CC} \cdot \frac{I_A I_B}{I_A + I_B} \tag{5}$$

where $K_{CC} = \frac{\left(\frac{W}{L}\right)_{middle}}{\left(\frac{W}{L}\right)_{outer}}$.

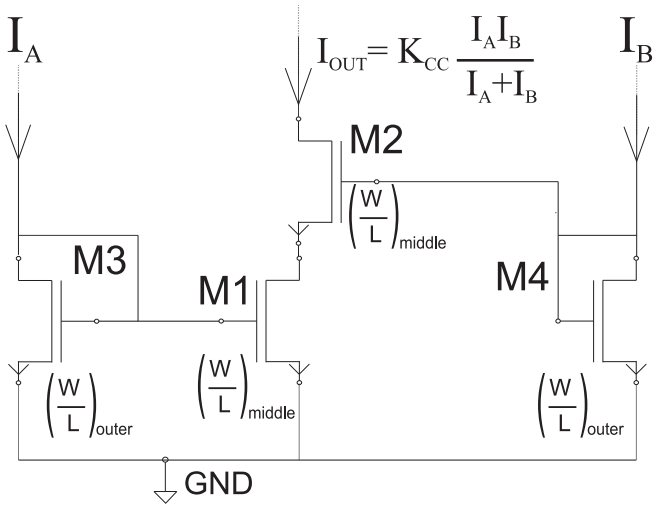

Figure 4. Schematic of a current-correlator [34].

To reduce the overall EMI-induced offset, in this topology I_A e I_B are considered to be, respectively, affected by the P- and N-type induced EMI offset:

$$\begin{aligned} I_A &= I_{IN} + I_{EMI_{OFFSETp}} \\ I_B &= I_{IN} - I_{EMI_{OFFSETn}} \end{aligned} \tag{6}$$

Assuming $I_{EMI_{OFFSETp}} \approx I_{EMI_{OFFSETn}} = I_{EMI_{OFFSET}}$, Equation (5) can be rewritten as:

$$I_{OUT_{emi}} \approx K_{CC}\left(\frac{I_{IN}}{2} - \frac{I^2_{EMI_{OFFSET}}}{2I_{IN}}\right) \tag{7}$$

The effect of the two different EMI offset contributions at the two input branches is compensated so that:

$$I_{\mathrm{OUT_{emi}}} \approx I_{\mathrm{OUT}} - K_{\mathrm{CC}} \cdot \left(\frac{I^2_{\mathrm{EMI_{OFFSET}}}}{2I_{\mathrm{IN}}} \right) = I_{\mathrm{OUT}} - I_{\mathrm{ERROR}} \tag{8}$$

where

$$I_{\mathrm{ERROR}} = K_{\mathrm{CC}} \cdot \left(\frac{I^2_{\mathrm{EMI_{OFFSET}}}}{2I_{\mathrm{IN}}} \right) \tag{9}$$

Comparing Equations (9) with Equation (3), it can be noticed that the overall EMI-induced offset error I_{ERROR} is now much attenuated. In fact, in the practical case $I^2_{\mathrm{EMI_{OFFSET}}} \ll I_{\mathrm{IN}}$ so that the error factor $K_{\mathrm{CC}} \cdot \frac{I^2_{\mathrm{EMI_{OFFSET}}}}{2I_{\mathrm{IN}}}$ is negligible and the output current is not strongly affected by the EMI:

$$I_{\mathrm{OUT_{emi}}} \approx K_{\mathrm{CC}} \cdot \frac{I_{\mathrm{IN}}}{2} = I_{\mathrm{OUT}} \tag{10}$$

Figure 5 represents how an EMI current i_{emi} generates an EMI-induced offset $I_{\mathrm{EMI_{OFFSET}}}$ on a conventional current mirror while EMI currents superimposed with the opposite sign to the two branches of a current correlator do not affect its output current I_{OUT}.

Notice that even if the EMI-induced offset currents $I_{\mathrm{EMI_{OFFSETp}}}$ and $I_{\mathrm{EMI_{OFFSETn}}}$ superimposed on the nominal current I_{IN} of the two input branches of the current correlator with opposite signs (as in Equation (6)) are not equal in amplitude ($I_{\mathrm{EMI_{OFFSETp}}} \neq I_{\mathrm{EMI_{OFFSETn}}}$) but in the same order of magnitude, the interference effect on the output current I_{OUT} is attenuated.

This characteristic will be exploited in the newly proposed solution and validated by means of simulation in Section 4.

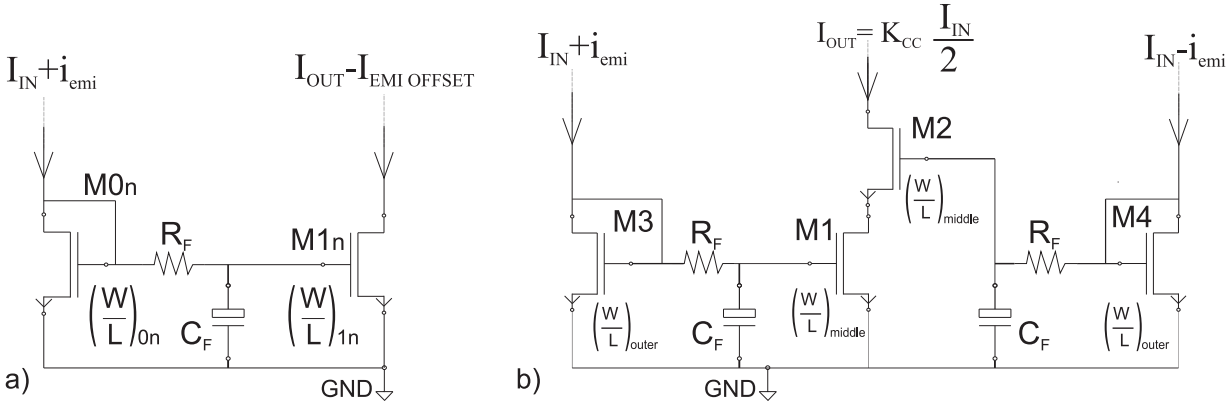

Figure 5. (**a**) N-type current mirror with N-type Electromagnetic Interference (EMI)-induced offset (negative offset current $I_{\mathrm{EMI_{OFFSETn}}}$) and (**b**) current-correlator [34] with opposite EMI-induced offset as input currents.

4. A New Current Generator Robust to EMI

The above-described circuit topologies operating in sub-threshold are employed as building blocks of a new current biasing circuit sketched in Figure 6 in which the input current to be mirrored and scaled is affected by EMI.

The input current I_{IN} represents both the independent sourced (I_{SOURCE}) and sunk (I_{SINK}) currents ($I_{\mathrm{SOURCE}} = I_{\mathrm{SINK}} = I_{\mathrm{IN}}$) that come from reference currents (not reported in Figure 6. These reference currents are usually implemented using a voltage regulator and an operational amplifier to produce a current from the feedback of a small series resistance [36]. To not introduce any error, these building blocks should be designed according to the existing design guidelines to avoid any EMI-induced offset at their outputs [37–40]. In this way, the proper input DC current I_{IN} can be provided even if still affected by a superimposed

EMI current i_{emi}. Thus, for sake of simplicity and focusing on the current generator only, $I_{IN} = I_{SOURCE} = I_{SINK}$ is considered. The same assumption is applied for the respective superimposed EMI currents ($i_{emi} = i_{emi,source} = i_{emi,sink}$). Notice that the minimum difference in the inputs branches currents (I_{SOURCE} and I_{SINK}) and in the respective superimposed EMI currents ($i_{emi,source}$ and $i_{emi,sink}$) do not affect the mathematical definition of the output current I_{OUT} much.

The input current I_{IN} is scaled down by a ratio factor K_{CS} through both P and N-type current-splitters. The presence of complementary current-splitters in the circuit in Figure 6 allows to rapidly scale the input current and benefit from the EMI-induced offset compensation based on an N-P offset compensation [40], which is performed through the current-correlator. The scaled currents coming from a P and N-type current-splitters flow to the respective current correlator that balances the opposite offset trend according to Equation (7). Assuming the aspect ratio of the current-correlator is equal to $K_{CC} = 2$:

$$I_{OUT} \approx K_{CC} \frac{I_{IN}}{2K_{CS}} = \frac{I_{IN}}{K_{CS}} \tag{11}$$

On this basis, the circuit in Figure 6 performs a current mirror-like function suitable for ICs operating in the nano-ampere range and highly immune to EMI.

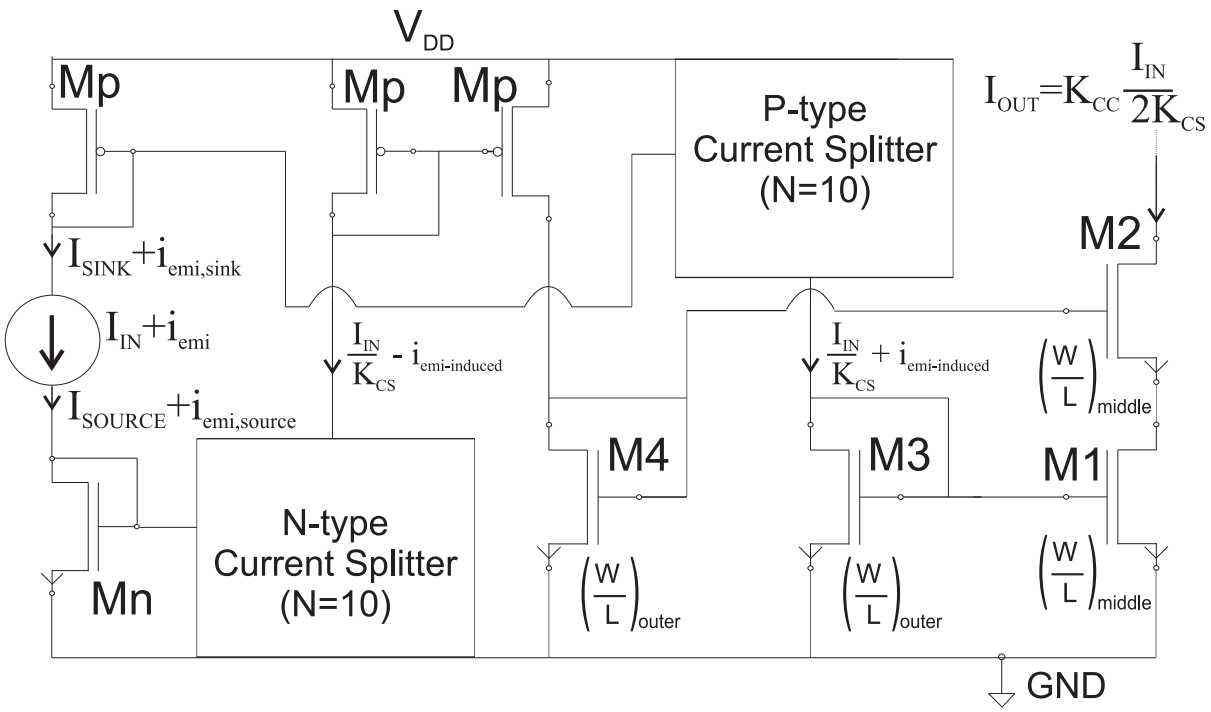

Figure 6. Schematic of the proposed current generator operating in the subthreshold region and robust to EMI.

Table 2. Sizing of the transistor employed in the new current bias method proposed in Figure 6.

Parameter	Value	Units
$(W/L)_{a_{n,p}}$	9/1	µm/µm
$(W/L)_{b_{n,p}}$	10/9	µm/µm
$(W/L)_{f_{n,p}}$	1/1	µm/µm
$(W/L)_{middle}$	10/1	µm/µm
$(W/L)_{outer}$	10/1	µm/µm
$(W/L)_{n}$	10/1	µm/µm
$(W/L)_{p}$	10/1	µm/µm

5. Validation and Comparison

To verify the EMI robustness of the proposed circuit solution, time-domain simulations have been performed with reference to the 180 nm CMOS technology. Analyses have been carried out referring to a traditional current mirror in Figure 5a and the proposed solution in Figure 6. For both these current bias methods, the output current $I_{OUT} = 100$ nA originates from an input current $I_{IN} = 10$ µA affected by a CW RF current i_{emi}. It means that $K_M = K_{CS} = 100$. Thus, both the P- and N-type current-splitters divide the input current twice by a factor N = 10. Table 2 reports the transistors' size for both the current-splitters and current correlator presented in Figure 6. On this basis, the overall area results to be 5× larger than that of a conventional current mirror with the same scaling factor.

The interference current i_{emi} is superimposed on the input current I_{IN} and the DC offset on the output current I_{OUT} is evaluated similarly to immunity tests [41]. Every simulation result refers to the average value assumed by the output current in steady-state conditions when the offset becomes constant and while the input is affected by a CW EMI. In addition, process corner variations have also been reported: ss (dashed) and ff (dotted-dashed) line. Such variations could vary the DC nominal output current I_{OUT} up to 10% in the proposed solution but not its EMI robustness. Thus, if a precise output current value is needed, it can be reached through calibration keeping the EMI robustness capability.

In Figure 7 the EMI-induced offset on the current $I_{OUT} = 100$ nA versus the amplitude of the interference i_{emi} at 100 MHz is reported. A relevant gap between the two EMI-induced offsets on the output current can be highlighted. The newly proposed solution represented in Figure 6 shows an error on the output current below 5% for a CW RF interference current i_{emi} equal to 50 µA. In the same condition, the conventional current mirror exhibits an error of 90% (from 100 to 10 nA).

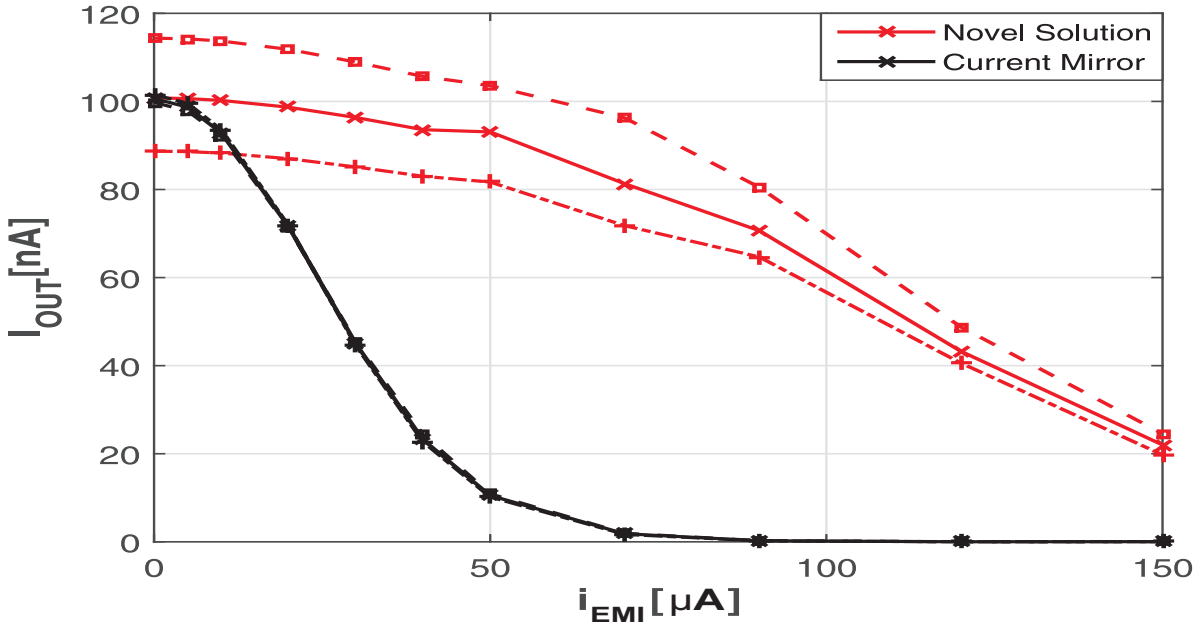

Figure 7. Output current I_{OUT} due to an input current $I_{IN} = 10$ µA with a superimposed Continuous Wave (CW) Radio Frequency (RF) current i_{emi} in an N-type current mirror ($K_M = 100$ in Figure 5a) and in the proposed solution ($K_{CS} = 100$ in Figure 6). Process corner: ss (dashed) and ff (dotted-dashed) line. I_{OUT} versus i_{emi} amplitude (i_{emi} @ 100 MHz).

Similarly, the amplitude of the interference is kept constant and equal to $i_{emi} = 50$ µA while its frequency is swept in the RF range in Figure 8. The proposed current generator shows higher robustness to EMI in a larger RF range.

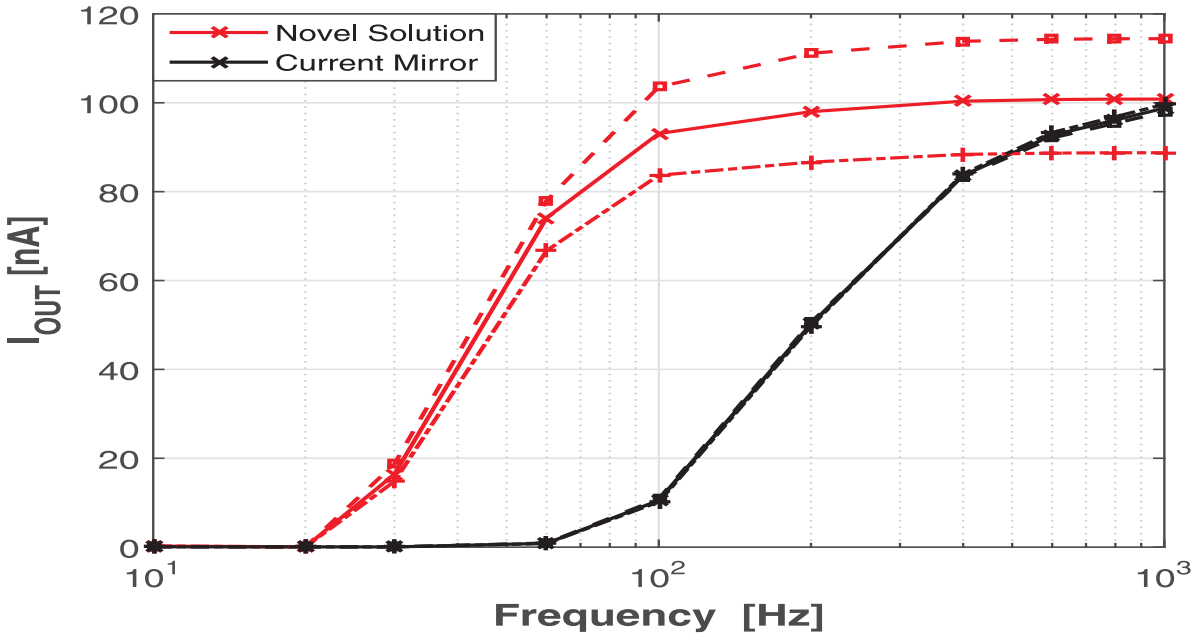

Figure 8. Output current I_{OUT} due to an input current $I_{IN} = 10$ µA with a superimposed CW RF current i_{emi} in an N-type current mirror ($K_M = 100$ in Figure 5a) and in the proposed solution ($K_{CS} = 100$ in Figure 6). Process corner: ss (dashed) and ff (dotted-dashed) line. I_{OUT} versus i_{emi} frequency ($i_{emi} = 50$ µA).

Figure 9 represents the percentage variations of the output current ($I_{OUT_{error}} = \frac{I_{OUT} - I_{OUT_{emi}}}{I_{OUT}} \cdot 100$) due to the interference i_{emi} versus the value of the DC value itself I_{OUT} with no EMI presence. The sweep in the I_{OUT} has been obtained simply changing the input DC current I_{IN} and keeping the CW RF interference i_{emi} at 100 MHz, the same frequency of the amplitude sweep in Figure 7 and with the same amplitude of the frequency sweep in Figure 8 ($i_{emi} = 50$ µA). The lower the output current I_{OUT} to obtain, the higher the effectiveness of the proposed method in providing a current robust to EMI.

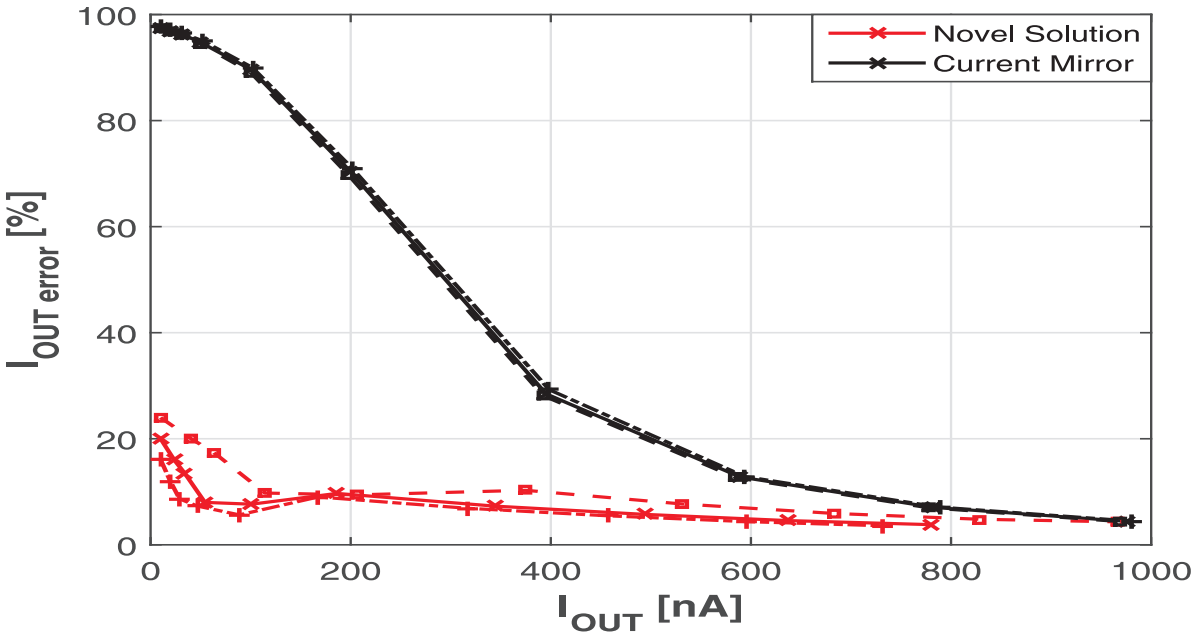

Figure 9. Percentage error $I_{OUT_{error}}$ due to a CW RF current i_{emi} superimposed on a variable input current I_{IN} in an N-type current mirror ($K_M = 100$ in Figure 5a) and in the proposed solution ($K_{CS} = 100$ in Figure 6). Process corner: ss (dashed) and ff (dotted-dashed) line. $I_{OUT_{error}}$ versus I_{OUT} for $i_{emi} = 50$ µA @ 100 MHz.

6. Conclusions

In this work, a new integrated method suitable to provide currents for ICs operating in sub-threshold and robust to EMI has been discussed. The EMI-induced offset on the output current of a conventional current mirror is first considered. Then, based on ICs building blocks operating in sub-threshold, a new current generator for ULV ICs has been proposed. Such an IC solution exploits the N-P offset compensation and the properties of the current-correlator to strongly attenuate the EMI-induced offset on the output current.

The mathematical results as well as the time domain simulations show that for different conditions of frequency and amplitude of the EMI, the newly proposed solution to generate currents for ICs operating in sub-threshold is highly immune to EMI and much more robust than conventional current mirrors. This is at the cost of 4× higher overall current consumption (2× for each current-splitter) and 5× larger area compared to the conventional current mirroring.

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Abbreviations

The following abbreviations are used in this manuscript:

EMI	Electromagnetic Interference
ICs	Integrated Circuits
CMOS	Complementary Metal-Oxide-Semiconductor
RF	Radio Frequency
RFI	Radio Frequency Interference
ULV	Ultr-Low Voltage
CW	Continuous Wave

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