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Article

Implementation of Power-Efficient Class AB Miller Amplifiers Using Resistive Local Common-Mode Feedback

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Abstract: An approach to implement single-ended power-efficient static class-AB Miller op-amps with symmetrical and significantly enhanced slew-rate and accurately controlled output quiescent current is introduced. The proposed op-amp can drive a wide range of resistive and capacitive loads. The output positive and negative currents can be much higher than the total op-amp quiescent current. The enhanced performance is achieved by utilizing a simple low-power auxiliary amplifier with resistive local common-mode feedback that increases the quiescent power dissipation by less than 10%. The proposed class AB op-amp is characterized by significantly enhanced large-signal dynamic, static current efficiency, and small-signal figures of merits. The dynamic current efficiency is 15.6 higher, the static current efficiency is 10.6 times higher, and the small-signal figure of merit is 2.3 times higher than the conventional class-A op-amp. A global figure of merit that determines an op-amp's ultimate speed is 6.33 times higher than the conventional class A op-amp.

Keywords: class AB; amplifier; Miller effect; resistive local common-mode feedback; slew rate; gain bandwidth

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1. Introduction

The Miller op-amp is the essential building block of analog integrated circuits [1,2]. In the conventional class-A Miller op-amp with an NMOS input stage [2,3] shown in Figure 1a, the NMOS output transistor limits the peak negative output current to a value I_{outQ} corresponding to the output branch's quiescent current. This imposes a severe limitation in the op-amp's negative slew rate (SR^-). This can be expressed as $SR^- = (I_{outQ} - I_{RL})/(C_C + C_L)$, where C_C and C_L are compensation and load capacitors and I_{RL} is the current of the resistive load. Many approaches have been proposed to implement Miller op-amps with static class-AB [4,5] output stages. This type of amplifier can drive a wide range of capacitive and resistive loads down to very low frequencies or DC. They are required to have approximately symmetrical slew rates and to be able to generate symmetrical peak load positive and negative output currents $I_{Outpk}{}^+$ and $I_{Outpk}{}^-$ much larger than the total op-amp quiescent current I_{totQ}. A common figure of merit to characterize the op-amp current efficiency CE = I_{Outpk}/I_{totQ} is defined as the ratio of the minimum of the positive and negative peak output currents I_{Outpk} = MIN{$I_{Outpk}{}^+$, $I_{Outpk}{}^-$} to I_{totQ}.

The conventional class-A op-amp (Conv-A) is characterized typically by CE < 0.5. Many approaches to implementing class-AB op-amps are based on the floating battery [6] scheme shown in Figure 1b. The floating battery that exists between the gates of the PMOS and NMOS output transistors causes the voltage V_Y at the gate of the output NMOS transistor to follow the variations at node V_X, which is the high impedance output node of the differential input stage. The voltage V_X drives the output PMOS transistor M_{OP}. The small signal model of the class-AB op-amps based on the floating battery [6] scheme is shown in Figure 1c. In this, the ideal floating battery has been replaced by an AC short circuit. The output resistance R_{Out} is given by $R_{Out} = R_{oOP} \| r_{oON} \| R_L$. As the conventional Miller compensation is used in the op-amp, the transfer function of the circuit of Figure 1c can be written as Equation (1).

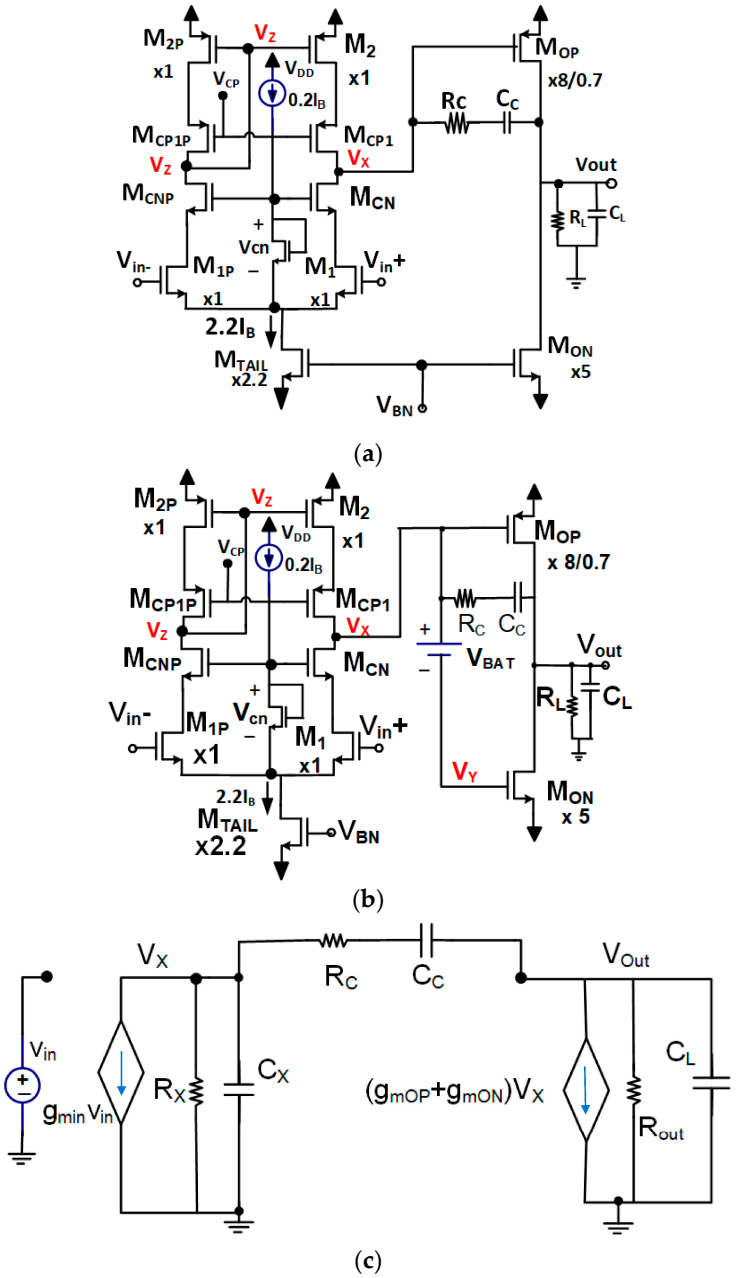

Figure 1. (**a**) Conventional class-A Miller op-amp, (**b**) Miller op-amp with class-AB output stage based on floating battery, and (**c**) small-signal model of the class-AB op-amp based on the floating battery scheme.

$$H(s) = \frac{A_{OLDC}\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{pOut}}\right)\left(1 + \frac{s}{\omega_{pDOMX}}\right)} \quad (1)$$

Here, ω_z, ω_{pOut}, and ω_{pDOMX} are given by the following expressions Equations (2)–(4).

$$\omega_z = \frac{1}{\left[R_C - \left(g_{mOP} + g_{mON}\right)^{-1}\right]C_C} \quad (2)$$

$$\omega_{pOut} = \frac{\left(g_{mOP} + g_{mON} + R_L\right)}{C_L} \quad (3)$$

$$\omega_{pDOMX} = 1/R_X C_X \quad (4)$$

where C_X is given by $C_X = (1 + |A_{Out}|)\, C_C$, $R_X = g_m {r_o}^2/2$, and $|A_{Out}|$ is the gain of the output stage.

The operation of Class-AB op-amps based on the floating battery principle is discussed below:

(a) Upon application of a positive step at V_{in}, the output of the op-amp provides a positive output current to the load. When the output slews in the positive direction, the voltage at node Vx is subject to a large negative variation, which is followed by the voltage at node V_Y until it reaches the bottom rail. This increases the current in M_{OP} and decreases the current in M_{ON}, bringing it to zero for large negative variations in V_Y that lead to $V_{GSON} < V_{TN}$, where V_{TN} is the threshold voltage of M_{ON}. Since V_X can have large negative variations, the peak positive output current ${I_{Outpk}}^+$ provided by M_{OP} can be much larger than its quiescent current $I_{OutQ,}$ and a large positive slew rate can be achieved. The situation is quite different for negative steps in V_{in}. In this case, V_X has a relatively limited excursion in the positive direction, which is transferred (in practice with some attenuation) to V_Y. This causes the current in M_{OP} to decrease (and eventually go to zero) and M_{ON} to increase. However, given that the variation in the positive direction of Vx and V_Y is much smaller than the variation in the negative direction, the op-amp's peak negative output current ${I_{Outpk}}^-$ generated by M_{ON} is in general much smaller than ${I_{Outpk}}^+$. This leads to a negative slew rate, which can be much smaller than the positive slew rate. In practice, the smaller of the two slew rates determines the nominal op-amp's slew rate $SR \equiv MIN\{SR^+, SR^-\}$.

(b) The practical implementation of the floating battery scheme requires a control circuit to achieve the desired nominal output quiescent current I_{OutQ}, which adjusts the value of the floating battery V_{BAT} so that its value is well defined and remains constant, independent of temperature, process parameters, and supply voltage variations. It can be shown that, in saturation, I_{OutQ} is approximately given by, $I_{outQ} = \left[\left(V_{supply} - V_{BAT} - |V_{TP}| - V_{TN}\right) / \left(\sqrt{1/\beta_N} + \sqrt{1/\beta_P}\right)\right]^2$ where β_N, β_P, V_{TN}, and V_{TP} are the NMOS and PMOS output transistors' gain factors and threshold voltages, respectively. A control circuit to adjust the value of V_{BAT} is required since a fixed V_{BAT} value would lead to large variations in I_{OutQ} with changes in V_{supply}, V_{TN}, V_{TP}, β_N, or β_P. An example of the class-AB output stage using a foating battery and a control circuit is shown in Figure 2. In this example, the floating battery is implemented using a voltage follower. The circuit implementation of both V_{BAT} and the control circuit [7,8] can be relatively complex (as shown in Figure 2b and in the circuit of [8]) and increases the total op-amp's quiescent current. This can significantly lower the current efficiency of the class-AB op-amp. In some cases, it can also increase the supply requirements beyond the nominal supply voltage of the implementation technology, which has been reduced to sub-volt values ($V_{supply} < 1$ V) in modern CMOS technologies.

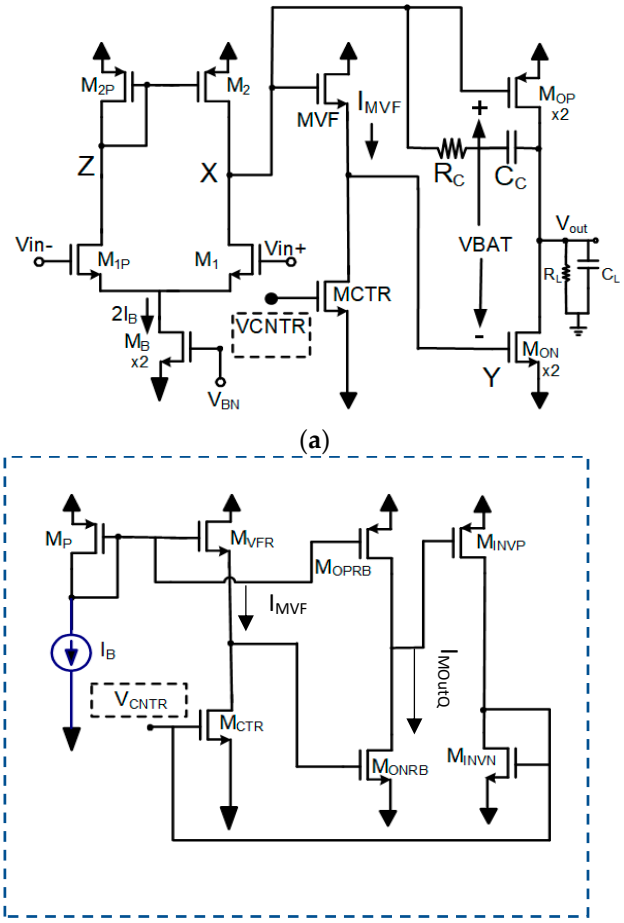

Figure 2. (**a**) Example of the class-AB output stage based on the floating battery principle using a VF with level shift and (**b**) a replica bias control circuit for the generation of VCNTR so that the quiescent output current has a nominal well-defined value independent of VDD, technology parameters, and temperature.

This paper introduces a simple scheme that overcomes the shortcomings discussed above, requiring minimal additional power dissipation and not increasing the supply requirements. This scheme is discussed in the next section. Traditionally, the performance of op-amps is compared using three well-known figures of merit: (a) the small-signal figure of merit $FOM_{SS} = f_u \cdot C_L / P_Q$, where f_u is the unity-gain frequency and P_Q is the quiescent power of the op-amp; (b) the large-signal static current efficiency figure of merit $FOM_{CEStat} = I_{outpkRL} / P_Q$; and (c) the large-signal dynamic current efficiency figure of merit $FOM_{CEDyn} = SR \cdot C_L / P_Q$, which is related to the maximum dynamic output current in load capacitance C_L. FOM_{CEStat} is determined by the maximum DC output current in the load resistor R_L (denoted $I_{outpkRL}$) relative to the total quiescent power P_Q of the op-amp. In addition, as both FOM_{SS} and FOM_{CEDyn} determine the ultimate speed of an op-amp, a new global figure of merit FOM_{Global} given by $FOM_{Global} = \sqrt{FOM_{SS} FOM_{CEDyn}}$ is also used here.

2. Circuit Description

The scheme of the proposed op-amp is shown in Figure 3a. A telescopic input stage is used in the first stage to achieve high gain even in the presence of a low-valued load resistor R_L (high loading conditions) that can degrade the second stage gain significantly. The proposed op-amp uses an auxiliary non-inverting amplifier with gain A_{aux} to generate a voltage variation V_Y, which is an amplified version of the variations in V_X, that is,

$V_Y = A_{aux}V_X$. This auxiliary amplifier consumes less than 10% of the op-amp's total bias current and does not increase supply requirements. The transistor-level implementation of the auxiliary amplifier is shown in Figure 3b. It uses a differential stage with resistive common-mode feedback (RCMFB) that has approximately a gain $A_{aux} = (g_{m4}R_{CMF})/2$, as shown in the analysis below. The auxiliary amplifier increases the op-amp's output negative current; the open-loop DC gain shifts the output poles to the higher frequency, allowing for a higher unity gain frequency. The quiescent voltage of V_Y has a value $V_{YQ} = V_{GSQM5P}$ independent of R_{CMF} (and of A_{Aux}). This allows to accurately control the quiescent current I_{OutQ} in the op-amp's output branch independent of the gain A_{aux}, supply voltage, technology parameters variations, and temperature changes. Given that the variations generated at V_Y are amplified with respect to those at Vx, M_{ON} can provide large negative output currents even though the amplitude of positive variations in V_X is smaller than that for negative variations. This overcomes one of the limitations of the conventional battery approach shown in Figure 1b.

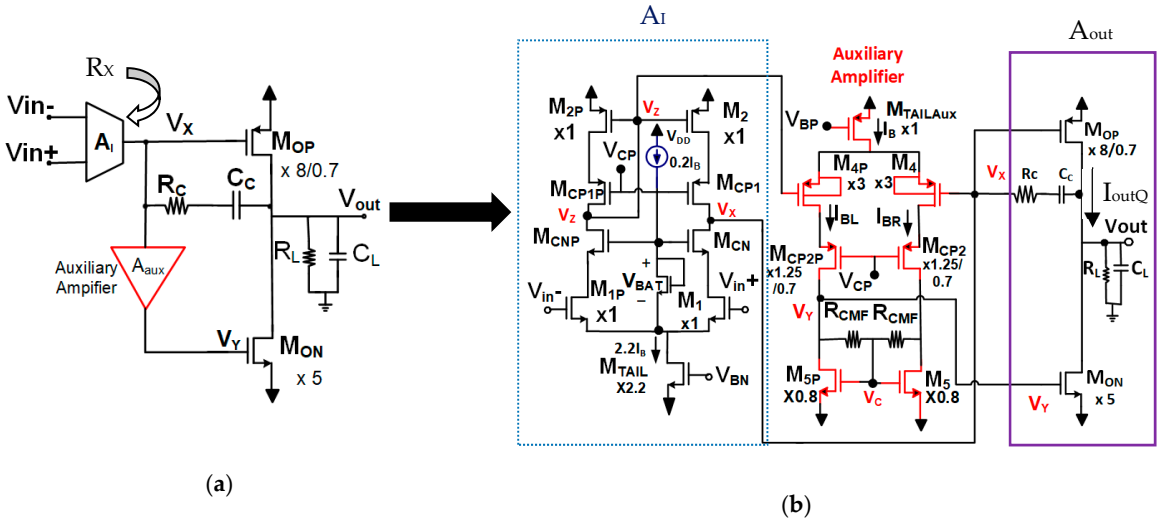

Figure 3. (**a**) Scheme of the proposed class-AB Miller op-amp and (**b**) transistor level implementation.

In order to prevent degradation of the phase margin of the op-amp, the value of R_{CMF} (and A_{aux}) is chosen in such a way that the pole at node Y is higher than the unity gain frequency f_u of the op-amp by at least a factor of 3. Thus, the selection of the optimal value of R_{CMF} is the crucial factor for the design of the proposed auxiliary amplifier. Larger values of R_{CMF} lead to enhanced negative output currents and gains, resulting in lower values for the pole at node Y and lower phase margin.

In the presence of positive signals in V_X larger than V_{SDsat4}, all of the tail current of $M_{TAILAUX}$ flows through M_{4P} and R_{CMF}. This causes a large positive voltage change at node V_Y that generates large negative op-amp output currents. In order to achieve similar peak positive and negative output currents with the selected value of R_{CMF}, the output transistors M_{ON} and M_{OP} are scaled by factor 5/1 and factor 8/0.7 with respect to the unit PMOS and NMOS transistors of size 10/0.27 used in the input stage. In addition, conventional Miller compensation is used to achieve stability.

2.1. Operation

The working principle of the proposed op-amp can be explained by considering its voltage follower operation. In the presence of the positive input signal V_{in}, the voltage at node V_X decreases and the voltage at node V_Y also decreases by a factor A_{aux}. As a result, M_{OP} provides a large positive current, and the drain current of M_{ON} decreases and eventually reaches zero. On the other hand, for negative input signals, the voltage at

node V_Y corresponds to the amplified version of the positive signals of node V_X, which is $V_Y = A_{aux}V_X$. As a result, M_{ON} can also provide large negative output currents.

2.2. Frequency Response

Conventional Miller compensation is used in the proposed op-amp. The proposed op-amp has one dominant pole ω_{pDOMX} at node V_X and two high-frequency poles ω_{pY} and ω_{pOut}. The zero ω_z approximately nullifies the effect of $\omega_{pOut.}$

Thus, the transfer function of the proposed op-amp is given by Equation (5).

$$H(s) \approx \frac{A_{OLDC}(1 + s/\omega_z)}{(1 + s/\omega_{pDOMX})\left(1 + s/\omega_{p_{Out}}\right)(1 + s/\omega_{pY})} \tag{5}$$

The gain of the first stage A_I is given by Equation (6).

$$A_I = g_{m1}R_X = g_{m1}\left(g_m {r_o}^2/2\right) \tag{6}$$

Here, for simplicity, g_m is the transconductance gain of all unit size NMOS and PMOS transistors, r_o is their output resistance, and R_X is resistance at node V_X. The auxiliary amplifier's gain is given by $A_{aux} = (g_{m4}R_Y)/2$, where $R_Y = r_{o4P} \cdot g_{mCP2P} r_{oCP2P} \left|\right| R_{CMF} \left|\right| r_{o5P}$. As $R_{CMF} << r_{o4P}, r_{oCP2P}, r_{o5P}$, $R_Y \approx R_{CMF}$ and $A_{aux} \approx (g_{m4}R_{CMF})/2$.

The gain of the output stage is given by Equation (7).

$$A_{Out} = \left(g_{mOP} + A_{aux}g_{mON}\right)R_{Out} \tag{7}$$

where R_{Out} is $R_{Out} = r_{oOP} \left|\right| r_{oON} \left|\right| R_L$.

Thus, the open-loop DC gain A_{OLDC} of the proposed op-amp is expressed by Equation (8).

$$A_{OLDC} = A_I A_{Out} = \left((g_m r_o)^2/2\right)\left(g_{mouteff}R_{Out}\right) \tag{8}$$

where $g_{mouteff} = g_{mOP} + A_{aux}g_{mON}$ and $R_{Out} = r_{OP} \left|\right| r_{ON} \left|\right| R_L$.

The dominant pole is at node V_X and is given by Equation (9).

$$f_{pDOMX} = 1/(2\pi R_X C_X) \tag{9}$$

where C_X is given by $C_X = (1 + |A_{out}|)\, C_C$.

Thus, the gain-bandwidth product (GBW) of the proposed op-amp is given by Equation (10).

$$\begin{aligned} GBW &= A_I A_{Out} \frac{1}{2\pi R_X (1+|A_{Out}|) C_C} \\ &= (g_{m1}A_{Out}) \frac{1}{2\pi (1+|A_{Out}|) C_C} \end{aligned} \tag{10}$$

Besides the dominant pole, the proposed op-amp has two high-frequency poles: one at V_Y and another at V_{Out}. The output high-frequency pole f_{pOut} is given in Equation (11).

$$f_{pOut} = \left(g_{mOP} + A_{aux}g_{mON}G_L\right)/(2\pi C_L) \tag{11}$$

The pole at node V_Y is expressed by Equation (12).

$$f_{pY} = 1/(2\pi R_Y C_Y) \tag{12}$$

where C_Y is given by $C_Y = C_{gsON} + C_{dBCP2P} + C_{dB5P} + C_{gdON}\left(1 + \left(\frac{A_{Out}}{A_{VY}}\right)\right) + C_{gd5P}$ and $R_Y = r_{o4p} \cdot g_{mCP2P} \cdot r_{oCP2P} \left|\right| R_{CMF} \left|\right| r_{o5P}$. The selection of R_{CMF} plays an important role in determining a compromise between the gain of the auxiliary amplifier and the phase margin of the op-amp. To achieve a sufficient phase margin, f_{PY} should be higher than the unity gain frequency of the op-amp. Thus, R_{CMF} has to be selected in such a way that the pole of the node Y, i.e., f_{PY}, is located at least a factor three higher than the op-

amp's unity gain frequency, and in that case, $R_{CMF} << r_{o5P}, r_{o4P} g_{mCP2P} r_{oCP2P}$ and R_Y can be approximated as $R_Y \approx R_{CMF}$. In this case, f_{PY} has a minor effect on the op-amp's frequency response up to the unity gain frequncy f_u, and Equation (12) can be simplified as below.

$$f_{pY} = 1/(2\pi R_{CMF} C_Y) \tag{13}$$

The zero is given by Equation (14).

$$f_z = 1/\left(2\pi C_C \left[R_C - \left(g_{mOP} + A_{Aux} g_{mON}\right)^{-1}\right]\right) \tag{14}$$

The simplified transfer function of the proposed op-amp neglecting the pole at node Y can be approximated by Equation (15).

$$H(s) \approx \frac{A_{OLDC}(1 + s/\omega_z)}{(1 + s/\omega_{pDOMX})(1 + s/\omega_{pOut})} \tag{15}$$

The small-signal model of the proposed op-amp is given in Figure 4.

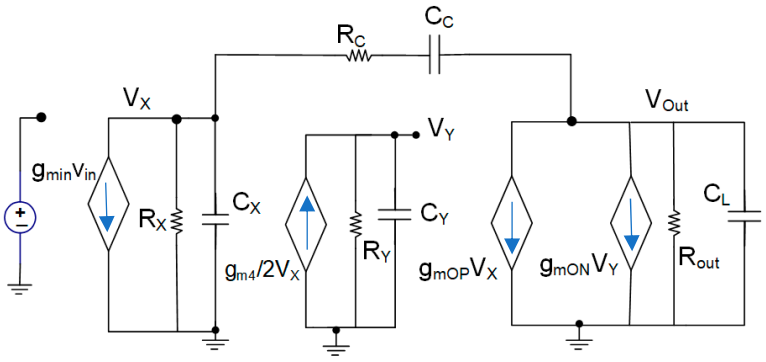

Figure 4. Small-signal model of the proposed op-amp.

3. Results

The proposed and conventional class-A op-amps are designed in 130 nm CMOS technology. The unit size transistors used in both op-amps are $(W/L)_N = (W/L)_P = 10/0.27$ (µm/µm). The compensation capacitor has a value $C_C = 4$ pF for both op-amps. The compensation resistor R_C has a value 8 kΩ for the proposed op-amp and 19 kΩ for the Conv-A op-amp. For a fair comparison, the output transistors of the Conv-A op-amp M_{OP} are scaled by the same factor 8/0.7 and M_{ON} is by the same factor 5/1 as the proposed op-amp compared to the unit size transistors used in the circuit. They are simulated using the same bias current $I_B = 15$ µA, and dual supply voltages $V_{DD} = +0.6$ V and $V_{SS} = -0.6$ V. Figure 5 shows the open-loop frequency response of the proposed op-amp. The proposed op-amp has open-loop gains $A_{OLDC} = 89.7$ dB with $R_L = 1$ MΩ and 57 dB with $R_L = 200$ Ω, and $C_L = 300$ pF in both cases. On the other hand, the conventional class-A(Conv-A) op-amp can provide a maximum A_{OLDC} of 75.8 dB for $R_L = 1$ MΩ and only 43.4 dB with $R_L = 200$ Ω. Figure 6 shows the corresponding frequency response of the Conv-A op-amp with $C_L = 300$ pF.

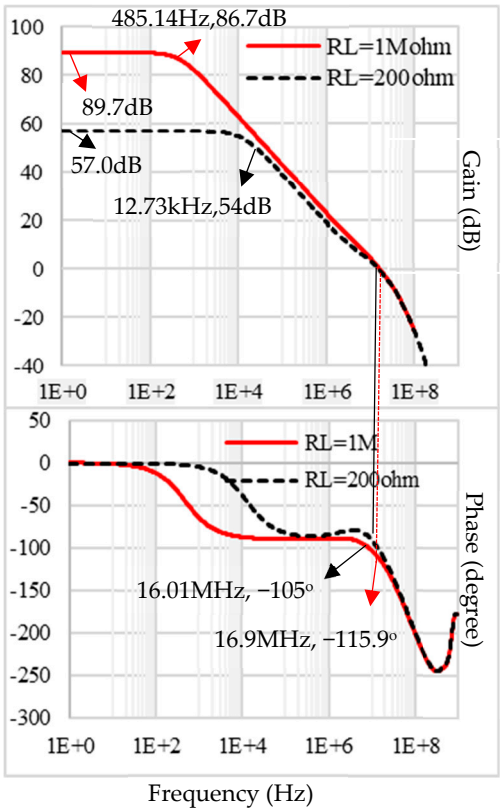

Figure 5. Frequency response of the proposed op-amp in open-loop configuration for RL = 1 MΩ and RL = 200 Ω.

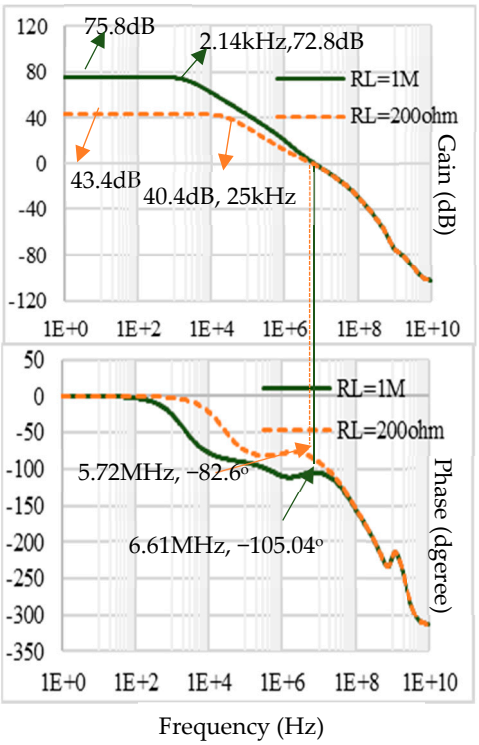

Figure 6. Open-loop frequency response of the Conv-A op-amp for R_L = 1 MΩ and R_L = 200 Ω.

The unity gain frequency f_u of the proposed op-amp for R_L = 1 MΩ is 16.9 MHz and for R_L = 200 Ω is 16.01 MHz. The small-signal figures of merit FOM_{SS} of the proposed

op-amp are 28.8 and 27.2 for R_L = 1 MΩ and 200 Ω. The Conv-A op-amp's FOM_{SS} for similar loading conditions are 12.4 and 10.8. Thus, the proposed op-amp can drive a low-value resistive load (high-loading condition) by maintaining a relatively high open-loop gain. It can be seen that, as expected, the introduction of the auxiliary amplifier in the proposed op-amp leads to lower gain degradation (and consequently, lower gain errors) for lower-valued load resistors.

Figure 7 shows the transient response of the proposed and Conv-A op-amp with R_L = 1 MΩ and C_L = 300 pF for a 500 kHz input pulse with 500 mVpp amplitude. It can be observed that the Conv-A op-amp cannot follow the input signal. From Figure 8, it can be asserted that this is because of the limitation of the peak negative output current, which corresponds to the quiescent current of the output branch in the Conv-A op-amp. From the pulse responses and load currents of the proposed and Conv-A op-amp for R_L = 1 MΩ, it can be asserted that the proposed op-amp increases the negative slew rate by a factor of 20 compared with the Conv-A op-amp. The SR enhances by a large factor close to 20 from 0.36 V/µs for the Conv-A to 7.4 V/µs for the proposed op-amp. Therefore, the CE of the proposed and Conv-A op-amps are 15.6 and 0.8, respectively.

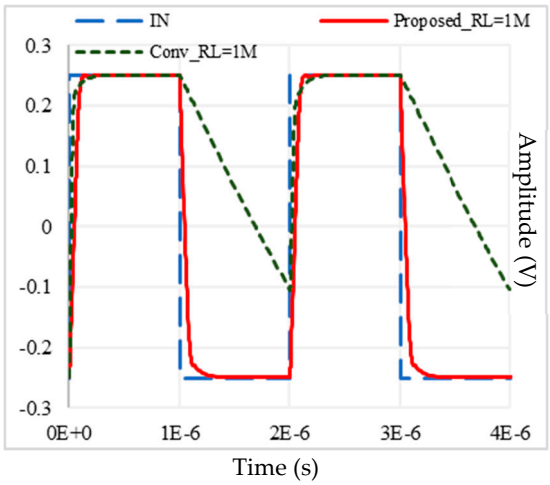

Figure 7. Transient response of the Conv-A and proposed op-amps for 500 kHz and 500 mV_{pp} amplitude input pulses with R_L = 1 MΩ and C_L = 300 pF.

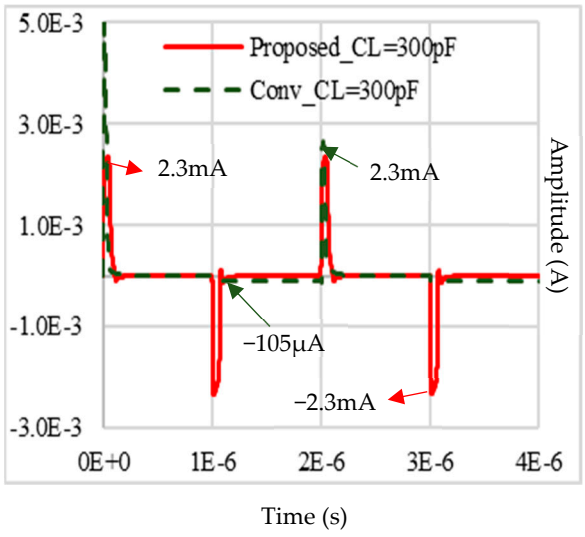

Figure 8. Current in the load capacitance C_L = 300 pF in the Conv-A and proposed op-amps for 500 kHz and 500 mV_{pp} amplitude pulse inputs.

From Figure 9, it can be asserted that the proposed op-amp can drive both large capacitive and low-valued resistive loads. Figure 10 shows the output current in the 200 Ω load resistor for the Conv-A and proposed op-amps for 500 mV_{pp} and 500 kHz input pulse. It can be seen that the proposed op-amp can provide 1.24 mA positive and negative peak output currents to a 200 Ω resistive load for a 500 mV_{pp} and 500 kHz input pulse. In contrast, the Conv-A op-amp with the same input signal can provide only a 105 µA negative output current, which is limited by the quiescent current of the output branch.

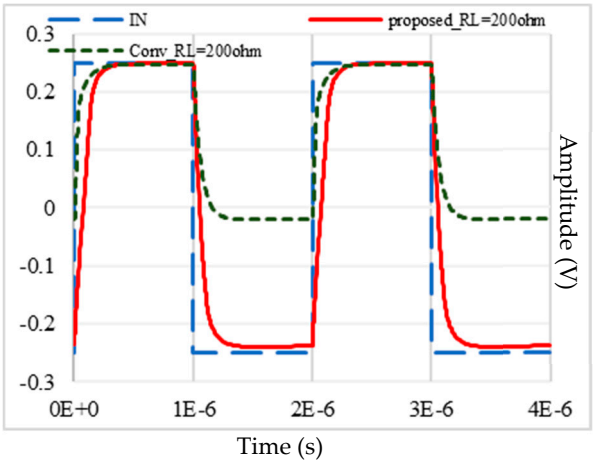

Figure 9. Transient response of the Conv-A and proposed op-amps for 500 kHz and 500 mV_{pp} pulse inputs with R_L = 200 Ω and C_L = 300 pF.

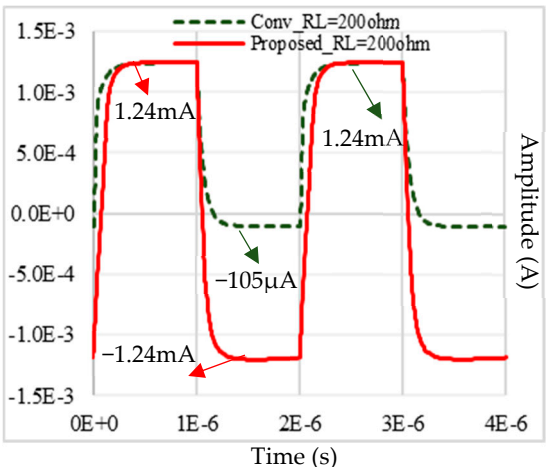

Figure 10. Current in R_L = 200 Ω in the Conv-A and Proposed op-amps 500 kHz and 500 mV_{pp} amplitude pulse inputs.

Figures 11 and 12 show the closed-loop frequency response of the proposed and Conv-A op-amps in the voltage follower configuration (VF). The proposed op-amp has 3 dB.

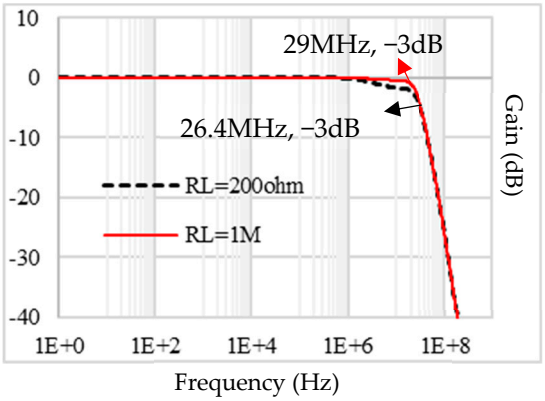

Figure 11. Frequency response of the proposed op-amp in a close-loop VF configuration for RL = 1 MΩ and RL = 200 Ω.

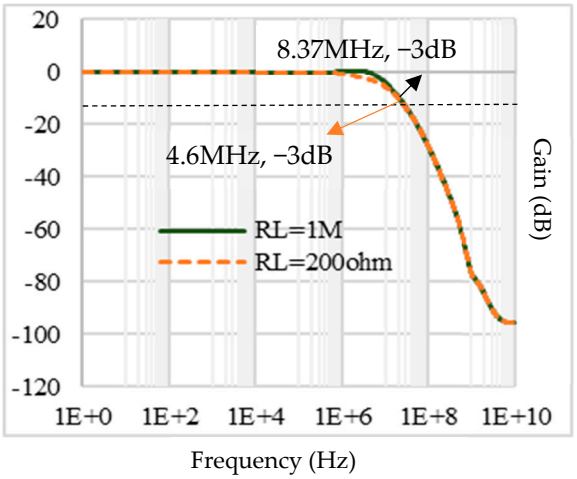

Figure 12. Closed-loop frequency response of the conventional class-A op-amp for R_L = 1 MΩ and R_L = 200 Ω in the VF mode.

The bandwidth (BW) is 29 MHz for R_L = 1 MΩ and 26.4 MHz for R_L = 200 Ω. In comparison, the Conv-A op-amp has 8.37 MHz and 4.6 MHz 3 dB bandwidths for similar loading conditions. It can be seen that the proposed op-amp has a higher bandwidth than the Conv-A op-amp.

A corner analysis of the proposed op-amp was performed to verify its robustness against temperature, process variations, and mismatches in the values of the design components. Table 1 shows the corner analysis of the op-amp employing typical 2% mismatches in the differential pair and the resistors used in the auxiliary amplifier. It can be asserted that, from the corner analysis, the proposed op-amp is robust against the temperature and process variations.

Figures of merit FOM_{CEDyn} and FOM_{CEStat} of the proposed op-amp are 12.6 and 7. FOM_{CEDyn} and FOM_{CEStat} of the Conv-A op-amp are 0.8 and 0.66. Thus, the proposed op-amp achieved 16 times higher FOM_{CEDyn} and 10.6 times higher FOM_{CEStat} than the Conv-A op-amp.

Table 1. Corner analysis of the op-amp at different temperatures.

	At T = 27 °C						At T = 120 °C						At T = −20 °C					
Corner	**tt**	**ff**	**fs**	**sf**	**ss**	**SD**	**tt**	**ff**	**fs**	**sf**	**ss**	**SD**	**tt**	**ff**	**fs**	**sf**	**ss**	**SD**
I_{TotalQ} (µA)	147	148	146	146	146	0.8	163	167	163	164	160	2.2	135	135	133	134	134	0.75
THD (dB) at R_L = 200 Ω	−66	−65	−66	−62	−60	2.4	−55	−50	−50	−49	−52	2.13	−65	−60	−61	−60	−62	1.9
f_u (MHz) at R_L = 200 Ω	16.9	17	16.7	16.7	16	0.3	11.62	11.12	11.36	11.59	11.83	0.24	19.14	19.4	19	18.9	18.4	0.33
PM (°) at R_L = 1 MΩ	64.1	63	65	65	67	1.31	70	68	72	69	68	1.5	62	62	60	62	64	1.26
Gain	90	87.7	89.4	85.7	90	1.65	74	70	78	71	79	3.6	91.3	90.7	91.5	90.3	90	0.57
SR (V/µs)	7.4	7	7.1	7.7	7.1	0.25	7	7.09	7.6	7.3	7.9	0.3	7.3	7.7	7.4	7.2	6.9	0.26
$I_{outpk}{}^{-}R_L$ = 200 Ω (mA)	1.24	1.23	1.24	1.23	1.24	0.004	1.19	1.2	1.21	1.15	1.20	0.02	1.24	1.23	1.1	1.25	1.24	0.06

Comprehensive comparisons of the proposed op-amp's performance with state-of-the-art op-amps and Conv-A op-amp are shown in Table 2. The proposed op-amp has the highest small-signal, dynamic, static current efficiency, and global figures of merits. It can be asserted that, from the comparison table, the proposed architecture can drive both resistive and capacitive load efficiently. The presence of the auxiliary amplifier in the prosed architecture makes this possible.

Table 2. Summary of the results and performance comparison.

Parameter (Units)	**Proposed**	**Conv-A**	**[8] 2020**	**[9] 2016**	**[10] 2016**	**[11] 2019**	**[12] 2017**	**[13] 2019**	**[14] 2020**
Inversion level	SI	SI	SI	SI	SBT	SI	SBT	SI	SBT
CMOS process (µm)	0.13	0.13	0.5	0.18	0.18	0.18	0.35	0.18	0.18
Supply voltage (V)	±0.6	±0.6	1.2/2/2.5	1.8	0.7	1.8	0.9	1.8	±0.3
Capacitive load (pF)	300	300	16	200	20	100	10	5	10
Resistive Load (Ω)	1 M/200	1 M/200	-	-	-	-	-	1 k	-
SR (V/µs)	7.4	0.36	3.9/4.3/4.3	74.1	2.8	51	0.25	13.25	8.4
DC gain (dB)	89.7/57	75.8/43.44	69/70/70	72	57.5	98	65	105.5	42.2
PM (°)	64.1/76	75/97	58/58/58.5	50	60	71	60	53	54
f_u (MHz)	16.9/16.0	6.6/5.72	8.3/8.4/8.5	86.5	3	21	1	231.7	16.1
CMRR at DC (dB)	71 at R_L = 1 M	52 at R_L = 1 M	69/70/64	NA	19	-	45	-	85.12
PSRR + at DC (dB)	109 at R_L = 1 M	69 at R_L = 1 M	73/73/73	NA	52.1	-	-	-	53.25
PSRR − at DC (dB)	99 at R_L = 1 M	57 at R_L = 1 M	73/73/72	NA	66.4	-	-	-	56.89
$I_{Outpk}{}^{+}{}_{RL = 200\ \Omega}$ (µA)	1241	1241	-	-	-	-	-	1200	-
$I_{Outpk}{}^{-}{}_{RL = 200\ \Omega}$ (µA)	1241	105	-	-	-	-	-	-	-
I_{totQ} (µA)	147	133	162/166/168	6611	36.3	1666.7	27	472	41.33
Power (µW)	176	159.6	244/332/420	11900	25.4	3000	24.3	850	24.8
FOM_{CEDyn} (V.pF/µs.µW)	12.6	0.8	0.25/0.21/0.16	1.25	2.2	1.7	0.1	0.078	3.3
FOM_{SS} (MHz.pF/µW)	28.8/27.2	12.4/10.8	0.54/0.4/0.3	1.45	2.36	0.7	0.4	1.4	6.49
FOM_{CEStat} (µA/µW)	7	0.66	-	-	-	-	-	1.4	-
FOM_{Global}	19	3	0.4/0.29/0.22	1.34	2.27	1.09	0.2	1.4	4.6

SI, strong inversion; SBT, sub-threshold.

4. Conclusions

A simple class-AB Miller op-amp that can drive both resistive and capacitive loads is presented here. A compact auxiliary amplifier is used to provide the static class-AB operation and helps to achieve higher gain, bandwidth, and a well-defined output quiescent current. The proposed op-amp can provide a 13.9 dB higher open-loop gain, a factor 20 higher slew-rate, and a factor 3.3 to 5.7 higher bandwidth (in VF configuration) than the conventional op-amp at the expense of only 10% additional quiescent current compared to the Conv-A op-amp.

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References

1. Cruz, S.C.D.; Reyes, M.G.T.D.; Gaffud, T.C.; Abaya, T.V.F.; Gusad, M.T.A.; Rosales, M.D. Design and implementation of operational amplifiers with programmable characteristics in a 90 nm CMOS process. In Proceedings of the 2009 European Conference on Circuit Theory and Design, Antalya, Turkey, 23–27 August 2009; pp. 209–212.
2. Razavi, B. *Design of Analog CMOS Integrated Circuits*; McGraw-Hill: New York, NY, USA, 2001.
3. William, S.M.C. *Analog Design Essentials*; Springer: New York, NY, USA; Berlin, Germany, 2006.
4. Monticelli, D.M. A quad CMOS single-supply op amp with rail-to-rail output swing. *IEEE J. Solid State Circuits* **1986**, *21*, 1026–1034. [CrossRef]
5. De Langen, K.-J.; Huijsing, J. Compact low-voltage power-efficient operational amplifier cells for VLSI. *IEEE J. Solid State Circuits* **1998**, *33*, 1482–1496. [CrossRef]
6. Gregorian, R.; Temes, G.C. *Analog MOS Integrated Circuits for Signal Processing*; Wiley Series on Filters: Design Manufacturing and Applications; Wiley-Interscience: New York, NY, USA, 1986.
7. Torralba, A.; Carvajal, R.G.; Ramirez-Angulo, J.; Tombs, J.; Galán, T. Class AB output stages for low voltage CMOS opamps with accurate quiescent current control by means of dynamic biasing. In Proceedings of the ICECS 2001 8th IEEE International Conference on Electronics, Circuits and Systems (Cat. No.01EX483), Malta City, Malta, 2–5 September 2001; Volume 2, pp. 967–970. [CrossRef]
8. Padilla-Cantoya, I.; Molinar-Solis, J.E.; Medina-Vazquez, A.S.; Gurrola-Navarro, M.A.; Rizo-Dominguez, L.; Gutierrez-Frias, E.F. Class AB Op-Amp with Accurate Static Current Control for Low and High Supply Voltages. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, 1. [CrossRef]
9. Sutula, S.; Dei, M.; Terés, L.; Serra-Graells, F. Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OTAs for Low-Power SC Circuits. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1101–1110. [CrossRef]
10. Cabrera-Bernal, E.; Pennisi, S.; Grasso, A.D.; Torralba, A.; Carvajal, R.G. 0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1807–1815. [CrossRef]
11. Anisheh, S.M.; Abbasizadeh, H.; Shamsi, H.; Dadkhah, C.; Lee, K.-Y. 98-dB Gain Class-AB OTA with 100 pF Load Capacitor in 180-nm Digital CMOS Process. *IEEE Access* **2019**, *7*, 17772–17779. [CrossRef]
12. Grasso, A.D.; Pennisi, S.; Scotti, G.; Trifiletti, A. 0.9-V Class-AB Miller OTA in 0.35µm CMOS with Threshold-Lowered Non-Tailed Differential Pair. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 1740–1747. [CrossRef]
13. Kuo, P.-Y.; Tsai, S.-D. An Enhanced Scheme of Multi-Stage Amplifier with High-Speed High-Gain Blocks and Recycling Frequency Cascode Circuitry to Improve Gain-Bandwidth and Slew Rate. *IEEE Access* **2019**, *7*, 130820–130829. [CrossRef]
14. Renteria-Pinon, M.; Ramirez-Angulo, J.; Diaz-Sanchez, A. Simple Scheme for the Implementation of Low Voltage Fully Differential Amplifiers without Output Common-Mode Feedback Network. *J. Low Power Electron. Appl.* **2020**, *10*, 34. [CrossRef]