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Design and Optimization of an Ultra-Low-Power Cross-Coupled LC VCO with a DFF Frequency Divider for 2.4 GHz RF Receivers Using 65 nm CMOS Technology

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Abstract: This article presents the design and optimization of a tunable quadrature differential LC CMOS voltage-controlled oscillator (VCO) with a D flip-flop (DFF) frequency divider. The VCO is designed for the low-power and low-phase-noise applications of 2.4 GHz IoT/BLE receivers and wireless sensor devices. The proposed design comprises the proper stacking of an LC VCO and a DFF frequency divider and is simulated using a TSMC 65 nm CMOS technology, and it has a tuning range of 4.4 to 5.7 GHz. The voltage headroom is preserved using a high-impedance on-chip passive inductor at the tail for filtering and enabling true differential operation. The VCO and frequency divider consume as low as 2.02 mW altogether, with the VCO section consuming only 0.47 mW. The active area of the chip including the pads is only 0.47 mm^2. The designed VCO achieved a much better phase noise of −118.36 dBc/Hz at a 1 MHz offset frequency with 1.2 V supply voltages. The design produced a much better FoM of −196.44 dBc/Hz compared to other related research.

Keywords: CMOS; quadrature; differential; DFF frequency divider; phase noise; quality factor; varactor; Inductor Capacitor voltage-controlled oscillator (LC-VCO); layout

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1. Introduction

The proliferation of mobile phones and the establishment of cellular networks revolutionized personal communication. The 21st century witnessed the emergence of 3G, 4G, and 5G wireless networks, enabling faster data transfer and the growth of the mobile internet. Wireless communication has continued to evolve, with innovations in areas like Wi-Fi, Bluetooth, and IoT (Internet of Things) communication. These technologies have become integral to daily life and various industries. The advent of Wi-Fi, Bluetooth low energy (BLE), and the subsequent growth of IoT (Internet of Things) devices has had a significant impact on the way we live, work, and interact with technology. The number of Internet of Things (IoT) devices and connected objects has grown significantly in recent years. Examples include automation systems for homes, smart appliances, smart agriculture systems, smart healthcare systems, wireless sensors, wearable technology, etc. The transportation, logistics, healthcare, life, and digital industries are all being improved with the emergence of intelligent, wirelessly interconnected objects. It is anticipated that billions of devices with sensor will be linked to the Internet through diverse access networks. Cisco's IoT Connections Count Forecast estimated that there would be over 36 billion connected IoT devices by 2025. The future of wireless communication holds the promise of even faster and more reliable networks, expanded IoT applications, and the integration of wireless technology into areas like autonomous vehicles and smart cities.

The proliferation of IoT devices, many of which rely on 2.4 GHz devices like Wi-Fi and Bluetooth low energy (BLE) for connectivity, has been revolutionary. These devices are embedded in our homes, industries, transportation systems, and cities. They collect

data, automate tasks, and enhance efficiency and convenience. Implementing economical, low-power, and adaptable systems is a significant necessity for these devices. The IoT sensor node needs to be mobile, battery-operated, and perhaps able to retain energy for several years. It is a crucial element of IoT systems, and it mostly influences the system's performance. Therefore, the transceiver RF must adhere to strict power limitations. The most important part of every RF transceiver is the voltage-controlled oscillator (VCO).

A substantial amount of the power budget is used by the VCO. The key challenge in this endeavor is reducing the power consumption.

The leading idea of this article is to produce a design that has low phase noise, low power consumption, accurate quadrature oscillation, and a better frequency tuning range with a reduced chip size. In this regard, we adopted the best technique of a VCO and frequency divider and integrated them at their optimal level. It has been used to satisfy the requirements of IoT applications: autonomy, stability, and frequency agility.

Wireless communication has become a ubiquitous part of our daily lives, and the demand for low-power, cost-effective, and secure RF transceivers has increased dramatically with the emergence of the Internet of Things (IoT) and other wireless applications.

The use of advanced techniques by RFIC designers has resulted in improved efficiency for RF transceivers. These techniques have allowed for the integration of more functionality onto a single chip, resulting in more efficient, reliable, and cost-effective wireless communication systems. The complete system-on-chip (SoC) design approach enables the integration of numerous components, including RF transceivers, onto a single chip, resulting in decreased power consumption and cost.

In this article, the LC tank complementary cross-coupled differential voltage-controlled oscillator (VCO) technique is used to achieve perfect symmetry between the quadrature outputs of an oscillator. This technique addresses the intrinsic asymmetry issue in current reusing and ensures an accurate quadrature phase relationship, leading to improved performance in RF transceivers.

In article [1], comparative analyses were conducted on various LC oscillator topologies, including Colpitts, Hartley, and common-source cross-coupled differential pairs, in the frequency range of 1 to 100 GHz. The circuits were implemented in 28 nm bulk CMOS technology to operate at different frequencies while maintaining equal power consumption, quality factor, and transistor sizes for a fair comparison. The impulse sensitivity function was accurately evaluated with all the necessary steps and settings discussed in detail. Additionally, PN performances were assessed through periodic steady-state simulations in the Spectre RF-Cadence environment.

The quadrature differential cross-coupled LC oscillator and the VCO Ring Oscillator are the two most prevalent kinds of integrated oscillators. Both types have their advantages and disadvantages, which make them more suitable for specific applications. Ring oscillators are so widely used because of their low power consumption and small size, which make them ideal for many applications where these factors are critical. The ring oscillator's phase noise performance is inferior to that of quadrature differential cross-coupled LC oscillators in applications where phase noise is an important characteristic. On the other hand, quadrature differential cross-coupled LC oscillators are preferred for systems that require high data rates and low bit error rates. They perform better in terms of phase noise than ring oscillators in RF applications demanding high-quality signals. However, they may require more area and consume more power compared to ring oscillators.

Due to their low power usage, improved phase noise performance, and straightforward implementation, LC tank VCO techniques and quadrature differential cross-coupled LC oscillator techniques are frequently used in high-performance RF and wireless communication systems. Their unique topologies and careful selection of components make them ideal for a wide range of applications. Those require high-speed data transfer rates, low bit error rates, and low power consumption [2]. When compared to a quadrature VCO, the approach of operating the VCO at twice the LO frequency and then $\frac{1}{2}$ division is often used to cover less chip space [3].

A power-efficient method for reusing current is the LC VCO followed by a 1/2 frequency divider circuit. When oscillation amplitude is decreased, the voltage headroom for each MOS is likewise decreased, which results in more phase noise than a separated VCO and divider. To minimize the trade-off between voltage headroom and power usage, VCO and frequency divider circuits must be carefully designed together [4].

1.1. Quadrature Generation VCO

Direct conversion transceivers are commonly used in modern radio systems. They offer a simpler architecture compared to other types of transceivers, such as super heterodyne transceivers, which require multiple stages of frequency conversion and filtering. Quadrature down-conversion is necessary for recent modern radio systems to reject the image signals in direct conversion and low-IF receivers. Both the Colpitts and LC oscillators can produce quadrature signals; however, the Colpitts oscillator performs worse concerning phase noise as compared to the LC oscillator [5,6].

To generate quadrature signals, the VCO usually employs a coupling network, such as a quadrature LC tank or a pair of coupled resonators, which provides the necessary phase shift between the two outputs. However, this coupling network can introduce additional phase noise, which can degrade the overall phase noise performance of the VCO. This demonstrates that a traditional parallel-coupled QVCO outperforms a single-phase VCO in terms of phase noise due to the coupling transistors being connected in parallel with the switching pairs, which causes a non-zero resonator phase shift and reduces the phase noise of the QVCO. A trade-off between phase noise and phase accuracy led to this coupling approach. [7]. Secondly, the QVCO design acquires more chip area as compared to a single VCO [4,8–10].

The most precise quadrature LO signals across a broad frequency range are produced using a double-frequency VCO using a 1/2 frequency divider technique. Increased power consumption was a result of this technique of high operating frequency for the VCO and frequency divider. However, the master–slave flip-flops, which have to be designed for the doubled frequency, consume much power. If the primary design concern is low cost or small area, then this solution clearly must be preferred, as the VCO designed at double frequency features a smaller coil, and the area of the master–slave flip-flops in sub-µm CMOS is negligible. Also, in ZERO-IF receivers, this solution should be preferred because it avoids direct parasitic coupling between the VCO and receiver input. There is a tradeoff between power consumption and phase noise and this technique will provide better phase noise [2].

The leading idea of this article is to produce a design that provides better phase noise, low power consumption, accurate quad oscillation, and a better frequency tuning range with a reduced chip size. In this regard, we adopted the best technique of the VCO and frequency divider and integrated them at their optimal level. The proposed VCO technique naturally provides an output CM level about equal to VDD/2. The technique can be viewed as complementary cross-coupled CMOS (NMOS and PMOS pair) sharing the same bias current. Instead of using a CMOS current source at the tail of the structure, we used a high-impedance passive inductor to save the voltage headroom and reduce the noise factor. To maximize the tuning range, we carefully selected the CMOS dimensions as mentioned in the article's design methodology in Section 3.1. More than fifty iterations were carried out during the design, integration, and simulation process by using TSMC 65 nm with a 1 poly and 9 metals (1P9M) CMOS process in the Cadence Virtues CAD environment. This article's results show that we achieved better phase noise, ultra-low power consumption, and better quad oscillation with the reduced chip area as compared to other related work.

1.2. The Contribution

The main objective of our work is to further reduce the phase noise and power consumption along with a reduced chip size. The proposed technique achieves phase noise as low as −118.36 dBc/Hz at a 1 MHz offset frequency with 1.2 V supply voltages and

consumes only 0.47 mW of power. The proposed technique consumed 76% less power as compared to the latest related work published in [11]. The active area of the chip including the pads is only 0.47 mm^2; furthermore, in the proposed design, we used a DFF master–slave $\frac{1}{2}$ frequency divider to obtain the accurate quadrature oscillation.

In this article, we used TSMC 65 nm with 1 poly and 9 metals (1P9M) CMOS technology in a Cadence Virtues CAD environment for the VCO schematic design, simulations, layout, and post-layout simulations. This article is structured in four sections. Section 2 of the paper discusses the LC-VCO and frequency divider designs. Section 3 presents the results of the post-layout simulation employing 0.65 m CMOS technology and its comparisons. Section 4 of the paper describes a brief conclusion.

2. Literature Review

Commonly Used Techniques in Traditional Low-Voltage LC-VCO

To reduce phase noise in cross-coupled oscillators, many research efforts have been carried out in recent years, each of which has distinct advantages and disadvantages. In an earlier study, by improving the resonator's design, the researchers also attempted to reduce phase noise as discussed in [12–14]. In [10], an active resonator with a high Q factor was used to minimize phase noise. In [13,14], the study's findings were that the oscillator's phase noise efficiency can be enhanced by increasing the inductance energy factor (IEF). In [15], the tail current shaping technique was used to manage tail current and improve phase disturbance.

One of the most popular types of oscillators is the quadrature differential cross-coupled LC tank oscillator, as they have advantages including better phase noise performance, less power consumption, and simple and straightforward designs, as reported in [7,16–18]. However, the researchers faced significant design challenges while trying to obtain lower phase noise in these oscillators. The analysis and prediction of phase noise or timing jitter in oscillators is a particularly difficult problem, since oscillators are independent non-linear circuits and their non-linearity is essential to their operation and evaluation of their noise performance. Along with LC tank loss, the MOSFET switching pairs and tail biasing MOSFET also produced some noise in this kind of oscillator.

Traditionally, PMOS or NMOS devices, or both together, could be utilized to produce a quadrature differential cross-coupled pair (CMOS). The quadrature differential cross-coupled MOS oscillator consumes less power, but the phase noise is increased because of noise from the extra cross-coupled block as compared to a single MOSFET. However, the power consumption of the CMOS circuit is almost half that of single pair topologies [6,15].

The complementary quadrature differential cross-coupled is the widely used technique of the LC–VCO presented in [2,12]. The circuit employs two MOSFETs to provide negative transconductance ($-gm$), which compensates for LC tank losses. It lessens the $1/f$ noise and has a symmetric and straightforward structure. However, due to the tail current source's limited voltage headroom, this configuration is inappropriate for low-supply voltage operation. A different method employed in [16] is effective for low-power applications. In a typical quadrature differential cross-coupled VCO, cross-connected PMOS and NMOS transistors produce the same negative conductance because of half-power dissipation. Since there is no tail current circuit, this architecture will not impact the headroom. Furthermore, because of its low power supply voltage and lack of a tail MOS current source in its design, this VCO is more sensitive to PVT changes. It has been reported in [19] that the VCO's performance would be improved by increasing its tolerance to PVT fluctuations by adopting an adaptive body-biasing approach.

The capacitive source degeneration (CSD) technique is used to improve the phase noise performance of an LC oscillator. In the CSD technique, a capacitor is placed in series with the input signal source of the LC tank, which provides a negative feedback path that reduces the amplitude of the oscillation signal. This reduces the non-linearity of the oscillator and improves its phase noise performance, as reported in [15,20,21]. Due to the improper selection of degeneration capacitors, the primary downside to this approach

is that it lowers the resonator's effective quality factor and hurts phase noise. The noise source is increased by placing an active MOS device in the tail. This technique lowers the thermal noise of the tail current by filtering several tail current harmonics through the source capacitor.

The researcher completed a lot of work to reduce the phase noise, like a traditional current source, which utilizes RC for noise filtering, tail filtering using LC, and sinusoidal noise shaping. All these techniques have some trade-offs. For example, by employing the notch filter feature of the LC circuitry, the second harmonic of the tail current noise can be eliminated. To prevent an increase in both the noise injected into the tank and the tank loss, sinusoidal noise shaping requires an external bias voltage and, respectively, larger resistors, as reported in [15,22].

This work aims to address some of the limitations that are associated with LC-VCO design, including the effect of the LC tank, a tail-active MOS device for the current source, large resistance at the tail, or the unsuitable selection of a degeneration capacitor. These limitations may negatively impact the performance of the LC-VCO. The LC-VCO is discussed in the next section, which may involve various techniques or strategies to address the identified limitations and describe the circuit diagram, components, parameters, or equations used in the design process. Additionally, we compare the suggested LC-VCO's performance to other methods that are already in use or gauge its main characteristics, such as frequency stability, phase noise, power consumption, or tuning range [6,23].

3. Design Methodology

3.1. The Proposed Circuit Design

In this article, a differential quadrature differential cross-coupled PMOS and NMOS LC-VCO with a tail inductor D flip-flop (DFF) frequency divider is proposed. In the design, the quadrature differential cross-coupled CMOS architecture is used to provide high linearity and low phase noise performance.

The cross-coupled architecture ensures that the output signals have a 180-degree phase difference between the complementary outputs, which improves the circuit's linearity. The differential architecture also provides a high common-mode rejection ratio (CMRR), which reduces the impact of common-mode noise on the output signals. The DFF frequency divider is used to divide the frequency of the output signals by a factor of two. The output of the VCO is connected to the clock input of the DFF, and the divided output signals are obtained from the Q and Q' outputs of the DFF. The use of a frequency divider allows the circuit to generate two signals with a 90-degree phase difference at a frequency that is half the frequency of the VCO output.

Here are some key design aspects to consider when implementing this VCO:

Differential cross-coupling: The VCO employs two pairs of PMOS and NMOS transistors that are cross-coupled differentially to create a positive feedback loop. Cross-coupling topology is designed to provide sufficient feedback to achieve the desired oscillation frequency and phase noise performance.

LC tank design: The resonant frequency and Q factor of the LC tank are critical parameters that determine the output frequency and phase noise performance of the oscillator. The tank should be designed with an appropriate inductance and capacitance to achieve the desired resonant frequency and Q factor.

Tail inductor design: The tail inductor is an additional inductor that is connected to the common source node of the differential transistors. It provides additional negative feedback to improve the oscillator's phase noise performance. The tail inductor is designed with an appropriate inductance value and quality factor to achieve optimal performance.

Transistor sizing and biasing: The PMOS and NMOS transistor sizes are appropriately chosen to achieve the desired oscillation frequency and phase noise performance. The biasing conditions of the transistors are chosen carefully to ensure optimal power consumption and linearity.

Parasitic elements: Parasitic elements, such as resistance and capacitance, can have a significant impact on the oscillator's performance. These elements can contribute to power consumption, noise, and frequency stability. It is important to carefully account for these parasitic elements in the design and layout of the oscillator.

3.2. A Quadrature Differential Cross-Coupled LC VCO Is Proposed

In this structure, a VCO design is intended for use in 2.4 GHz IoT/BLE devices such as direct conversion, low IF receivers, or WSN sensors. The design replaces the tail MOS transistor with a high-quality factor inductor to reduce tail noise effects and improve the effective quality factor of the LC tank. The VCO operates at twice the needed LO frequency and is followed by a frequency divider's bias current. The design is aimed at achieving accurate quadrature signal generation while consuming low power.

Figure 1 depicts the proposed VCO, which features the high-quality factor inductor in place of the tail transistor. This modification results in a reduction in the tail noise current and an increase in the effective quality factor of the LC tank, thereby improving the overall performance of the oscillator. The VCO is designed to operate at 2.4 GHz, making it suitable for use in IoT/BLE devices. Its power-efficient design and accurate quadrature signal generation make it well-suited for low-power wireless applications.

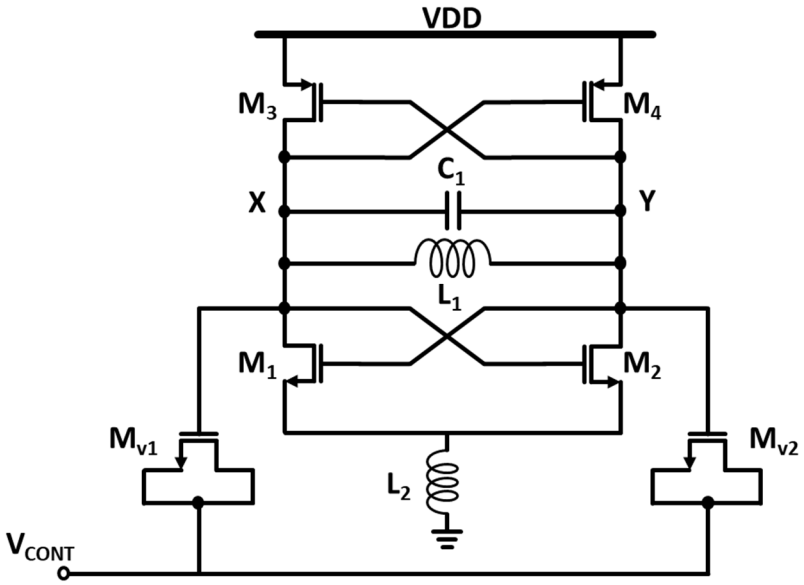

Figure 1. The schematic of the proposed differentially quadrature differential cross-coupled PMOS and NMOS LC-VCO with a tail inductor.

The proposed technique is based on two back-to-back quadrature differential cross-coupled inverting CMOSs along with a high impedance inductor at the tail for biasing, and provides truly differential operation. The bias current is reused by the PMOS devices, which provide high transconductance, and the quadrature differential cross-coupled NMOS and PMOS pair shares the same current. However, it offers double the voltage swing, which places points X and Y at VDD/2 at the CM level. The capacitive varactors are used to adjust the resonance frequency; the LC tank is employed to reach the desired frequency. The on-chip high Q integrated inductor is used to reduce losses in the LC tank.

In the proposed design technique, the PMOS transistors utilize the bias current to increase transconductance. However, a more significant benefit of other LC topologies, such as traditional two LC tanks with just NMOS quadrature differential cross-coupled VCOs and top-biased LC tank quadrature differential cross-coupled VCOs, is that they provide double the voltage swing for a given bias current and inductor design. To comprehend this issue, we suppose that L1 and L2 in a traditional two-tank circuit correspond to LXY in

the complementary architecture. Consequently, LXY displays an equal parallel resistance of 2Rp.

The design of the proposed VCO consists of a pair of PMOS and NMOS transistors coupled back-to-back to form differential complementary CMOS architecture. The PMOS transistors staked at top of the circuit provide a high transconductance. This approach anticipates an output common-mode (CM) level equal to VDD/2. The suggested technique yields double the voltage swing for a given bias current as compared to typically only NMOS, PMOS, or LC CMOS pairs. The nodes LXY present an equivalent parallel resistance of 2Rp. In the design, a high-impedance inductor is introduced at the tail of the VCO for biasing instead of the conventional MOS current source. This induction of the inductor is used to block the 1/f noise to enhance spectral purity. This technique will save the voltage headroom of the supply voltage. Furthermore, due to no 1/f noise, the phase noise was also reduced, as reflected in the results.

The paragraph describes the role of the passive high-impedance tail inductor in the performance of the VCO. The high-impedance inductor is placed at the tail for filtering purposes and to preserve voltage headroom while ignoring frequency modulation. Traditionally, the output common-mode (CM) level is modulated by the capacitances of the varactors, which are cross-coupled with a MOSFET current source at the tail for biasing. This can result in poor phase noise due to the modulation of the CM level. However, the article addresses this issue by replacing the MOS current source with a high-quality factor inductor at the tail. This modification reduces the phase noise and improves the performance of the VCO.

The MOS varactor is occupied as a PN junction, with Mvar1 and Mvar2 appearing parallel to the tanks. The two factors that determine a varactor's performance are (a) the capacitance range, or the ratio between the maximum and minimum capacitances it can deliver as the applied voltage varies, and (b) the quality factor, which is constrained by the series resistance within the varactor structure [22]. As a consequence of the high impedance inductor at the tail, the design saves the voltage headroom, lowers phase noise, and ignores frequency modulation. Because the complementary structure has quadrature differential cross-coupled pairs of PMOS and NMOS transistors, which are useful in deep submicron CMOS technologies, it exhibits resilience to process changes. The capacitance of M_{V1} and M_{V2} reduces when V*cont* increases from zero to VDD because their gates are operating at an average level equal to VDD, maintaining a positive gate-source voltage. This behavior persists even when there are significant voltage fluctuations across M_{V1} and M_{V2} and at X and Y. The control voltage (V*cont*) across each varactor varies from zero to VDD. There is a monotonic decrease in the varactor's capacitances which is observed as the control voltages increase. Hence, the oscillation frequency may be written as,

$$\omega_{osc} = \frac{1}{\sqrt{L1(C1 + Cvar)}} \quad (1)$$

Cvar is the average capacitance of each varactor.

In the case of the proposed LC-VCOs, the RF circuit sizing tool was used to optimize the circuit performance by exploring various design parameters such as the sizes of the transistors, capacitors, and inductors, and their respective placements in the circuit. The goal was to achieve the desired performance specifications, such as frequency stability, phase noise, and power consumption while minimizing the impact of noise and other sources of interference. There are boundaries for design variables (transistor width, length, bias current, inductor value, Q factor (size), and varactor (control voltages and capacitance value)).

The design methodology described here involves optimizing the components of a voltage-controlled oscillator (VCO), including the inductor, varactor, and active circuit. The focus of the optimization process is to improve the power consumption and phase noise performance of the VCO.

The merit of paper is to design an ultra-low-power VCO. The design methodology emphasizes the importance of optimizing each component of the VCO to meet the required performance parameters. By optimizing the inductor, varactor, and active circuit, it is possible to enhance the VCO's phase noise and power consumption efficiency overall. The design flow is to be considering a part of optimizing the overall design of the VCO. To improve the design, three key considerations have been taken into account, as is shown below in Figure 2. To reduce the resistive loss (gL) and increase the quality factor, the inductor must first be tuned, after which the varactor needs to be optimized, and then the active circuit needs to be optimized.

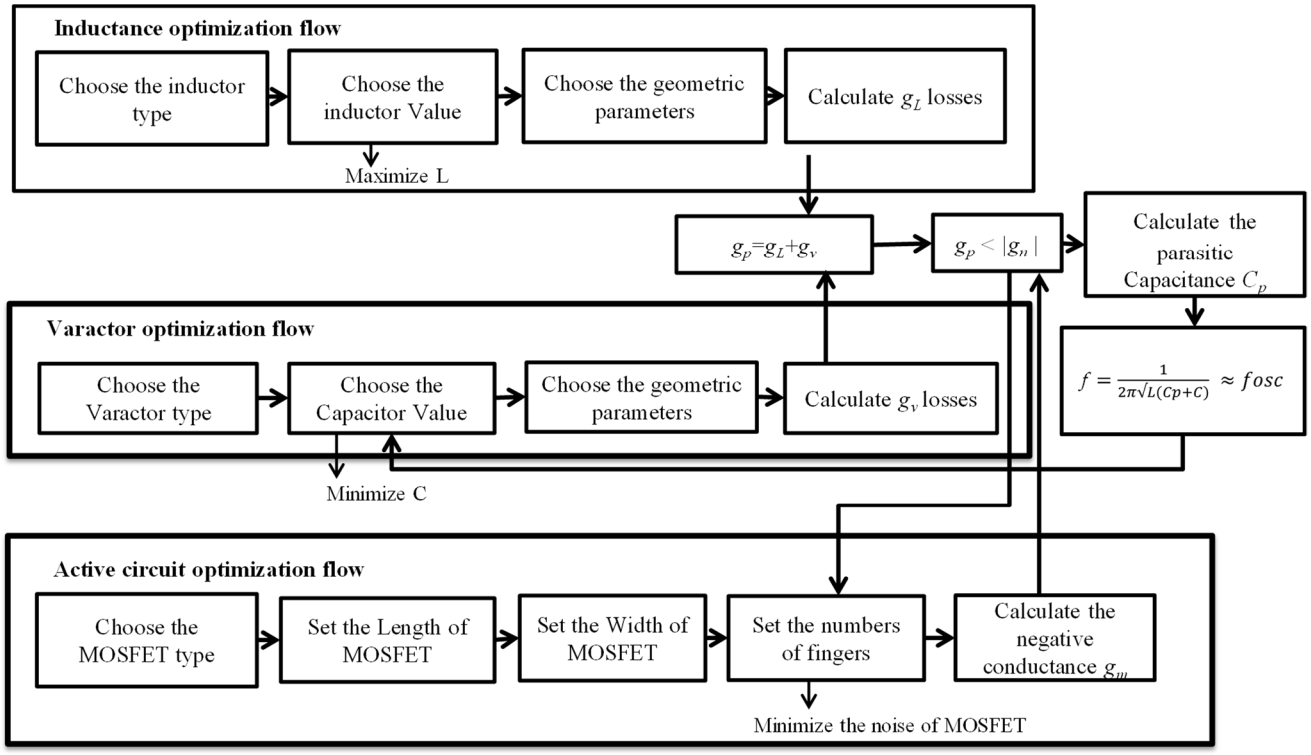

Figure 2. Design flow of ULP LC-VCO.

Inductance optimization:

When considering the design of a ULP VCO, the inductor optimization process requires an abundance of focus. A suitable inductance value and quality factor are used in the design of the tail inductor to ensure optimum performance. The initial phase is to select the type of inductor based on the desired boundaries.

In the proposed design, we selected a high-impedance passive inductor (spiral_std_mu_z) from the tsmcN65 library. In comparison with the other types of inductors, this type of inductor presented a good compromise between quality factor (QL), resistive loss (gL), occupation area, and self-resonant frequency (SRF). The following phases involve selecting the proper inductance size (width and length), as well as geometrical variables such spacing, count of turns, inner radius, and guard ring distance. By choosing a high inductor value with minimal series resistance and maximum quality factor, both power consumption and power factor can be reduced. It is important to note that increasing L's value is limited by its SRF, which should be greater than the oscillation frequency. The inductor track width (W) and the number of turns (N) have been adjusted. The minimum number of turns (Nmin) is needed to reduce the resistive loss (gL). As a result, Nmin must be increased to increase the inductance value. In addition, SRF, QL, and gL are significantly impacted by the inductor's track width. Increasing track width typically enables a reduction in gL followed by an increase in QL. However, it has several downsides, like increased substrate

coupling. The frequency of self-resonance may decrease as a result. For the inductive action to continue, this SRF should be greater than the operational frequency. Therefore, we had used the minimum track width (Wmin) on occasion to boost the SRF.

Varactor optimization:

The phase noise and power dissipation capabilities of the LC resonator are greatly influenced by the varactor's quality factor, making it a crucial component of the device. In order to evaluate the performance of the VCO, the varactor must be optimized. The initial phase of the optimization technique is to select the appropriate varactor type based on the application-specific constraints. In particular, MOS varactors have been proposed as their tuning range is highly constrained. The diode varactor, on the other hand, offers a good compromise between linearity, quality factor (Qv), and effective parallel equivalent conductance, making it desirable for applications with high limits on consumption. In order to attain the wide tuning range for this design, a MOS varactor has been adopted. In order to mitigate PN and power consumption, the value of C should be lowered. The frequency tuning range will, however, be restricted as a result. Subsequently, it is necessary for adjusting the varactor's physical settings. In terms of tuning range and PN, these properties have an impact on the oscillator's performance.

Active circuit optimization:

A key element of the VCO employed to compensate for tank loss is the active circuit. It also reaffirms parasitic components, though, which may manipulate the oscillation frequency and compromise the phase noise of the VCO. The switching speed and power consumption of this circuit can be improved by employing low-leakage transistors with modest channel lengths. In order to provide the lowest transconductance, transistor width is determined next. The performance of the VCO in terms of noise and power consumption is further improved by using the maximum number of fingers (NF), which lowers the gate resistance.

Furthermore, in this article, we used TSMC 65 nm with I poly and 9 metal (1P9M) CMOS technology in a Cadence Virtues CAD environment for the VCO schematic design, simulations, analysis of the simulation results, layout, and post-layout simulation. Optimizing a VCO is a complex and iterative process. In this research, the optimizing process took several iterations to obtain the best results. The following steps have been taken to design and optimize the proposed VCO.

VCO specifications: The leading idea of this article is to produce a design that provides better phase noise, low power consumption, accurate quad oscillation, and a better frequency tuning range with reduced chip size. In this regard, we adopted the best technique of the VCO and frequency divider.

VCO schematic: Using Cadence Virtuoso, create the VCO schematic that meets the specifications of cross-coupled LC VCO. Choose an appropriate MOS sizing as the transistor size is crucial in optimizing the VCO.

Simulate the VCO: Simulate the VCO using Cadence Spectre in TSMC 65 nm. The simulation should include frequency response and phase noise. Completing the proper biasing can ensure stable oscillation and minimize phase noise. Adjust the voltage levels and current source of the VCO to be properly biased.

Analyze the simulation results: Analyze the simulation results to identify areas that require improvement. To reduce the phase noise, use different transistor sizes and adjust the biasing.

Modify the VCO schematic: Based on the analysis of the simulation results, modify the VCO schematic to improve its performance. This may include changing the transistor sizes, adding or removing components, and adjusting the biasing.

Simulate and analyze the modified VCO: Simulate the modified VCO and analyze the simulation results to determine if the performance has been improved. If necessary, repeat steps 5 and 6 until the desired performance is achieved.

Lay out the VCO: Once the VCO schematic has been optimized, lay out the VCO using the Cadence Virtuoso layout editor. Ensure that the layout adheres to the SMC 65 nm with 1P9M CMOS technology rules and guidelines.

Verify the layout: Verify the layout using the Cadence Virtuoso verification tools to ensure that it meets the design rules and guidelines, and is free from any errors.

Simulate the post-layout VCO: Simulate the post-layout VCO using the Cadence Spectre simulation tools to verify its performance.

Analyze the simulation results and perform optimization: Analyze the simulation results of the post-layout VCO and perform any necessary optimization to further improve its performance.

All these steps were carried out to produce the best results. This article's results show that we achieved lower phase noise, ultra-low power consumption, and better quad oscillation with the reduced chip area as compared to other related work.

Overall, this design methodology emphasizes the importance of optimizing each component of the VCO to meet the required performance parameters. By following this methodology and optimizing the inductor, varactor, and active circuit, it is possible to enhance the VCO's phase noise and power consumption efficiency. Furthermore, the article proposes an optimized approach for addressing the trade-off between phase noise and power consumption in VCO design by using a high-quality factor inductor at the tail to minimize phase noise. This modification improves the performance of the VCO and makes it suitable for use in low-power wireless applications. A high-impedance passive inductor (spiral_std_mu_z) is used from the tsmcN65 library at the tail for filtering, which preserves voltage headroom and ignores frequency modulation. The tail inductor provides additional negative feedback to improve the oscillator's phase noise performance as well. The induction of the tail inductor instead of the conventional MOSFET current source results in a reduction in the tail noise current and an increase in the effective quality factor of the LC tank, thereby improving the overall performance of the oscillator.

3.3. Frequency Divider Design

An effective frequency divider is an essential component in many electronic circuits and systems, particularly in wireless communication applications. The primary function of a frequency divider is to divide the input frequency by a fixed integer value to generate a lower-frequency output signal. However, an effective frequency divider must not only divide frequencies correctly across the entire band of interest, but also add very little noise to the system.

There are different topologies of frequency dividers. In general, the injection-locked dividers have the simplest structure and the narrowest locking range, which results in the greatest operation frequency. Only for low frequencies do static dividers show a reasonably wide range of operation. Miller dividers, also referred to as regenerative dividers, serve as a common way between the two. Among them, the static dividers for relatively low frequencies would be a better choice for this research perspective as they cater for 2.4 GHz applications. The static divider has some different techniques like the LC tank, Current Mode Logic CML ring, and CML DFF. The D flip-flops 1/2 frequency divider utilized current mode logic (CML) with negative feedback, whereas the LC tank and CML ring frequency dividers employ injection locking. The DFF frequency divider is used by most researchers in VCOs and PLL circuits, as reported in [24–26].

Static frequency dividers have been extensively used in synthesizer design because of their ease of implementation and robustness. MOS current mode logic (CML) is commonly used for D-latch applications in a static frequency divider. CML logic can handle high operation frequencies due to its small voltage swing, which reduces rise and fall times. In addition, the CML logic's inherent differential configuration would reduce switching and supply noise. A power-efficient method for reusing current is the LC VCO followed by a 1/2 frequency divider circuit. When oscillation amplitude is decreased, the voltage

headroom for each MOS is likewise decreased, which results in more phase noise than a separated VCO and divider. This technique produces an accurate quadrature signal.

The proposed VCO is followed by a 1/2 frequency divider with two D-type flip-flop latches for quadrature waveform at the desired frequency, as shown in Figure 3. Two D latches constitute the frequency divider's adopted circuit based on the master–slave formation, i.e., the inverted output of the slave latch (MD2, ML1) connect to the input of the master latch (MD1, ML1), which is also reported in [6,26].

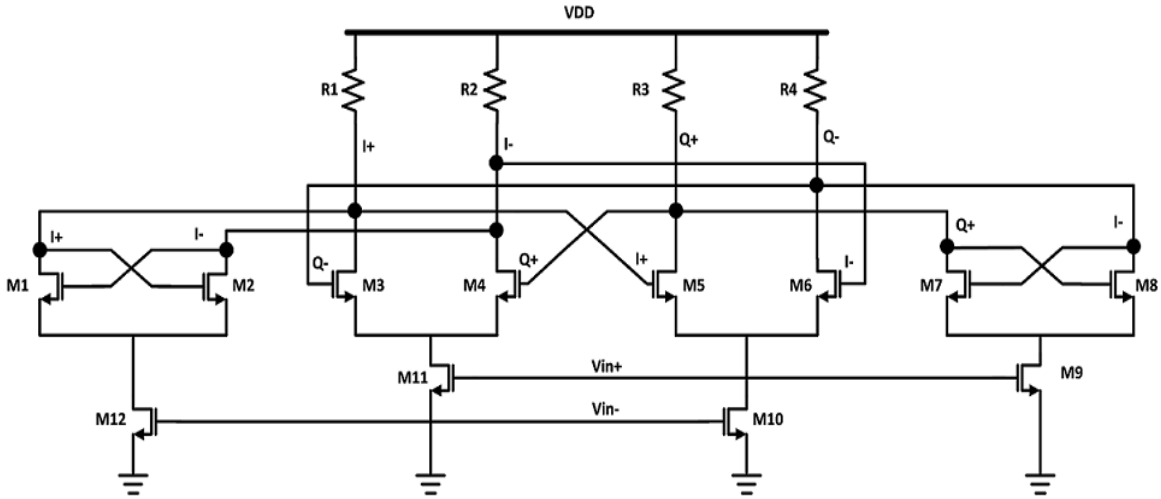

Figure 3. The schematic of the proposed CML D flip-flop 1/2 frequency divider.

The master–slave DFF latch formation is a popular technique for implementing high-speed digital circuits. To create the differential and quadrature phases in the latch formation, the output of the master DFF is delayed by half an input clock cycle, while the output of the slave DFF is delayed by a quarter of an output clock cycle. This delay creates a phase difference between the two outputs, which can be used to drive downstream circuitry. The sizing of the MOS transistors in the divider circuit can have a significant impact on the overall performance of the oscillator, including its frequency stability, phase noise, and power consumption. By optimizing the transistor sizes and other parameters in the divider circuit, it is possible to improve the overall performance of the oscillator and achieve self-oscillation at minimum power dissipation. The W_L/W_D widths ratio has a critical effect on increasing the operating frequency of the divider. The master and slave MOS latches width ratio determines the operating frequency range of the divider. The simulation results show that, with a small W_L/W_D width ratio, the divider is capable of dividing much higher frequencies but with a higher input frequency range such that (4.4–5.8 GHz @ $W_L/W_D = 0.1$) compared to a large W_L/W_D ratio, where the lower input frequency range such that (1.8–2.2 GHz @ $W_L/W_D = 1$), as depicted in Figure 4.

As discussed in [24], a necessary condition of the divider for self-oscillation is

$$gm_L R_{LD} > 1 \tag{2}$$

where gm_L is the transconductance of the latch M_L and R_{LD} is the load resistor of the divider. It is observed that the width of the latch transistor decreases and the transconductance also decreases. To self-oscillate the divider, the load resistance should be increased accordingly, affecting the increase in the output voltage swing. Furthermore, the width of the divider transistor W_D is decreased, causing a further increase in the maximum frequency of the divider. The maximum division frequency and W_L have a monotonic relationship is observed. To ensure that the divider's minimum input division frequency is within the specified frequency range of 2.2 GHz, a low W_L/W_D ratio of 0.6 was selected. This range also gives better amplitude as compared to other W_L/W_D width ratios.

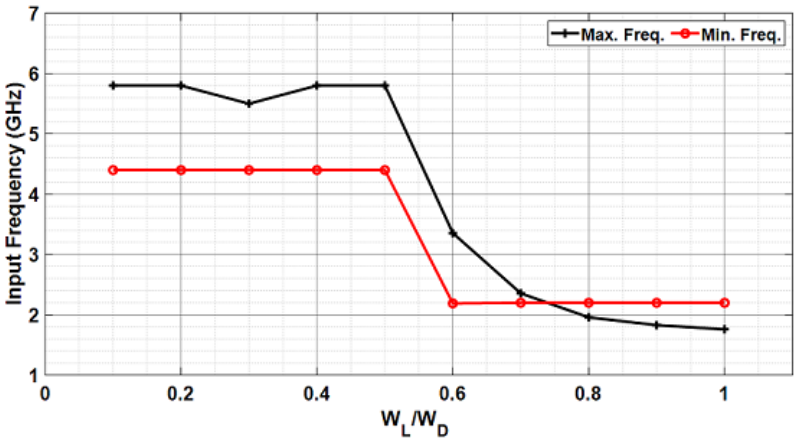

Figure 4. The latch-to-driver width ratio (W_L/W_D) concerning the input frequency range response.

Figure 5 shows the transistor's clock width (W_{CLK}) response concerning the divider's input frequency range. At high frequencies, it is critical to optimize the energy linked to the common source node for a certain externally injected signal. The transistor's clock size and biasing have an important role. For a particular size of the clock transistor, a specific common-mode value produces the maximum self-oscillating frequency [25]. A constant W_L/W_D ratio is used to simulate the response, and it is evident that the divider works at high input frequencies for small-size M_{CLK} transistors such that (4.4–5.8 GHz @ 1 µm). Comparatively, as the M_{CLK} transistor size increased, the input frequency range became narrower such that (1.9–2.2 GHz @ 10 µm).

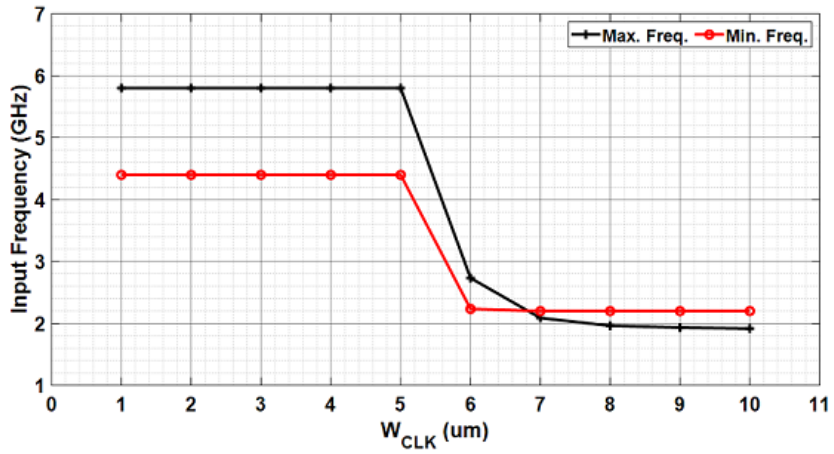

Figure 5. The input frequency ranges as a function of W_{CLK}.

For similar reasons as those cited above for choosing the W_L/W_D ratio, a width of WCLK = 6 µm was chosen for the divider in this work.

4. Post-Layout Simulation Results Using the TSMC 65 nm CMOS Process

This section describes the performance evaluation of the VCO designed with the inclusion of a high-impedance inductor at the tail of two quadrature differential cross-coupled MOSs instead of a conventional MOS current source. The simulation results focus on three performance metrics: phase noise, power consumption, and chip size. Phase noise is an essential parameter in the performance evaluation of a VCO as it determines the amount of jitter or frequency instability in the output signal. Minimizing power consumption is critical in the design of low-power wireless communication systems. By using low-power components, power management techniques, and optimizing the design of individual components, it is possible to extend the battery life of the system. Finally, a

key factor in the design of integrated circuits is the chip size because smaller chips result in lower manufacturing costs and greater integration densities.

The post layout simulations were performed using TSMC 65 nm with 1 poly and 9 metals (1P9M) CMOS technology in a Cadence Virtues CAD environment. Based on the simulation results of the design of the VCO, the performance matrices of the VCO are analyzed. The results are compared with those of a conventional VCO that uses an MOS current source at the tail. The inclusion of the high-impedance inductor is expected to improve the phase noise performance of the VCO while reducing power consumption. Additionally, the design should allow for a smaller chip size.

The proposed work is focused on a quadrature differential cross-coupled CMOS VCO followed by a 1/2 CML DFF frequency divider using a 1.2 V supply voltage which produced low phase noise and consumed low power. The designed VCO using a 2.4 GHz carrier frequency and a 1.2 V supply voltage consumed only 0.47 mW of ultra-low power and has −118.36 dBc/Hz of phase noise at 1 MHz offset with the control voltages (V*cont*) of 1.2 V. The proposed VCO combined with a frequency divider consumed only 2.02 mW power. A small active chip area of 0.19 mm^2 is covered by the proposed VCO with a frequency divider.

Several articles analyzing the performance of the LC VCO have reported a widely acknowledged figure of merit, as indicated below and described in [26]:

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) \quad (3)$$

where L{Δf} is the phase noise measured at a 1 MHz offset frequency, the power consumption (P_{dc}) is measured in mW, and the oscillation frequency is (f_0).

This article establishes a new figure of merit (FoM) expression. The FoM is an important metric in integrated circuit (IC) design that considers multiple factors such as phase noise, power consumption, and chip area. The newly proposed FoM expression includes all these factors and extends Equation (3) which includes the chip area as shown in the below expression.

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) - \mathbf{10log}(\mathbf{chip\ area}) \quad (4)$$

The FoM expression includes a tradeoff between the various factors considered, and the goal is to optimize the FoM value for a given application. By including the chip area in the FoM expression, the new expression allows for a more comprehensive assessment of the IC design, as chip area is an important consideration in IC manufacturing cost and integration density. The new FoM expression provides a valuable tool for IC designers to optimize their designs based on a comprehensive set of performance metrics.

4.1. Phase Noise

This section discusses the phase noise achieved after the simulation. In the presented work, we successfully achieved the required phase noise characteristics at low offset frequencies. The flicker noise is a dominant source of noise at low frequencies, and the VCO design aims to minimize this noise contribution to achieve low phase noise.

As depicted in Figure 6, the phase noise efficiency improved when the control voltages of the VCO were increased from 0 V to 1.2 V.

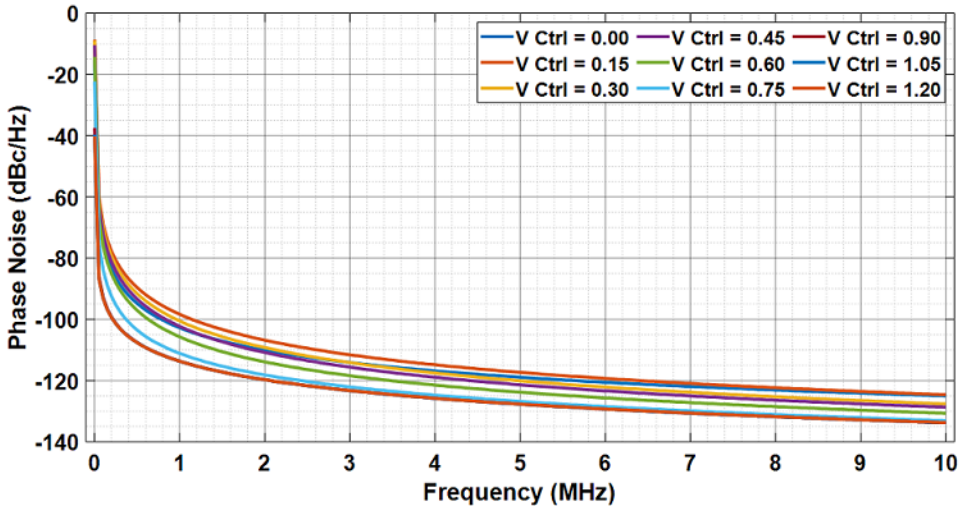

Figure 6. Phase noise v/s frequency at different control voltages.

The lowest phase noise of −118.36 dBc/Hz at 1 MHz offset is achieved at the carrier frequency of 2.4 GHz and a control voltage of 1.2 V, as depicted in Figure 7. The proposed VCO design achieves low phase noise performance by minimizing the effects of flicker noise and optimizing the control voltages. The results show that the VCO design is effective in achieving the required phase noise characteristics, rendering it appropriate for use in a variety of applications, including low IF receivers, wireless sensor networks, and direct conversion receivers.

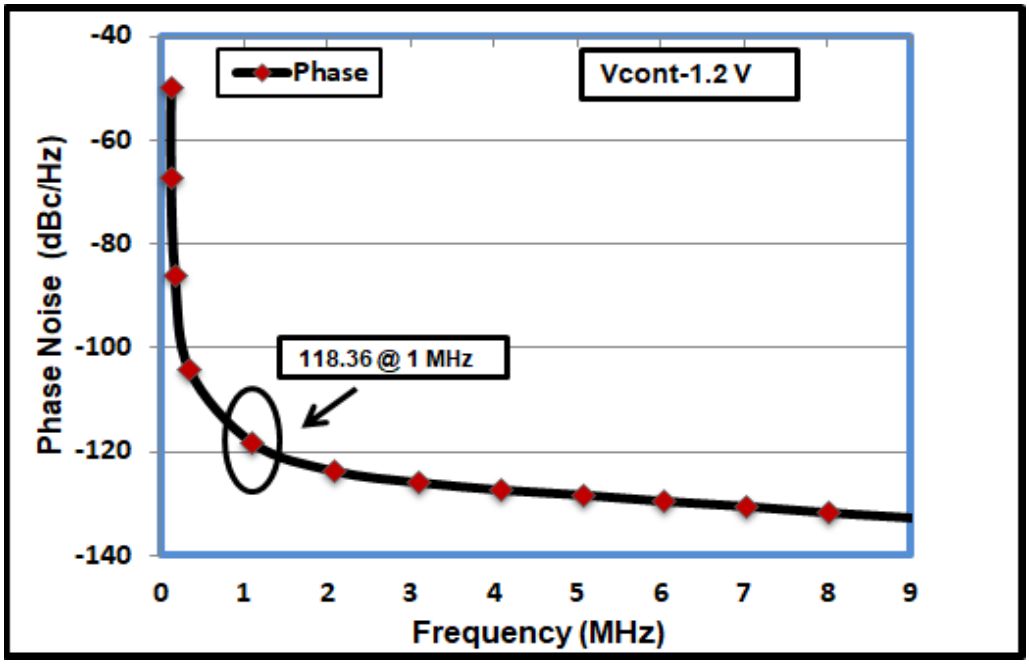

Figure 7. Phase noise −118.36 @ 1 MHz offset frequency.

The quadrature differential cross-coupled VCO and divide-by-two frequency divider's output frequencies may be adjusted between 4.4 GHz and 5.7 GHz, as depicted in Figure 8, where, at minimum control voltages, the frequency is low, i.e., 4.4 GHz, and as the voltages increase, the VCO exhibits a high frequency, i.e., 5.7 GHz. These characteristics of the VCO make it tunable. By changing the variable capacitor's control voltage, the frequency of oscillation may be tuned. The VCO takes around 29 ns to attain a steady amplitude. The time domain output of the designed LC-VCO is present in Figure 9.

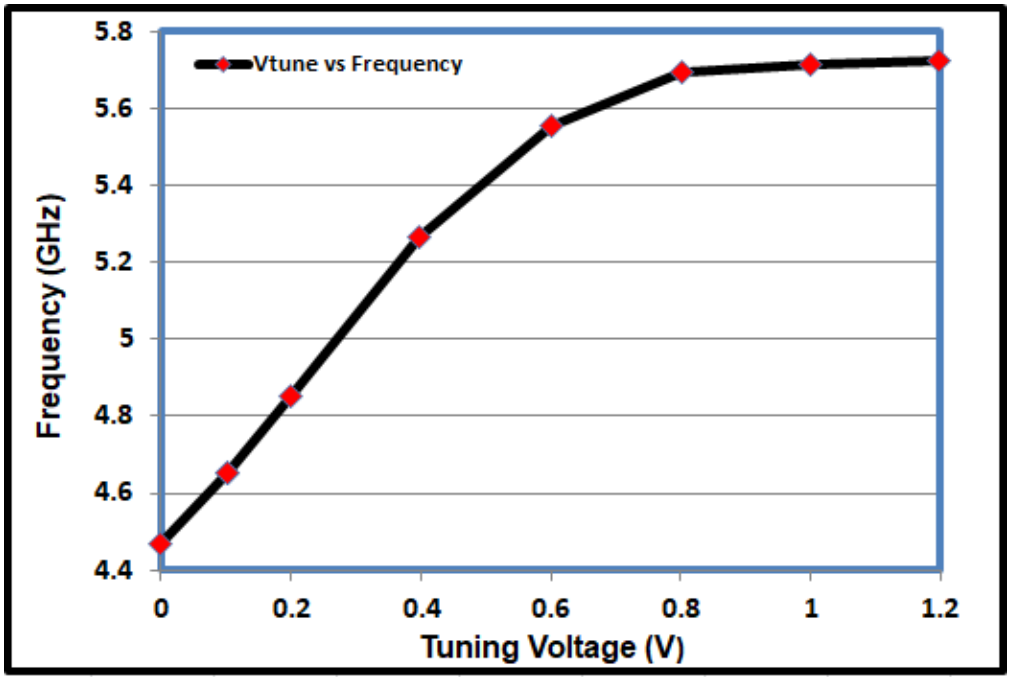

Figure 8. Frequency v/s control voltages.

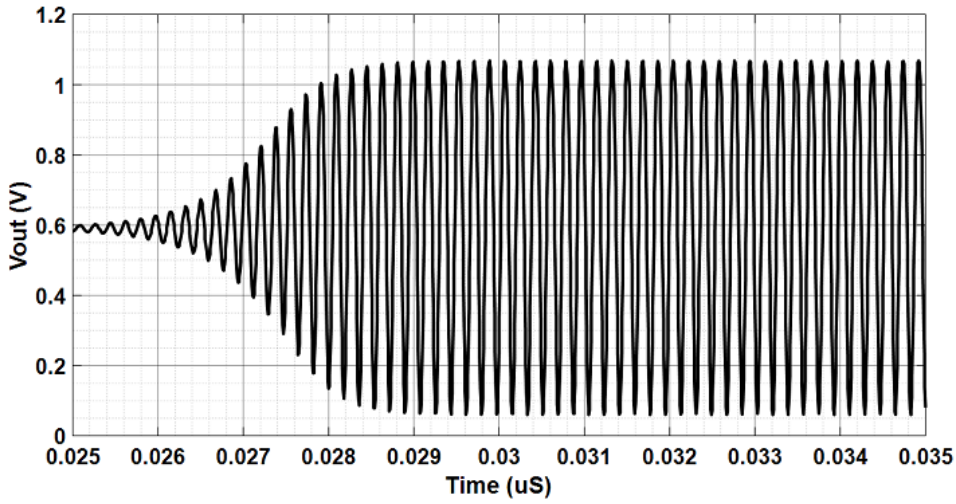

Figure 9. The proposed VCO's time domain output waveform.

In this article, a differential VCO technique has been adopted that consists of an LC tank complementary cross-coupled MOS pair (NMOS and PMOS) operating at double the required LO frequency reuses the bias current of a divide-by-two frequency divider and capacitor varactor for voltage control. The technique provides high phase accuracy and acquires low power and accurate quadrature local oscillator (LO) signal generation. The master–slave flip-flop in series makes it possible to generate two output signals that are 90 degrees out of phase with each other and this constitutes the divide-by-two frequency divider which generates the accurate quadrature LO signals.

The fact that the complementary cross-coupled pair only requires half the current than the cross-coupled structure allows for the more efficient utilization of current resources, leading to lower power consumption. Furthermore, the reduced current requirement in the complementary pair allows for the possibility of increasing the tail current without significant concerns for power consumption. By increasing the tail current, the gain of the VCO can be improved, resulting in better overall performance. The current is reused in

the PMOS and NMOS pair leading to an increase in the transconductance gm. It would double the transconductance *gm* for the same current. The symmetry provided by the complementary topology can help lower phase noise. Phase noise refers to the random fluctuations in the output signal's phase, which can degrade the performance of an oscillator. The balanced structure of the complementary topology can reduce phase noise, which is the unpredictable variation in the phase of the output signal. These fluctuations can negatively impact the oscillator's performance. However, the symmetry of the complementary pair can minimize specific sources of phase noise, resulting in better spectral purity and improved performance.

Furthermore, the most precise quadrature LO signals across a broad frequency range are produced using a double-frequency VCO using a 1/2 frequency divider technique. In this article, a LC tank complementary cross-coupled differential voltage-controlled oscillator (VCO) with master-slave D flip-flops is used to achieve perfect symmetry between the quadrature outputs of an oscillator. This technique addresses the intrinsic asymmetry issue in current reusing and ensures an accurate quadrature phase relationship, leading to improved performance in RF transceivers. To design ZERO-IF receivers, this solution should be preferred because it avoids direct parasitic coupling between the VCO and receiver input. Figure 10 exhibits the quadrature output waveform in the time domain of the proposed VCO with a frequency divider in post-layout simulation.

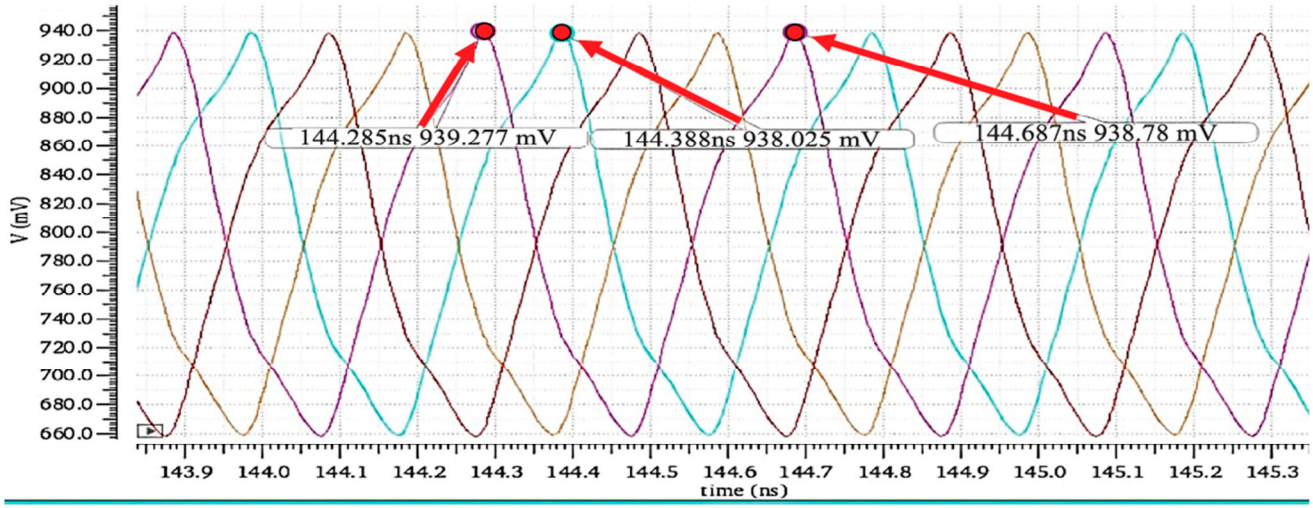

Figure 10. The quadrature time domain output waveform of the proposed VCO with a frequency divider.

The proposed VCO technique naturally provides an output CM level around equal to VDD/2. The technique can be viewed as two back-to-back CMOS inverters or as cross-coupled NMOS and PMOS pairs sharing the same bias current. Instead of using CMOS current source at the tail of the structure, we used a high-impedance passive inductor to save the voltage headroom and reduced the noise factor. To maximize the tuning range, we carefully selected the CMOS dimensions as mentioned in the article.

4.2. Design Layout

The layout area of the presented CMOS VCO and frequency divider architecture in this article occupied a small active area of 0.19 mm^2 of the chip without a pad and 0.47 mm^2 with pads. Figure 11 shows a chip photograph of the proposed LC-VCO. The design presented in this article is simulated with the TSMC 65 nm CMOS technology with 1 poly and 9 metals.

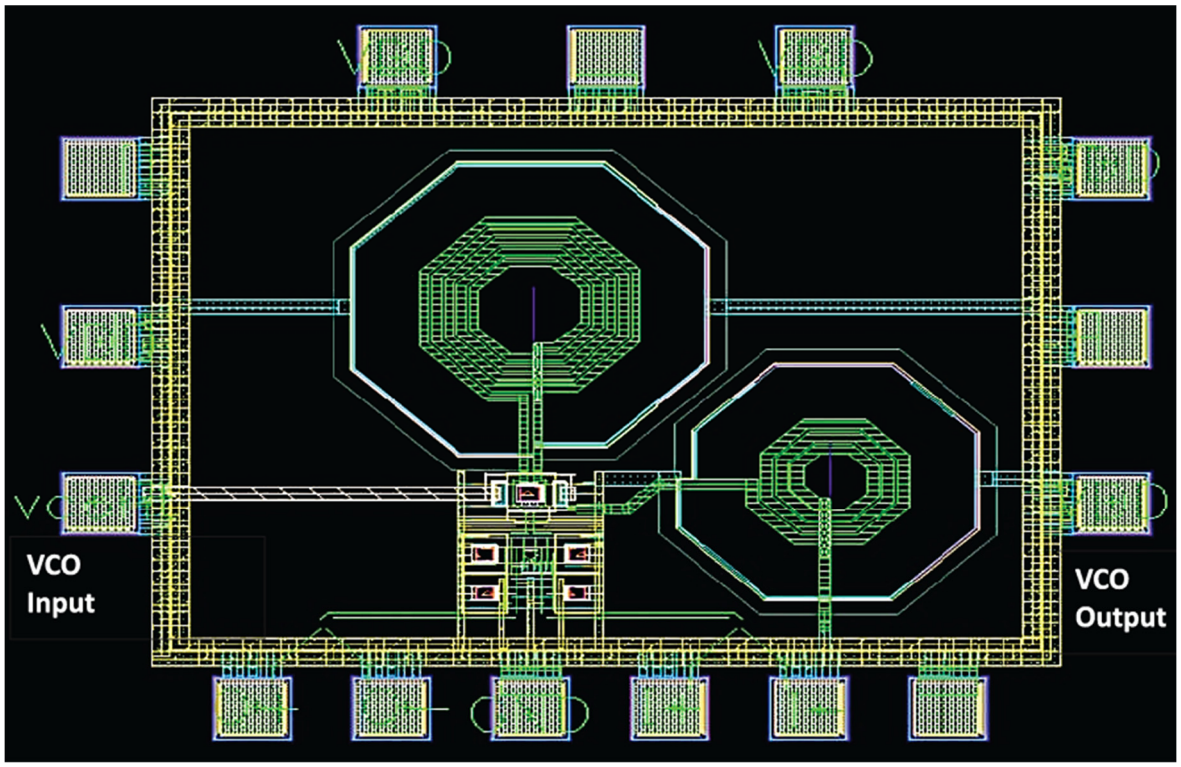

Figure 11. Layout of proposed ULP-VCO using 65 nm CMOS technology.

As highlighted, the simulation results may differ during the manufacturing process. These would be manufacturing deviations, temperature variations, supply voltage variations, or environmental noise sources. These variations would impact design results if not properly simulated considering these factors. To mitigate the impact of manufacturing deviations and environmental influences, designers employ techniques such as process calibration, temperature compensation, voltage regulation, shielding, and isolation to improve the performance and reliability of the complementary structure of cross-coupled VCOs. Furthermore, proper layout techniques, the use of well-matched components, and the careful consideration of environmental factors during the design process can help minimize the effects of these influences.

To mitigate the impact of manufacturing deviations and environmental influences and to maintain the desired performance, we adopted the following:

Layout techniques: Proper layout techniques can minimize the impact of environmental influences. Careful placement of critical components, proper grounding, and separation of sensitive RF circuitry from noise sources reduced the effects of noise and interference.

Simulation and modeling: Advanced simulation tools and accurate models enabled us to predict the impact of environmental influences during the design phase. By simulating the behavior of RF circuits under different environmental conditions, it optimized circuit performance, selected the appropriate compensation techniques, and ensured robustness against environmental variations.

These techniques collectively help mitigate the influence of environmental factors on RF circuits, maintain consistent performance, and ensure reliable operation across different operating conditions and environments.

We used TSMC 65 nm with 1 poly and 9 metals (1P9M) CMOS technology in Cadence Virtues CAD environment for the VCO schematic design, simulations, analysis of the simulation results, layout, and post-layout simulation. To cater to the manufacturing deviations and environmental influences and maintain the desired performance, Cadence has tools to account for real-world effects in the development of a VCO. We adopted multiple steps, and some are as follows:

Circuit Simulation: After the selection of the appropriate components and schematic design, we used Cadence's circuit simulation tool SpectreRF 65 nm to perform various simulations. These simulations help analyze the circuit's behavior under different operating conditions, including manufacturing variations and environmental influences.

Layout Design: Once the circuit behavior was validated through simulations, we went through the layout design phase. We used Virtuoso Layout Suite to create the physical layout of the VCO circuit, considering design rules, parasitic effects, and the manufacturing process.

Design Rule Checking (DRC) and Layout Versus Schematic (LVS) Checks: Before proceeding further, we used Cadence's DRC and LVS tools to ensure that the layout adhered to the design rules and matched the schematic connectivity accurately.

Post-layout Simulation: Once the layout was verified, we performed post-layout simulations to evaluate the circuit's performance under real-world conditions. This step considered parasitic effects, such as parasitic capacitance and inductance, which can significantly affect the VCO's behavior.

Due to some limitations, we would not go for the fabrication of the chip to further prototype testing and validation after. Unfortunately, up until now, this research received no specific grant from any funding agency in the public or commercial sectors. If we found any potential collaborator in near future, we would definitely go for the chip fabrication through TSMC Taiwan.

4.3. Comparison with Previous Work

The proposed LC cross-coupled VCO with a high impedance passive tail inductor followed by a frequency divider in this paper has exhibited better phase noise, less chip area, i.e., 0.19 mm^2, and consumed only 0.47 mW of power. The leading idea of the article is to produce a design that provides better phase noise, low power consumption, accurate quad oscillation, and a better frequency tuning range with reduced chip size. The citations cover a wide range of topics related to oscillator design, including low-phase noise design, low-power operation, frequency dividers, and various techniques for improving VCO performance. There are some recent works but with different CMOS process, techniques, and carrier frequency are cited in [27–31].

To fairly compare of our work with other VCO techniques, we only cater to the frequency range of 2.4 GHz. We have adopted the conventional state-of-the-art FoM equations as well, and compared the VCO results with other similar works. To better understand and elaborate on our results, we compare the results of our proposed VCO with the conventional FoM equation and with the FoM equation including chip size as well, as described in Tables 1 and 2. To compare this work with other related works, we used conventional FoM equations.

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) \tag{5}$$

$$\mathbf{FoM} = \mathbf{L}(\Delta\mathbf{f}) + \mathbf{10log}\left(\frac{\mathbf{P_{dc}}}{[\mathbf{mW}]}\right) - \mathbf{20log}\left(\frac{\mathbf{f_o}}{\mathbf{F_{offset}}}\right) - \mathbf{10log}(\mathbf{chip\ area}) \tag{6}$$

The proposed VCO has produced −196.44 dBc/Hz of FoM. Overall, this research exhibits a better figure of merit than other related works.

Table 1. Performance comparison of LC-VCO with other similar VCO designs.

Simulated/ Measured	FoM (dBc/Hz)	Chip Area (mm^2 (Active))	Power Consumption (mW)	Phase Noise @ 1 MHz (dBc/Hz)	Supply Voltage (V)	Carrier Frequency (GHz)	CMOS Process (nm)	Reference
S	−184.47	0.63	8.22	−125	1.5	2.7	180	[4]
M	−179.7	0.72	4.32	−121.5	1.8	1.58	180	[10]
S	−192.22	0.48	2.4	−130	1.2	2	130	[23]
M	−187	1.44	2.92	−117.4	1	5.13	180	[32]
S	−186.91	0.837	2.04	−122.4	1.2	2.4	130	[11]
S	−189.24	0.19	0.47	−118.36	1.2	2.4	65	This Work

Table 2. Performance comparison of LC-VCO with other similar VCO designs including chip area.

Simulated/ Measured	FoM (dBc/Hz)	Chip Area (mm^2 (Active))	Power Consumption (mW)	Phase Noise @ 1 MHz (dBc/Hz)	Supply Voltage (V)	Carrier Frequency (GHz)	CMOS Process (nm)	Reference
S	−186.47	0.63	8.22	−125	1.5	2.7	180	[4]
M	−177.7	0.72	4.32	−121.5	1.8	1.58	180	[10]
S	−189.04	0.48	2.4	−130	1.2	2	130	[23]
M	−188.53	1.44	2.92	−117.4	1	5.13	180	[32]
S	−187.68	0.837	2.04	−122.4	1.2	2.4	130	[11]
S	−196.44	0.19	0.47	−118.36	1.2	2.4	65	This Work

5. Conclusions

This article presents a tunable quadrature differential cross-coupled CMOS LC-VCO followed by a 1/2 DFF frequency divider for low-power, low-phase IoT/BLE receivers and wireless sensors. An ultra-low-power VCO with a tuning range of 4.4 to 5.8 GHz was designed using TSMC 65-nm CMOS technology. The technique is constructed on two back-to-back quadrature differential cross-coupled inverting CMOSs through a high-impedance on-chip passive inductor at the tail and allows for truly differential operation followed by a $\frac{1}{2}$ DFF frequency divider producing accurate quadrature outputs. In the design, a high-impedance inductor is used at the tail for filtering, and this preserves voltage headroom and ignores frequency modulation.

The designed VCO operates at 2.4 GHz carrier frequency and 1.2 V supply voltage consuming only 0.47 mW of ultra-low power and has −118.36 dBc/Hz of phase noise at 1 MHz offset with the control voltages (V*cont*) of 1.2 V. The proposed VCO combined with a frequency divider consumed only 2.02 mW power. The active area of the chip is 476 × 416 m^2 without pads and 783 × 638 m^2 with pads. A figure of merit (FoM) of −196.44 dBc/Hz was produced by the proposed VCO. In comparison to other related research, this work exhibits a higher figure of merit (FoM).

Future Enhancement:

The fabrication and testing of the simulated ULP VCO design are important steps towards validating the design and demonstrating its potential impact in the field of wireless communication. The use of a well-developed IC design tool library for 65 nm CMOS technology from TSMC made the design process more efficient and cost-effective.

Once the ULP VCO design is fabricated and tested, it can be evaluated for its performance in terms of frequency stability, phase noise, phase error, and power consumption. This will provide valuable data that can be used to further optimize the design and evaluate its suitability for specific applications. The potential applications for IoT/BLE receivers and WSN devices make this design highly impactful in the field of wireless communication. Its successful fabrication and testing can lead to the development of more efficient and

reliable IoT/BLE receivers and WSN devices, which can have a positive impact on various industries, such as healthcare, industrial automation, and smart cities.

Author Contributions: Conceptualization, M.F.S. and M.K.M.; methodology, M.F.S. and M.R.; investigation, M.F.S. and M.R.; supervision, M.K.M. and A.R.M.; writing—original draft, M.F.S. and M.K.M.; review and editing, M.F.S., M.K.M. and A.R.M. All authors have read and agreed to the published version of the manuscript.

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