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A Sub-1-V Nanopower MOS-Only Voltage Reference

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Abstract: A novel low-power MOS-only voltage reference is presented. The Enz–Krummenacher–Vittoz (EKV) model is adopted to provide a new perspective on the operating principle. The normalized charge density, introduced as a new variable, serves as an indicator when trimming the output temperature coefficient. The proposed voltage reference consists of a specific current generator and a 5-bit trimmable load. Thanks to the good match between the current source stage and the output stage, the nonlinear temperature dependence of carrier mobility is automatically canceled out. The circuit is designed using 55 nm COMS technology. The operating temperature ranges from −40 °C to 120 °C. The average temperature coefficient of the output voltage can be reduced to 21.7 ppm/°C by trimming. The power consumption is only 23.2 nW with a supply voltage of 0.8 V. The line sensitivity and the power supply rejection ratio at 100 Hz are 0.011 %/V and −89 dB, respectively.

Keywords: voltage reference; MOS-only; low power; low voltage; sub-threshold

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1. Introduction

The low-power voltage reference is an essential circuit block in power-limited applications, such as the Internet of Things (IoT), portable devices, and biological interfaces [1–5]. As a constant reference quantity for the circuit system, the robustness and insensitivity of its output have crucial impacts on the performance of the system. The voltage reference in such applications aims to keep a stable and constant output in any process, voltage, and temperature (PVT) with minimal power.

Currently, voltage reference sources can be roughly sorted into three categories: bipolar (BJT) references, CMOS references, and hybrid references. The traditional bipolar bandgap references (BGRs) generate an output voltage of about 1.2 V (V_{BG}), which is relatively consistent among different process technologies. Despite that BGR has little process variation, it requires a supply voltage higher than 1 V [6–8]. This is not suitable for most low-power applications and is not available in some advanced technology nodes. Furthermore, the temperature coefficient (TC) of the conventional first-order BGR is relatively large. Meanwhile, high-order compensation technology inevitably makes the circuit topology more complex.

To realize a voltage reference operating with a sub-1 V supply, the latter two references have been developed [9–14]. The CMOS references are generally based on the temperature characteristics of the threshold voltage (V_T). The V_T-based references (VTR) utilize the exponential relationship of MOS transistors biased in the subthreshold region to take the place of BJTs. The output voltage of VTRs is usually equal to the extrapolated value of the threshold voltage, thus allowing the lower supply voltage. Unfortunately, the process variation of its output voltage is larger compared to that of BGR. Some VTRs also need resistors to generate a controllable voltage proportional to the absolute temperature (PTAT) [15–17].

Because the current is limited to very small, it can be seen that the resistor not only costs more mask layers in manufacturing but also occupies more chip area. In addition, some designs associate the different types of transistors [1,18,19], generating an output proportional to the difference of two threshold values ($V_{T1} - V_{T2}$). Although this technique can significantly reduce the supply voltage, it also requires the use of more masks and increases the process variations.

Recently, some works combined the principles of VTR and BGR, creating a hybrid voltage reference [20–22]. The hybrid reference generates a nominal value of $V_{BG} - V_T$ with process dependence compensated by a dimension-induced side-effect. However, reducing the minimum supply voltage of the hybrid reference is challenging because of the fixed voltage drop between the base and emitter.

Based on the analyses above, we present a new VTR that only consists of one type of MOS transistor. A novel current source is proposed and discussed by a new approach. A simple trimming method is also adopted to further reduce the TC. The paper is organized as follows. Section 2 reviews the basic EKV model, and introduces it into the explanation of the principle of V_T-based voltage reference. Section 3 presents the design of the proposed circuit and shows the detailed design considerations of each part. Section 4 gives the simulated results and the comparison with other works that have been reported in recent years. Section 5 concludes the paper.

2. Principle of MOS-Only Voltage Reference

2.1. EKV Model

Before we look into the Enz–Krummenacher–Vittoz (EKV) model, it is admirable to revisit the conventional square-law model, which is widely adopted in textbooks. For saturation region and triode region, the drain current equation I_D of the square-law model can be expressed as follows:

$$I_{\mathrm{D}} = \mu C_{\mathrm{ox}} \frac{W}{L} \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{1}{2} V_{\mathrm{DS}}^2 \right], \tag{1}$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance of unit area, W is the width of the MOS transistor, L is the length of the MOS transistor, and V_{GS} and V_{DS} are, respectively, the gate and drain voltage referred to the source terminal. It is important to note that, to distinguish it from V_T, V_{TH} is the threshold voltage with respect to the source. It can be seen from Equation (1) that the thermal voltage U_T is not taken into account, which leads to the poor coherence between the equation and simulation in temperature-dependent performance. As a circuit module that is highly concerned with temperature characteristics, when designing and analyzing the voltage reference, the model should include a comprehensive representation of temperature characteristics. Thus, we introduce the Enz–Krummenacher–Vittoz (EKV) model to explain and optimize the proposed voltage reference circuit.

The EKV model is a charge-based compact model proposed by Enz, Krummenacher, and Vittoz in Switzerland in 1995 [23]. The starting point of this model was to establish a single equation that could adapt to all inversion regions [24–27]. The drain current I_D of the EKV model is expressed through the normalized drain current i [28,29]:

$$i = \frac{I_D}{I_S}, \tag{2}$$

where I_S is the specific current, defined as

$$I_S = 2n{U_T}^2 \mu C_{ox} \frac{W}{L} = 2n{U_T}^2 \mu C_{ox} K. \tag{3}$$

Here, n is the subthreshold slope factor of the MOS transistor, which varies between 1.3 and 2, depending on the process technology. K is called the aspect ratio. It can be seen that

the temperature dependence of I_S depends on the carrier mobility and thermal voltage. The temperature dependence of the mobility can be expressed as $\mu = \mu(T_R) \cdot (T/T_R)^{-m}$, where the range of m is 1.5 to 2 [30]. Hence, the specific current is a nonlinear increasing function of temperature, approximately proportional to T^{2-m}.

The basic EKV model introduces a new variable q_x, called normalized mobile charge density, to value the amount of charge density at the location x along the channel. The normalized mobile charge density can be calculated from the nonequilibrium voltage V_x along the channel as follows:

$$V_P - V_x = U_T[2(q_x - 1) + \ln(q_x)], \tag{4}$$

$$V_P = \frac{V_G - V_T}{n}, \tag{5}$$

where V_T and V_G are the bulk-referenced threshold voltage and gate voltage, respectively, and V_P is defined as the pinch-off voltage. Equation (4) represents the relationship between the V_x and q_x at the location x. We can replace the subscript of x with S or D to obtain the charge density at the source or drain terminal. When we obtain the q_S and q_D based on the source and drain voltage, the normalized drain current of the transistor i can be derived as follows:

$$i = (q_S^2 + q_S) - (q_D^2 + q_D). \tag{6}$$

On the right side of Equation (6), the square term q^2 represents drift current, which is proportional to the surface potential strength. The linear term q represents diffusion current, which is proportional to the mobile charge density gradient. The part inside the first bracket is called forward current, and the part inside the second bracket is called reverse current. Equation (6) is applicable to both saturated and nonsaturated transistors. However, for saturated transistors, where the V_D is greater than the pinch-off voltage V_P, the current contributed by the second bracket can be neglected.

Above are the basic equations of the EKV model. For the origin of Equations (4)–(6), we provide a detailed derivation in Appendix A. It is admirable that the EKV model provides predictions of MOSFET behavior across all operating regions, including weak inversion, moderate inversion, and strong inversion. In addition, q not only represents the normalized charge density but also can serve as an index of channel inversion level. When $q \ll 1$, that is, $q > q^2$, the diffusion current is dominant. At this point, the channel is in weak inversion (WI). Similarly, when $q \gg 1$, the channel is in strong inversion (SI). When $q = 1$, the drift current is equal to the diffusion current, and the channel is in moderate inversion (MI).

2.2. MOS-Only Voltage Reference Operation Principle

The basic principle of V_T-based voltage reference is to bias a diode-connected MOSFET with a definite current that varies with temperature. The conceptual diagram is shown in Figure 1a, and the following text details the analysis of how to determine the magnitude and the temperature dependence of this current.

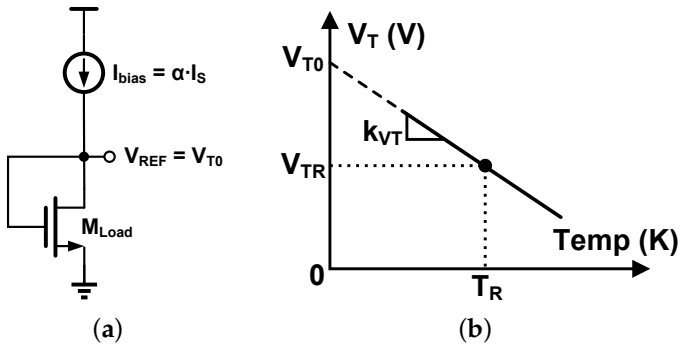

Figure 1. (**a**) The conceptual diagram of V_T-based voltage reference; (**b**) the temperature characteristic of V_T.

As shown in Figure 1b, the threshold voltage V_T is complementary to the absolute temperature (CTAT) with good linearity. Thus its temperature dependence can be represented by a linear function:

$$V_T = V_{T0} - k_{VT}T, \tag{7}$$

where k_{VT} is the temperature coefficient (positive value), and V_{T0} is the intersection when the line is extrapolated to absolute zero temperature.

According to Equations (4) and (5), the gate voltage for a source-grounded MOSFET can be expressed as follows:

$$V_G = nU_T[2(q_S - 1) + \ln(q_S)] + V_T. \tag{8}$$

The first term of Equation (8) is PTAT, and the second term is CTAT. In other words, to make the gate voltage a temperature-independent quantity V_{REF}, the temperature coefficients of the two terms must complement each other.

$$\frac{nk_b}{e_0}[2(q_S - 1) + \ln(q_S)] = k_{VT}, \tag{9}$$

where k_b is the Boltzmann constant, e_0 is the elementary charge. Unfortunately, Equation (9) does not have an analytical solution, but we can use the function $\omega(x)$ to represent the solution of the equation $y + \ln(y) = x$. $\omega(x)$ can be found in the Symbolic Math Toolbox of MATLAB R2018a or newer versions as a mathematical function *wrightOmega*. Therefore, q_S can be expressed as follows:

$$q_S = \frac{1}{2}\omega\left(\frac{k_{VT}}{k_b/e_0} + 2 + \ln 2\right). \tag{10}$$

Assuming the transistor is saturated, we eliminate the reverse current by combining Equations (2), (6) and (10), and it can be determined that the required bias current I_{bias} is

$$I_{bias} = I_S \cdot \frac{1}{4}\omega^2\left(\frac{k_{VT}}{k_b/e_0} + 2 + \ln 2\right) = \alpha I_S, \tag{11}$$

where α is a positive dimensionless constant. As shown in Equation (11), the quantity in the parentheses is temperature-independent, i.e., α is temperature-independent. Therefore, the temperature characteristic of the required bias current is consistent with the temperature characteristic of I_S. At this bias current, the gate voltage of the diode-connected transistor M_{Load} is equal to V_{T0}. It should be noted that the drain voltage of M_{Load} is also V_{T0}; thus, the assumption of saturation holds.

Through the analysis above, we can see that the key of V_T-based voltage reference is to generate a current exactly proportional to the specific current I_S of the load transistor. It is worth noting that when q_S deviates from our expected value, the right side of Equation (8) introduces a temperature-dependent term. In other words, the target bias current biases the load transistor to a constant inversion level. Interestingly, the temperature characteristic of carrier mobility does not appear in the analysis above. This is because as long as the bias current is proportional to the specific current, the nonlinear temperature dependence of μ is automatically canceled out.

3. Circuit Design

3.1. Proposed Specific Current Source

Just as we concluded in Section 2.2, the key of the V_T-based voltage reference is to design a specific current source. The core circuit of the proposed specific current source is shown in Figure 2. The devices in the circuit determining the current are $M_1 - M_4$. To ensure that the current generated matches the load transistor M_{Load}, the unit size of $M_1 - M_4$ is equal to the size of M_{Load}. In other words, to avoid V_T mismatch caused by inconsistent channel lengths, all NMOS transistors have identical unit sizes to eliminate the

impact of second-order effects. In addition, the bulk terminals of all NMOS are connected to VSS.

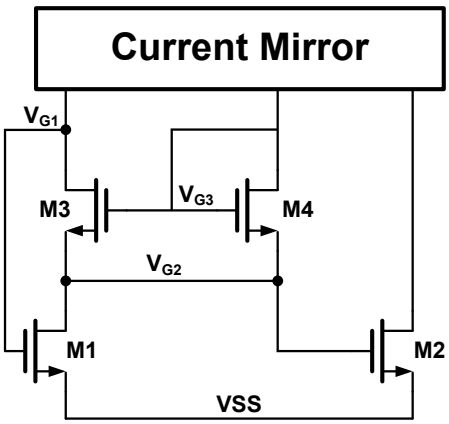

Figure 2. Core circuit of the proposed specific current source.

The current mirror in the upper part of Figure 2 could be replaced by either a simple PMOS current mirror or a cascoded one. For ease of explaining its operating principle, we assume that the current ratios of these three branches are equal. Thus, the drain currents of $M_1 - M_4$ can be expressed as follows:

$$\frac{1}{2} i_1 I_{S1} = i_2 I_{S2} = i_3 I_{S3} = i_4 I_{S4} = I_R. \tag{12}$$

For each transistor, we can use Equations (4) and (6) to sequentially derive out the following relationships:

$$M_1 : \begin{cases} V_{P1} = U_T[-2 + \ln(q_{S1})] = \frac{V_{G1} - V_T}{n} \\ i_1 = q_{S1} = \frac{2I_R}{I_{S1}} \end{cases} ; \tag{13}$$

$$M_2 : \begin{cases} V_{P2} = U_T[-2 + \ln(q_{S2})] = \frac{V_{G2} - V_T}{n} \\ i_2 = q_{S2} = \frac{I_R}{I_{S2}} \end{cases} ; \tag{14}$$

$$M_3 : \begin{cases} V_{P3} - V_{G2} = U_T[2(q_{S3} - 1)] \\ V_{P3} - V_{G1} = U_T[2(q_{D3} - 1)] \\ i_3 = q_{S3}^2 - q_{D3}^2 = \frac{I_R}{I_{S3}} \end{cases} ; \tag{15}$$

$$M_4 : \begin{cases} V_{P4} - V_{G2} = U_T[2(q_{S4} - 1)] \\ i_4 = q_{S4}^2 = \frac{I_R}{I_{S4}} \end{cases} . \tag{16}$$

The equations listed above were simplified based on the proper assumptions as follows: (i) The sizes of M_1 and M_2 are set large enough, thus, the $q_{1,2} = I_{D1,2}/I_{S1,2} \ll 1$. (ii) The sizes of M_3 and M_4 are set small enough, thus, the $q_{3,4} = I_{D3,4}/I_{S3,4} \gg 1$. Simply speaking, $M_{1,2}$ are in weak inversion level, and $M_{3,4}$ are in strong inversion level. If we set the sizes of the M_1 and M_2 to be similar, the difference between V_{G1} and V_{G2} can be controlled at a lower level. In other words, M_3 is in the deep triode region, while $M_{1,2,4}$ is in saturation. In Equations (13), (14) and (16), therefore, we neglected the contribution of $q_{D1,2,4}$ to the normalized drain current.

By combining Equations (13) and (14), we have the following:

$$V_{G1} - V_{G2} = nU_T \ln(\frac{2I_{S2}}{I_{S1}}). \tag{17}$$

Since V_{P3} is equal to V_{P4}, we can easily determine that q_{S3} and q_{S4} are equal. When we take the difference of the first two rows of Equation (15), we can obtain another relationship of V_{G1} and V_{G2}:

$$V_{G1} - V_{G2} = 2U_T(q_{S3} - q_{D3}). \tag{18}$$

The third row of Equation (15) can also be written as follows:

$$q_{S3}{}^2 - q_{D3}{}^2 = \frac{I_R}{I_{S3}} = \frac{q_{S4}^2 \cdot I_{S4}}{I_{S3}} = \frac{q_{S3}^2 \cdot I_{S4}}{I_{S3}}. \tag{19}$$

By substituting Equation (17) into Equation (18), we will have a quadratic equation of q_{S3}:

$$q_{S3}^2 - (q_{S3} - c_1)^2 = q_{S3}^2 \cdot c_2, \tag{20}$$

where $c_1 = \frac{1}{2} n \ln(2I_{S2}/I_{S1})$, and $c_2 = I_{S4}/I_{S3}$. Finally, we can obtain the solution of Equation (20), and the produced current can be expressed as follows:

$$q_{S3} = \frac{c_1}{c_2}(1 + \sqrt{1 - c_2}) = q_{S4}, \tag{21}$$

$$I_R = q_{S4}^2 \cdot I_{S4} = \frac{c_1^2}{c_2^2}(1 + \sqrt{1 - c_2})^2 \cdot I_{S4}. \tag{22}$$

The other root of Equation (20) is discarded, as it does not comply with the assumption made before, that $q_{S3,D3} \gg 1$. If we substitute c_1 and c_2 with the aspect ratios of $M_1 - M_4$, Equation (22) can be rewritten as follows:

$$I_R = \frac{1}{2}\mu U_T^2 C_{ox} n^3 \ln^2\left(\frac{2K_2}{K_1}\right) \cdot \frac{K_3^2}{K_4}\left(1 + \sqrt{1 - \frac{K_4}{K_3}}\right)^2. \tag{23}$$

Therefore, the current of each branch is proportional to the specific current. The temperature characteristic of I_R also follows the characteristic of the unit transistor.

The complete schematic of the proposed voltage reference is given in Figure 3. As annotated in the figure, the overall circuit is composed of four parts: a specific current source, an operational transconductance amplifier (OTA), a start-up circuit, and a trimmable output stage. A cascode transistor M_5 is added to mitigate the difference in drain voltage between M_1 and M_2. The OTA is used to decrease the voltage difference of V_{D7} and V_{D8}, thus, improving the accuracy of the current mirror and reducing the line sensitivity. The role of the start-up circuit is to help the circuit to reach the desired stable state after power-up. Finally, the output stage copies the I_R and generates the reference voltage V_{REF}. In the following subsection, we will give detailed explanations of the operating principles of the remaining part.

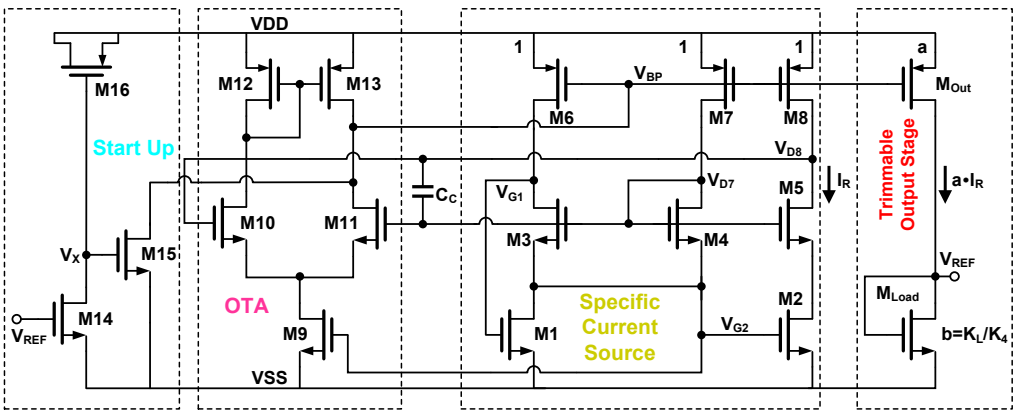

Figure 3. Schematic of the proposed V_T-based voltage reference source.

3.2. Loop Stability

While the amplifier enhances the loop gain, at the same time, the stability of the loop needs to be carefully analyzed. Thus, to prevent the parasitic oscillation of the circuit, a compensation capacitor C_C is added.

The proposed specific current source contains three branches, and both positive feedback and negative feedback exist in the loop. Thus, the expression of the total loop gain is quite complex. Based on reasonable simplifications and comparison with simulation, the frequency response of the loop gain can be expressed as follows:

$$LG(s) = \frac{K(s - w_z)}{(s - w_{p1})(s - w_{p2})(s - w_{p3})}, \tag{24}$$

where

$$\begin{array}{ll} w_z & = -\frac{g_{m1}}{C_{gs2}}; \\ w_{p1} & = w_{ota} = -\frac{g_{ota}}{C_{ota}}; \\ w_{p2} & = -\frac{g_{dsp}}{C_c\left(1+\frac{g_{m2}}{g_{m1}}+\frac{g_{m2}g_{m3}}{g_{m4}g_{ds3}}\right)}; \\ w_{p3} & = -\frac{g_{m2}}{C_{gs2}} \cdot (1 + \frac{g_{m1}}{g_{m2}} + \frac{g_{m1}}{g_{ds3}}); \\ LG(0) & = -\frac{g_{mp}}{g_{dsp}} \cdot \frac{g_{m2}}{g_{ds3}} \cdot (1 - \frac{g_{m3}}{g_{m_4}}) \cdot \frac{g_{mota}}{g_{ota}}. \end{array} \tag{25}$$

$LG(0)$ is the DC gain of the loop. g_{ota} and C_{ota} denote the conductance and capacitance at the output node of the amplifier. The loop gain contains one negative zero and three negative poles. w_{p1} and w_{p2} are much smaller than w_{p3}, contributing a phase shift of $-180°$. Given that the current in M_1 is twice that of M_2, g_{m1}/g_{m2} is approximately equal to 2. Hence, w_{p3} is larger than the zero w_z, causing the phase to increase by 90° and then decrease by 90°. The distribution of the loop's poles and zero is shown in Figure 4. As the compensating capacitance C_C increases, w_{p2} moves towards the origin. By carefully locating two poles, w_{p1-2}, it is possible to retain enough phase margin. The detailed stability results will be presented in the section on simulation results.

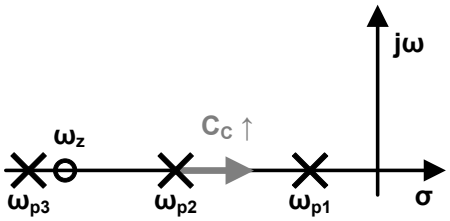

Figure 4. Pole-zero plot of loop gain and the effect of compensating capacitor.

3.3. Output Stage

After generating the required current I_R, we can copy it into the load transistor with a certain proportion and obtain a reference voltage approximately equal to V_{T0}. Due to the variation of V_T and its temperature coefficient during the actual manufacturing, it is necessary to perform trimming in the output branch. As follows, two methods of trimming will be presented: (i) trimming the multiplier of M_{Load}; (ii) trimming the copy ratio of the current mirror.

If we suppose the copy ratio of the PMOS current mirror is $1 : a$, and the aspect ratio of the load transistor is K_L, then

$$q_{SL} = \sqrt{\frac{aK_4}{K_L}} \cdot q_{s4} = \frac{c_1}{c_2}(1 + \sqrt{1 - c_2}) \cdot \sqrt{\frac{a}{b}}, \tag{26}$$

where $b = K_L/K_4$. According to Equation (10), the trimming range determined by the variables a and b must cover the variations in k_{VT} caused by the process corner. The effects of a and b on the normalized charge density of M_{Load} are shown in Figure 5. If we increase the output stage current, i.e., a, the normalized charge density of the load q_{SL} will rise.

When it reaches the value calculated from Equation (10), the temperature coefficient of the V_{REF} approximates zero. Similarly, adjusting the size of the load transistor, i.e., b, can achieve the same goal.

The dashed line represents the target charge density, where the temperature coefficient should be zero. $q^*_{SL}(k_{VT,max})$ corresponds to the case of a relatively large k_{VT}, and, similarly, the $q^*_{SL}(k_{VT,min})$ does, too. Hence, the intersection points of two dashed lines and $q_{SL}(a)$, or $q_{SL}(b)$, indicate the minimum trimming range.

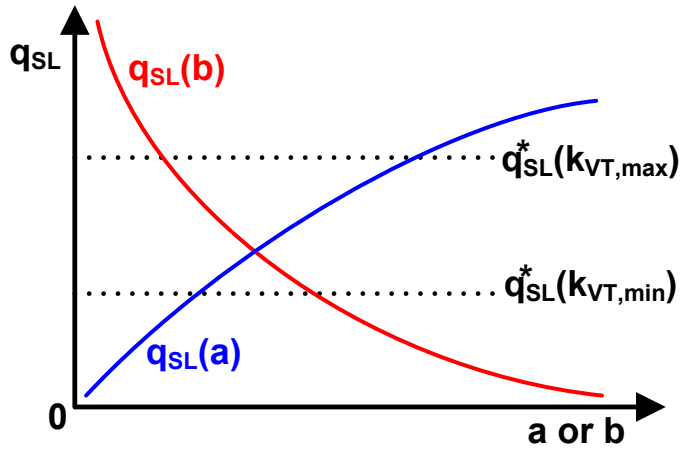

Figure 5. The impact of a (current mirror copy ratio) and b (size ratio K_L/K_4) on the normalized charge density of M_{Load}.

3.4. Start-Up Circuit

When the power supply voltage is applied, all branches in the voltage reference may remain zero. Thus, a start-up circuit formed by $M_{14} - M_{16}$ is adopted to assist the circuit escape from the zero-current state [31].

In the initial start-up stage, due to V_{REF} being zero, M_{14} is turned off. Therefore, the ramp-up of VDD is coupled to node V_{ST} through the MOS capacitor M_{16}. Once the voltage of V_{ST} exceeds the threshold voltage of M_{15}, the node V_{BP} will be pulled down, hence the branch current rising. Meanwhile, V_{REF} will also rise until it reaches the final steady state. When V_{REF} becomes the desired value, approximately V_{T0}, M_{14} is turned on, discharging the node V_{ST} to ground. Finally, M_{15} is turned off, disconnecting the start-up circuit from the core circuit.

4. Simulation Results

In the early stage of circuit design, we use the EKV model to investigate the behavior of the circuit and roughly determine the size of the transistor. The parameters of the EKV model can be extracted through simulation using a MATLAB script which is available on the website provided in [29]. To ensure the simulation accuracy, the final results are still obtained through the Spectre simulator with the BSIM4 model. Table 1 gives the sizes of each transistor in Figure 3.

Table 1. Sizes of the transistors in Figure 3.

Transistor	Size	Transistor	Size
M_u	0.12/20 (µm/µm)	$M_{10,11}$	$4M_u$
M_1	$64M_u$	$M_{12,13}$	5/20 (µm/µm)
M_2	$52M_u$	M_{14}	$2M_u$
M_3	$3M_u$	M_{15}	$2M_u$
$M_{4,5}$	$1M_u$	M_{16}	5/20 (µm/µm)
M_{6-8}	5/20 (µm/µm)	M_{Out}	3×5/20 (µm/µm)
M_9	$104M_u$	M_{Load}	$(\frac{1}{4} \sim \frac{47}{64})M_u$

4.1. Temperature Dependence before Trimming

As explained in Section 3.3, we can trim the temperature coefficient by adjusting the size of the load transistor or the current mirror ratio. It is preferred to take the method of trimming load, thus the consumption of the circuit can be constant. The total current consumption of the proposed voltage reference is proportional to the specific current of the unit NMOS transistor. According to Equation (3), the power of the circuit is approximately a PTAT quantity. At room temperature, the generated specific current I_R is 3.6 nA. As we set the output current ratio a equal to 3, the total current is approximately 8 times that of I_R, i.e., 29.0 nA. Across the entire temperature range, the total current increases from 19.3 nA at -40 °C to 41.2 nA at 120 °C.

In order to determine the trimming range of the circuit, it is necessary to evaluate the temperature dependence before trimming. A Monte Carlo simulation of 500 samples is performed, sweeping the temperature from -40 °C to 120 °C. Both mismatch and corner variation are included in the model to ensure the performance after layout. To avoid making the figure too cluttered, only 100 V_{REF} curves are shown in Figure 6. Thanks to the fact that the specific current of M_{Load} is well matched to the current generated, curves before trimming are relatively flat. The average value of V_{REF} varies from 421 mV to 522 mV. Figure 7 shows the TC histogram of 500 samples. The mean of TC is about 41.8 ppm/°C, and the standard deviation is about 37.0 ppm/°C. The statistical distribution indicates that the temperature coefficient of the vast majority of samples is less than 100 ppm/°C, which can be easily reduced through trimming.

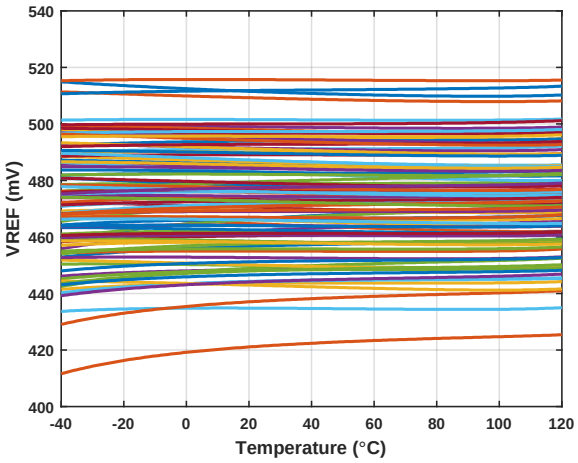

Figure 6. Monte Carlo simulation results before trimming: temperature dependence of V_{REF}.

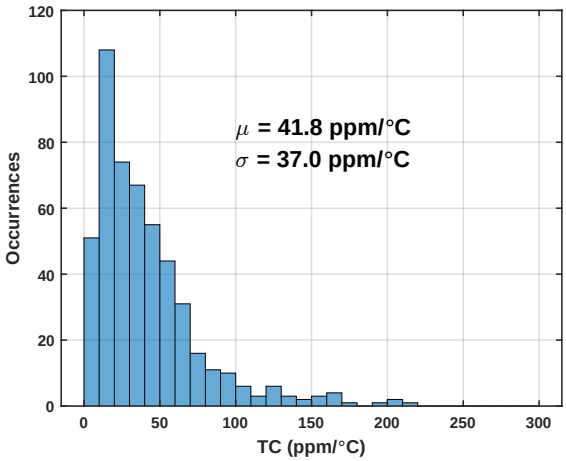

Figure 7. Monte Carlo simulation results before trimming: histogram of temperature coefficient.

4.2. Temperature Dependence after Trimming

The process variation range of V_{T0} is relatively wide, as Figure 6 confirms. Therefore, we cannot use the one-point trimming methodology as BJT-based voltage reference does. The trimming method we adopted can be described as follows: (1) Sweep the trim bits at one ambient temperature, e.g., 20 °C, to obtain the voltage of V_{REF}. (2) Sweep the trim bits at another ambient temperature, e.g., 60 °C, to obtain another set of output values. (3) Take the absolute difference between two sets of data. The trim bits corresponding to the minimum difference are the final bits we need.

A single NMOS switch is used to connect or disconnect the variable load transistors to the output. The size of the variable load follows a binary order, specifically, 1, 1/2, 1/4, 1/16, and 1/32, with respect to the size of M_{Load}. Similarly, we performed a Monte Carlo simulation of 500 samples with the above trimming procedure. Figure 8 presents the trimmed output voltage after subtracting its mean value. The curves intersect at the two temperature points where we performed the trimming. The histogram in Figure 9 shows that the mean of TC is reduced to 21.7 ppm/°C and the standard deviation to 10.6 ppm/°C. A total of 84.2 percent of the samples have a temperature coefficient below 30 ppm/°C, and 95.4 percent of the samples have a temperature coefficient below 40 ppm/°C.

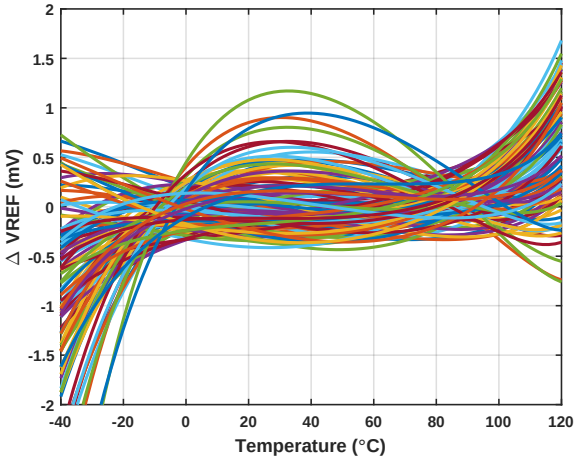

Figure 8. Monte Carlo simulation results after trimming: temperature dependence of ΔV_{REF}.

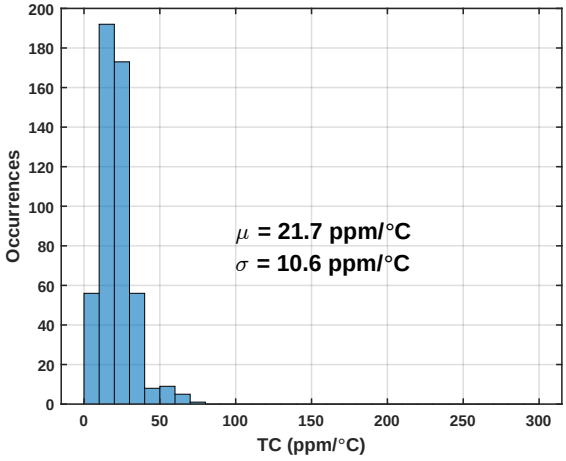

Figure 9. Monte Carlo simulation results after trimming: histogram of temperature coefficient.

After calibration, the distribution of average output voltage and the final determined trimming bits are shown in Figures 10 and 11. The mean value of the V_{REF} is 474.4 mV, roughly similar to the output under the typical process corner. As we adopted the global Monte Carlo model during simulation, the variation coefficient σ/μ is 5.8%, which is larger compared to the coefficient of BGR. V_{REF} is relatively higher under the fast corner and

lower under the slow corner; therefore, the proposed voltage reference can also serve as an indicator of the NMOS corner. Figure 11 implies that the selection of a 5-bit trimming range can meet the needs of the vast majority of samples. The bits number varies from 9 to 23, and its mean value is around the half of 2^5.

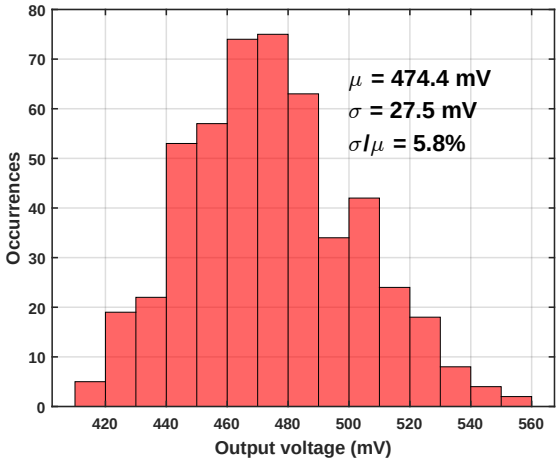

Figure 10. Histogram of average output voltage after trimming.

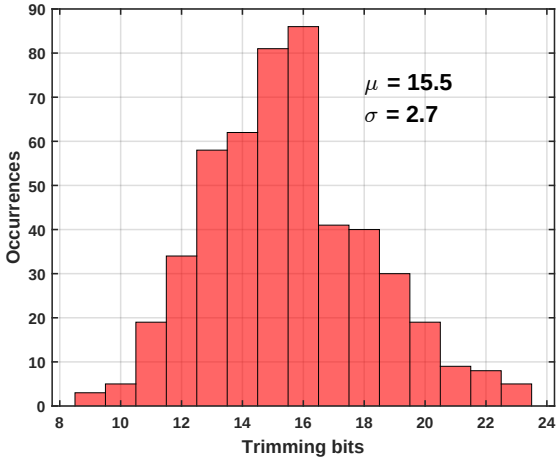

Figure 11. Histogram of determined trimming bits number.

4.3. Frequency Compensation

Figure 12 illustrates the frequency response of the loop gain with or without C_C. The red circles in the figure denote the unit gain frequency and the corresponding phase margin. As explained in Section 3.2, the increasing of C_C compresses the unity gain bandwidth of the loop. When the unity gain bandwidth decreases, the frequency point corresponding to the phase margin first approaches w_{p3} and then moves closer to w_z. In a figurative sense, the corresponding point will first climb a hill and then descend into a valley. The simulation result of phase margin versus C_C is shown in Figure 13. The capacitance value of the C_C is finally determined to be 400 fF, while the phase margin of the loop is 38.7°.

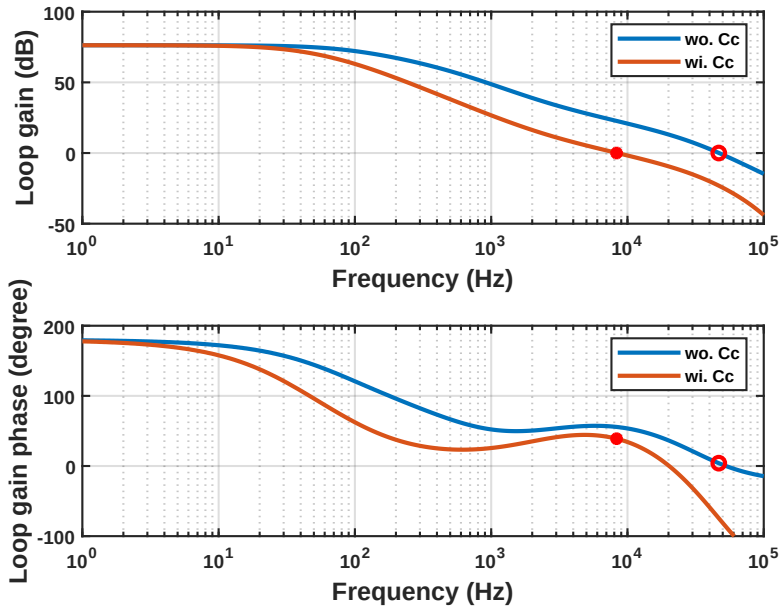

Figure 12. Frequency response of loop gain without or with C_C.

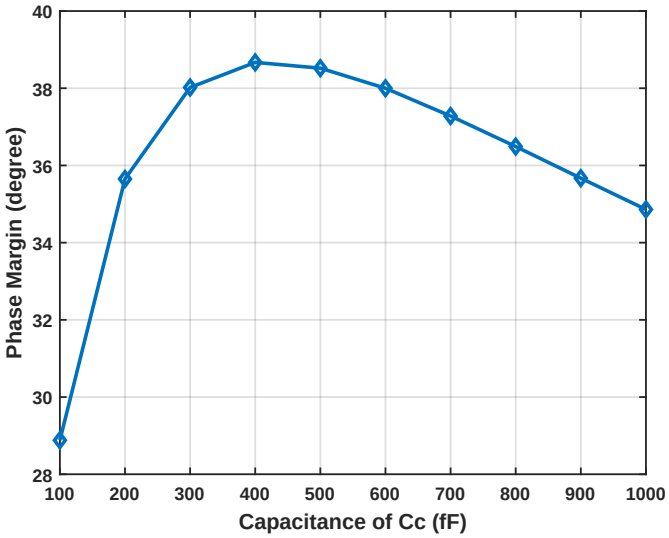

Figure 13. Phase margin as a function of C_C.

4.4. Supply Dependence

The supply dependence of the proposed voltage reference was simulated at room temperature. Figure 14 shows the output voltage and the input difference of the amplifier as functions of VDD. The minimum supply voltage could be as low as 0.8 V, and the line sensitivity (LS) is 0.011%, ranging from 0.8 V to 1.5 V. The maximum supply voltage is mainly limited by the breakdown voltage of V_{DS}. The results also indicate that a lower supply voltage leads to inaccuracy in the specific current generator. The acceptable supply voltage depends not only on the voltage headroom of the PMOS current mirror but also on the allowable amplifier input residue, because the larger the residue, the worse the temperature coefficient of V_{REF}. Figure 15 shows the power supply rejection ratio (PSRR) with a load capacitance of 10 pF at room temperature. Thanks to the additional amplifier, the PSRR is −89 dB at 100 Hz.

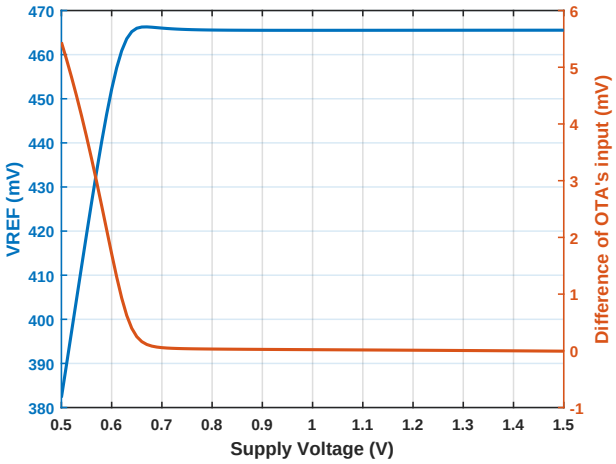

Figure 14. V_{REF} and difference of OTA's input voltage versus supply voltage.

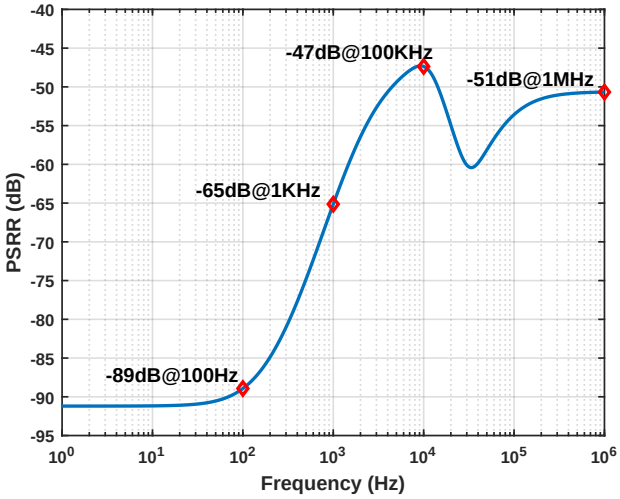

Figure 15. PSRR with a C_L of 10 pF.

Figure 16 shows the layout of the proposed voltage reference. Each part of the circuit is annotated, including the compensation capacitor C_C. The overall area of the core circuit is only 90 µm × 100 µm. Since the size of all NMOS is determined based on the unit cell M_u, the layout of the circuit is highly compact. C_C is composed of a metal–insulator–metal (MIM) capacitor using top metal; thus, it can be stacked on the active device to save area. Dummy transistors are added on both sides of the layout to mitigate the layout-dependent effect (LDE).

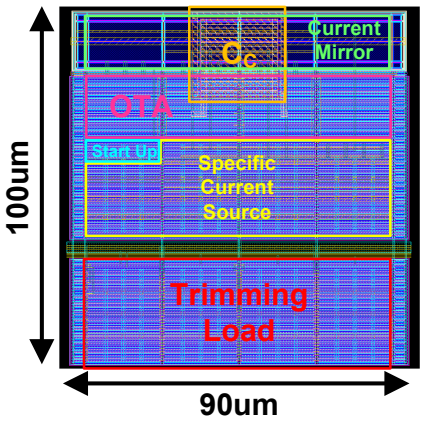

Figure 16. Layout.

Table 2 compares the performance of the proposed V_T-based voltage reference with other reported works. It can be seen that the proposed reference is very competitive in many aspects. We balanced the circuit's power and TC, adding an amplifier to improve LS with an acceptable current consumption. Thus, our design shows excellent supply and temperature independence. Meanwhile, our design only adopts one type of MOSFET, which makes it more efficient in terms of mask layer numbers and process portability. Compared with [32], which also contains one MOSFET type, our design achieves a lower supply voltage and less power consumption. In addition, our design enables the majority of chips to achieve a small TC through a 5-bit trimming, which improves the yield in practical system applications.

Table 2. Comparison of the proposed voltage reference with previous works.

Parameter	This Work	TCASII'23 [1]	TCASII'23 [15]	TCASII'21 [32]	SBCCI'20 [14]	JLPEA'18 [18]
Process (nm)	55	180	65	180	130	350
Temp. Range (°C)	−40–120	−10–100	−20–80	−40–85	−40–125	−70–85
TC (ppm/°C)	21.7	90	79.4	60.86	28.8	42
V_{REF} (mV)	474.4	288	107.2	985	575.2	1520
σ/μ (%)	5.8	0.574	2.4	2.6	4.32	2
Supply (V)	0.8–1.5	0.5–2	0.4–0.8	1.5–6	1–1.8	1.7–3.3
LS (%/V)	0.011	0.23	0.54	0.003	0.071	10
Consumption (nW)	23.2	0.5	56.7	63	36.4	1110
PSRR (dB)	−89 (@100 Hz)	−45 (@100 Hz)	−66.5 (@10 Hz)	−93.3 (@10 Hz)	−54.4 (@100 Hz)	−35 (@100 Hz)
Area (mm^2)	0.009	0.0029	0.0084	0.015	0.0078	0.06
Components	1 Type MOS	3 Types MOS	MOS + Res	2 Types MOS	1 Type MOS	2 Types MOS + Res

5. Conclusions

This paper presents a 55 nm low-power V_T-based voltage reference. The reference proposed only requires MOS transistors, and no BJTs or resistors are needed. A detailed explanation of the operating principle and design of the circuit was given with the EKV model. The reference consists of a novel specific current generator, a simple amplifier, a start-up circuit, and a trimmable output stage.

The simulation results showed that a balanced trade-off between TC and power was achieved. The proposed voltage reference has an average TC of 21.7 ppm/°C with a power consumption of 23.2 nW. The circuit also has excellent supply independence. Its line sensitivity is only 0.011 %/V, and PSRR is −89 dB at 100 Hz. The core area of the circuit is 0.009 mm^2. Therefore, the proposed circuit is a suitable voltage reference module for low-power applications.

Author Contributions: Conceptualization, S.W.; methodology, S.W.; validation, S.W.; writing—original draft, S.W.; writing—review and editing, Z.L. and X.Y.; supervision, K.X.; project administration, H.D. and Z.W. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: Authors Kunpeng Xu, Hongguang Dai and Zhanxia Wu were employed by the company Beijing Smartchip Microelectronics Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or finacial relationships that could be construed as a potential conflict of interest.

Appendix A

In this appendix, the origins of basic EKV equations are derived. Firstly, there are two transport mechanisms in the composition of the MOS transistor: drift current and diffusion current. The total drain current I_D can be expressed as follows:

$$I_D = \mu W\left(-Q_i\frac{d\psi_S}{dx} + U_T\frac{dQ_i}{dx}\right), \tag{A1}$$

where Q_i is the mobile charge density, and ψ_S is the surface potential at the position x along the channel. The diffusion factor varies little across the WI, MI, and SI. Therefore, for diffusion current, the relationship between Q_i and surface potential can be approximated as follows:

$$d\left(-\frac{Q_i}{C_{ox}}\right) = -\left(1+\frac{\gamma}{2\sqrt{\psi_S}}\right)d\psi_S = -nd\psi_S, \tag{A2}$$

where γ is known as the back gate parameter. We normalize the Q_i as follows:

$$q = -\frac{Q_i}{2nU_TC_{ox}}, \tag{A3}$$

Thus, Equation (A2) can be expressed as follows:

$$d\psi_S = -2U_Tdq. \tag{A4}$$

Therefore, we rewrite the differential equation of the drain current:

$$\int_S^D I_Ddx = \int_S^D -2nU_T^2C_{ox}(2q+q)dq. \tag{A5}$$

Finally, we perform the integration from the source terminal to the drain terminal and obtain

$$I_D = 2nU_T^2\mu C_{ox}\frac{W}{L}\cdot\left[\left(q_S^2+q_S\right)-\left(q_D^2+q_D\right)\right]. \tag{A6}$$

Another fundamental physical equation of the EKV model relates the nonequilibrium voltage V and q:

$$Q_i \propto \exp\left(\frac{\psi_S-\phi_F-V}{U_T}\right), \tag{A7}$$

hence,

$$\frac{dQ_i}{Q_i} = \frac{dq}{q} = \frac{d\psi_S-dV}{U_T}. \tag{A8}$$

Substituting Equation (A4) into Equation (A8), we obtain

$$\int_{q_x}^{q_P}\left(2+\frac{1}{q}\right)dq = \int_{V_x}^{V_P}-\frac{1}{U_T}dV. \tag{A9}$$

where q_P denotes the normalized charge density at the pinch-off point and equals one. Thus, we connect the V and q after integration and have Equation (4).

The physical interpretation of the linear relationship between V_P and V_G is relatively complex, and due to text space constraints, the detailed derivation is not provided here. Readers can find a detailed explanation of Equation (5) in reference [23,28].

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