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A Low Power Injection-Locked CDR Using 28 nm FDSOI Technology for Burst-Mode Applications

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Abstract: In this paper, a low-power Injection-Locked Clock and Data Recovery (ILCDR) using a 28 nm Ultra-Thin Body and Box-Fully Depleted Silicon On Insulator (UTBB-FDSOI) technology is presented. The back-gate auto-biasing of UTBB-FDSOI transistors enables the creation of a Quadrature Ring Oscillator (QRO) reducing both size and power consumption compared to an LC tank oscillator. By injecting a digital signal into this circuit, we realize an Injection-Locked Oscillator (ILO) with low jitter. Thanks to the good performance of this oscillator, we propose a low-power ILCDR with fast locking time and low jitter for burst-mode applications. The main novelty consists of the implementation of a complementary QRO based on back-gate control using FDSOI technology to realize a simple and efficient ILCDR circuit. With a Pseudo-Random Binary Sequence (PRBS7) at 868 Mbps, the recovered clock jitter is 26.7 ps (2.3% UIp-p) and the recovered data jitter is 11.9 ps (1% UIp-p). With a 0.6 V power supply, the power consumption is 318µW. All the results presented here are based on post-layout simulations, as no prototypes have been produced. Similarly, we can estimate the surface area of the chip (without the pad ring) at around 6600 μm^2.

Keywords: Clock and Data Recovery (CDR); Quadrature Ring Oscillator (QRO); Injection-Locked Oscillator (ILO); Injection-Locked Clock and Data Recovery (ILCDR); burst-mode; FDSOI technology

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1. Introduction

Generally, synchronous data transmission systems send only the data signal to reduce the bandwidth and power consumption. The receiver has to implement a CDR circuit to perform both the extraction of the transmitted data sequence from the noisy received signal and the recovery of the associated clock timing information [1]. The data must be retimed to remove the jitter accumulated during transmission. The generated clock must have a frequency equal to the data rate and a low jitter because it is the main contributor to the retimed data jitter. To have an optimum sampling of the bits, the rising edges of the restored clock must coincide with the midpoint of each bit. In this case, the sampling occurs farthest from the previous and following data transitions, providing a maximum margin for jitter [2].

In the field of CDR architectures, closed-loop systems, such as Phase Locked Loop (PLL) and Delay Locked Loop (DLL), excel in providing low-jitter performance, making them the preferred choice in many applications [1–6]. However, open-loop CDR structures offer distinct advantages, particularly in terms of low power consumption, fast locking time, and simplicity of design, often resulting in cost-effective solutions [7]. The choice between closed-loop and open-loop CDRs ultimately depends on the specific requirements of the application. Closed-loop systems offer precision and stability but with higher complexity and power consumption. Conversely, open-loop CDRs provide an alternative, particularly suitable for burst-mode communication where speed and efficiency are required.

A 28 nm FDSOI technology allows us to create a complementary inverter by using the back-gate of the transistor to symmetrize its outputs [3]. Complementary inverters allow us

to implement back-gate auto-biasing feedback and to realize a QRO with an even number of inverters. By injecting a signal into this circuit, we create an ILO with low jitter [4]. Thanks to the good performance of this oscillator, we can propose a low-cost and low-power ILCDR with an improved jitter and a fast-locking time for burst-mode applications.

This paper is organized as follows: Section 2 introduces and compares the various types of open-loop CDR. Section 3 presents the circuit implementation of the injection complementary QRO based on the UTBB-FDSOI technology. The proposed ILCDR architecture and the simulation results are described in Section 4, followed by a conclusion of this work in Section 5.

2. CDR Architectures

CDR can be classified into two major categories. The first structures are using feedback phase tracking like Phase Locked Loop (PLL) or Delay Locked Loop (DLL). These closed-loop architectures are the most used essentially for their low jitter [1,2,5,6]. The second ones are open loop structures with low power, fast locking time, and simple and low-cost design [7].

Open-loop CDR structures aim at local area networks, passive optical networks, and Serializer/Deserializer applications in which jitter accumulation is not a major problem but need a burst-mode operation to extract a synchronous clock and recover the received data quickly for each asynchronous packet [1,7–9]. An open-loop CDR is usually based on a gated oscillator, a high-Q bandpass filter, or an ILO circuit [7] as shown in Figure 1.

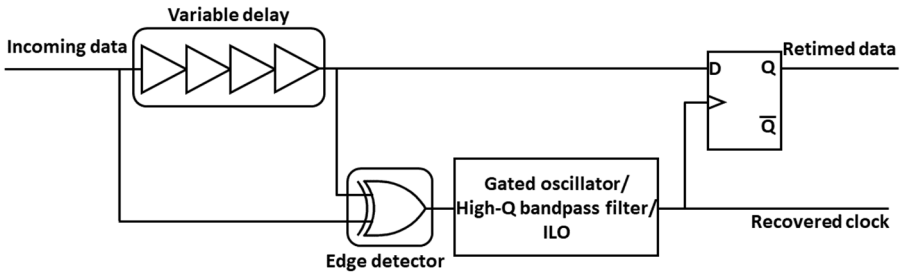


Figure 1. The standard architecture of an open-loop CDR [7].

Driven by the recovered clock, the D Flip-Flop (DFF) retimes the incoming data. The variable delay buffer provides an adjustable delay of the input data to align it with the clock edge (the best time is the midpoint of each bit). It can be controlled externally to correct the Process, Voltage, and Temperature (PVT) variations. The edge detector is generally an XOR gate that will generate pulses at the input data bit frequency that commands the oscillator.

The high-Q filter-based CDR, such as an LC filter, directly samples the clock but its integration on a chip is difficult and there is no input jitter rejection [1,7]. The gated oscillator circuit aligns this phase with every input data transition, so it also has no input jitter rejection and a strong sensitivity to PVT variations [1].

We propose the implementation of an ILCDR to achieve a rapid acquisition time and robust jitter tolerance. Notably, this type of CDR exhibits an input-jitter-filtering nature, distinguishing it from CDRs relying on the high-Q filter or gated oscillator [7,10]. Additionally, injecting the output of the edge detector into the ILO forces it to lock onto this frequency. This allows for some process variation in the oscillator design, thereby enhancing PVT variation tolerance. Certainly, injecting a periodic signal into an oscillator leads to pulling or locking phenomena [11]. Injection locking occurs when an oscillation source is shifted by an interference signal with a frequency very close to its own. In this case, the output frequency will be locked to the frequency of the interference signal instead of its own free-running frequency [4]. The principle of a simple injection structure is shown in Figure 2 [4].

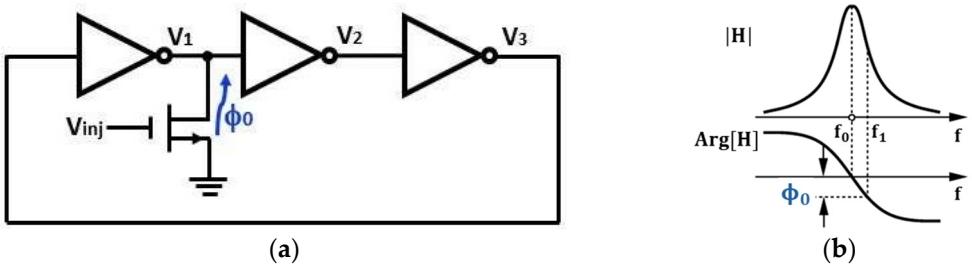


Figure 2. Injection modeling in a Ring Oscillator (RO) [4]: (**a**) RO with injection; (**b**) Oscillation frequency shift.

A three-stage ring oscillator oscillates at the frequency f_0. The introduction of a phase shift ϕ_0 in this loop modifies the oscillation frequency because the system phase deviates by a value equal to ϕ_0. Figure 2b shows the change in the oscillation frequency from f_0 to f1 induced by the effect of ϕ_0. Assuming that ϕ_0 is generated by an injection voltage V_{inj}, the system then oscillates at the injection frequency f_{inj} [4].

The ILCDR structure may include a closed-loop, typically designed with a PLL, to conduct the input data frequency tracking and adjust the free-running frequency of the ILO, as illustrated in Figure 3.

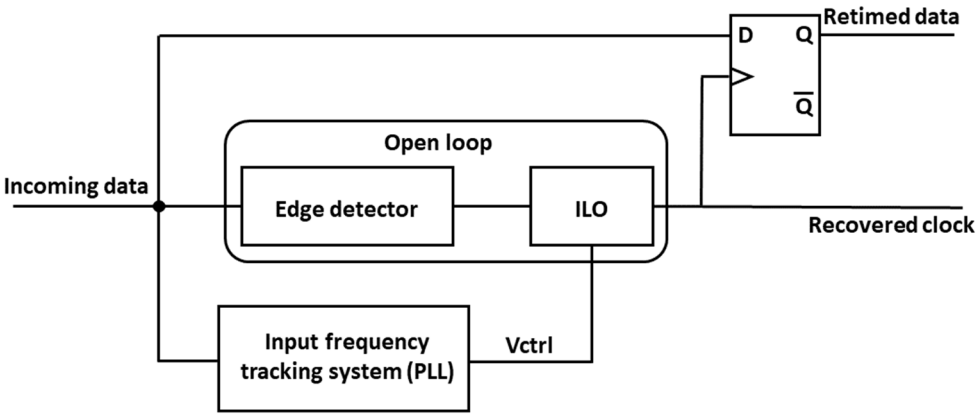


Figure 3. ILCDR structure with an input frequency tracking system [7].

In case of a long sequence of 0 or 1, the input frequency tracking system improves the BER of the ILCDR by reducing the difference between the free-running frequency and the input data frequency of the ILO [7]. Adding a PLL increases the cost, complexity, power consumption, and die area of the CDR. In this study, our proposition aims to enhance the jitter of the standard architecture of the open-loop ILCDR without utilizing a PLL, thus maintaining a low-cost and low-power design.

3. Injection Complementary QRO

3.1. RO Design

To perform a quadratic demodulation, it is necessary to have at least two 90°-phase shifted signals. A VCO enables this operation to be carried out [12]. LC tanks are the most popular circuits to realize a VCO. On the contrary, RO is known to exhibit high phase noise, but this design will address aggressively the size and power consumption reduction. We have proposed a new inverter topology to realize a VCO using FDSOI technology [13].

The access to UTBB transistor Back-Gates offers an extended control of the threshold voltages of the transistors (Figure 4), opening new opportunities for exciting performances [14–19]. We have proposed a new complementary structure based on a pair of Back-gate cross-coupled inverters offering a fully symmetrical operation of complementary signals, as shown in Figure 5 [3].

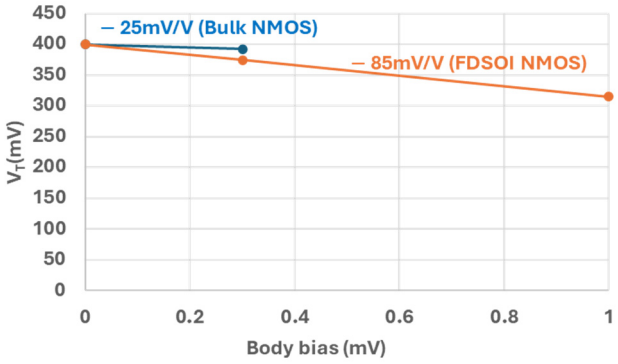


Figure 4. Body-biasing effect for similar size transistors in 28 nm FDSOI (blue curve) and bulk (orange curve) from STMicroelectronics.

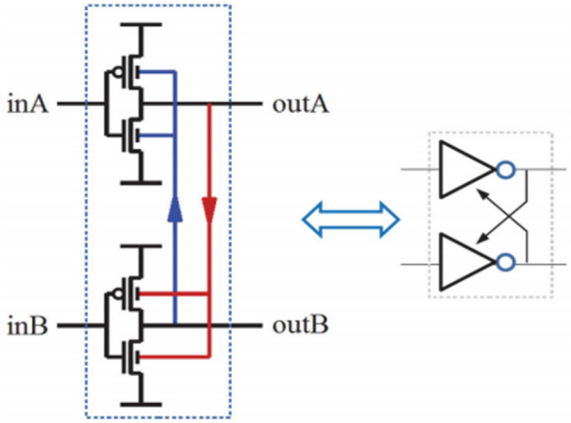


Figure 5. A complementary inverter based on a pair of back-gate cross-coupled (blue and red wires) [3].

The main idea is as follows: frequently, the NMOS transistor, the faster one, is going to accelerate the conduction of the slower PMOS transistor, and reciprocally. So, by connecting the output of each inverter to the back-gate of the other, the faster stage will accelerate the slower one, realizing a symmetrization of the two stages. The complementary outputs are crossing at V_{DD} divided by 2. Monte Carlo (MC) simulations exhibit a mean value of $V_{DD}/2 = 500$ mV, and the standard deviation is about $\sigma = 2.7$ mV [13].

The AC simulation of the complementary inverter shows a gain of 17 dB and a bandwidth of 4.4 GHz [4] (see Figure 6). The input signals are amplified in one group and then fed to the other group via backgate feedback. The bandwidth of the complementary inverters reflects their ability to amplify signals across frequencies maintained by the feedback mechanism, enabling operation up to 4.4 GHz. Phase stability and delay performance remain excellent in the low-frequency range, with phase changes maintained at 180 degrees up to 10 MHz.

This new complementary inverter will offer two other advantages very important for ring oscillator realization. The first one concerns the duty cycle, which has to be close to 50% and low jitter [3]. Secondly, this topology enables an oscillator with an even number of inverters (cf. Figure 7) and provides a common-mode feedback loop for the RO stage [4]. This latter feature makes it easy to perform a QRO: four identical outputs with the same amplitude and same frequency but with different phases (0°, 90°, 180°, and 270°).

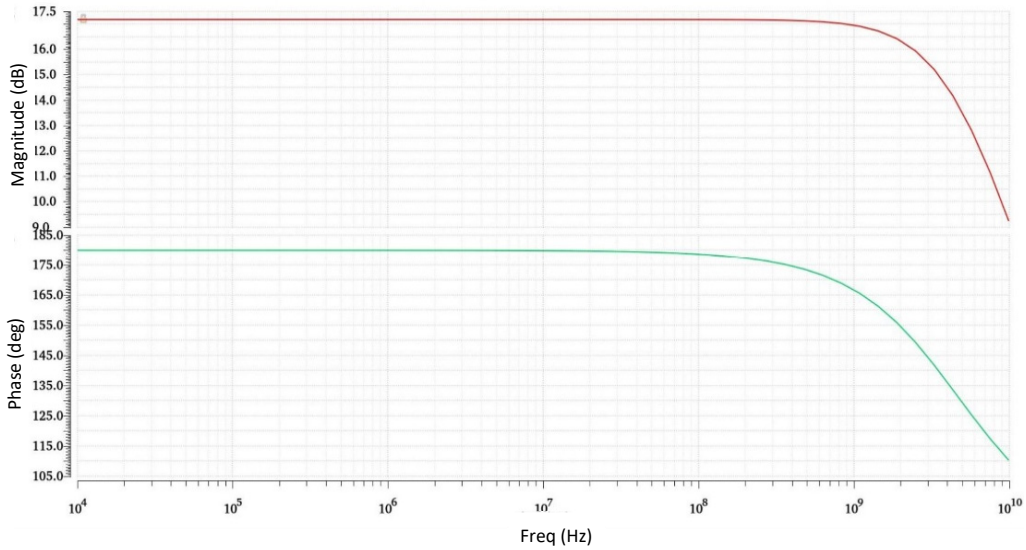


Figure 6. AC frequency response of complementary inverter [4].

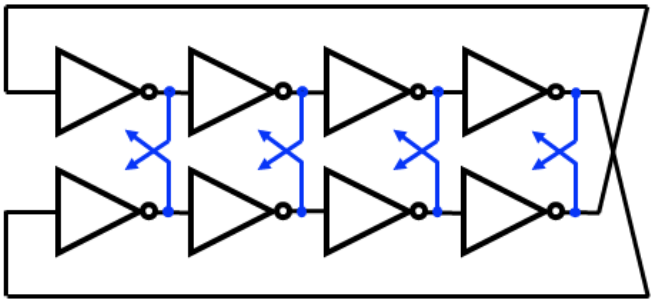


Figure 7. QRO with four inverters (back-gates cross-coupled in blue) [4].

The transient result is shown in Figure 8, where the complementary outputs are crossed at V_{DD} divided by 2. The 8 single-ended outputs are plotted which produces a clock equally spaced by 45°. In CDR, the 8-phase output provides the ability to create a variable delay.

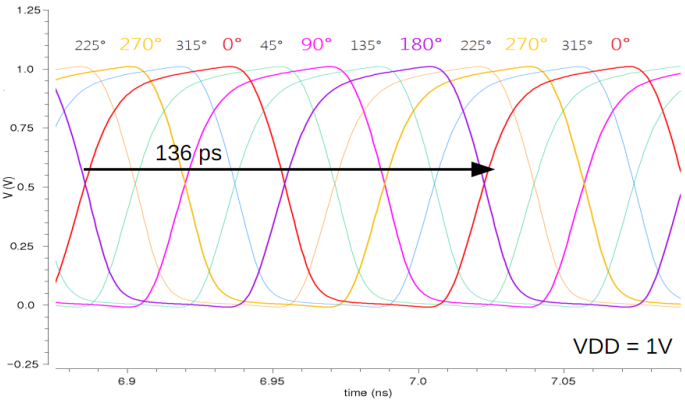


Figure 8. Transient simulation results of the QRO at 7.3 Ghz [13].

3.2. Injection Complementary QRO

Figure 9 shows the schematic of the proposed design. The QRO may not oscillate automatically, so it needs a startup design. The complementary signal output for a complementary inverter is a necessary condition for the oscillator to start. The use of NMOS transistors as the switch can only pull the voltage down to 0, and the complementary signal

can be obtained from the output of the next stage inverter, so a two-stage complementary inverter should be considered to study the start of the oscillator [3].

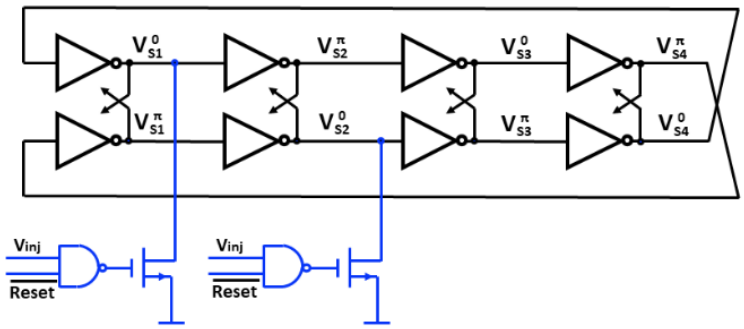


Figure 9. Single injection complementary QRO (injection and reset in blue) [4].

To ensure normal oscillation of the QRO and obtain a complementary signal pair, the initialization configuration should involve initializing both outputs: one from the first stage and the other output of the second stage (Reset). This reset mechanism is detailed in [3]. Simultaneously, the injection signal V_{inj} is also transmitted through the two NMOS transistors to generate the complementary signals [4].

To make the Reset signal and the injected signal work together and not interfere with each other, it is necessary to use these two signals as the two input signals of a NAND gate. In practice so as not to unbalance the different outputs of the QRO, the same capacitance values C of the Reset transistors (T1 and T2) will be added to all the other outputs.

According to the principle of injection locking, this structure can expand the range of oscillation frequency. The circuit starts to oscillate when V_{DD} is 0.4 V, and as V_{DD} increases, the locking range becomes larger.

In this paper, we choose to present the results at 868 Mhz for wireless communications, notably for IoT protocols but our circuit works until 7.3 Ghz in free frequency without injection as depicted in Figure 10. When the oscillation frequency is 868 MHz, the injection locking range can be expanded from 690 MHz to 1 GHz, which is 36% of 868 MHz, as shown in Figure 10 [4].

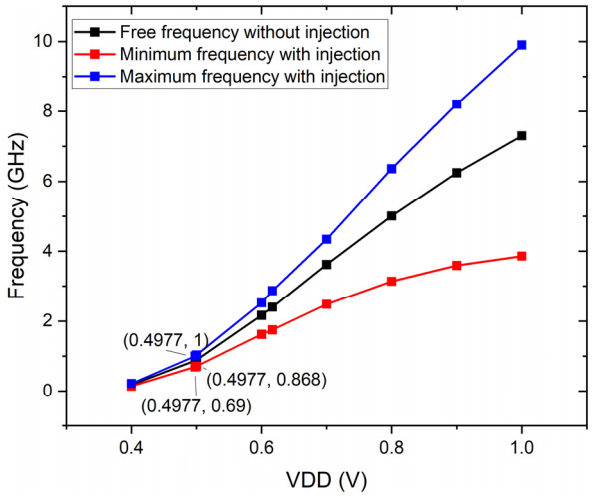


Figure 10. Tuning range versus free-running frequency [4].

Figure 11 compares the relationship between oscillation frequency and phase noise with or without injection signal [4]. Due to thermal noise and flicker noise, the phase error of a free-running QRO will increase randomly compared to an ideal QRO. The injection pulse forces the edge of the output signal to move back to the correct position every injection

period, so the phase error no longer accumulates, and the phase noise can be reduced. In contrast, the phase noise measured at 1 MHz is −117 dBc/Hz, which is 34 dB less than the phase noise of no injection signal.

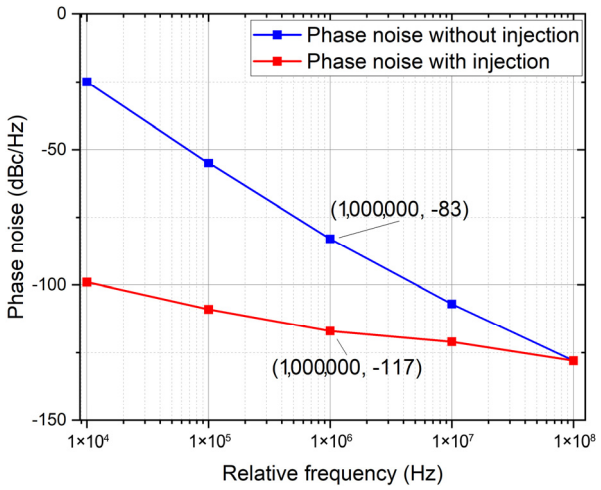


Figure 11. Comparison of phase noise as a function of relative frequency [4].

4. Proposed ILCDR

4.1. Timing Analysis of the Proposed ILCDR

Figure 12 depicts a simplified block diagram of the injection CDR. The input signal is a PRBS7 at 868 Mbps [4]. After the pulse generator, a pseudo-random pulse signal is obtained at the rate multiplied by 2, which is 1.736 Gbps. After injecting the pulse signal into the complementary RO, it outputs a periodic signal with a frequency of 868 MHz, which is the recovered clock signal. The recovered data signal is the output signal with a rate of 868 Mbps after sampling.

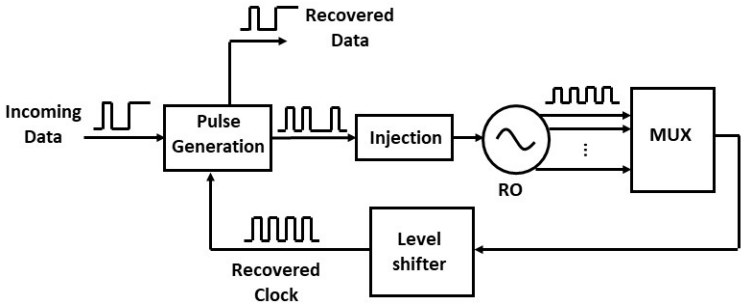


Figure 12. Simplified block diagram of the proposed ILCDR [4].

Equation (1) indicates the behavior of the injection current pulse:

$$x(t) = \begin{cases} I_{injection} & 0 < t < \gamma \\ 0 & \gamma < t < T \end{cases}, \quad (1)$$

where γ denotes the pulse width and t denotes the period of the injected pulse [20]. Experimental results on the 8 quadrature-phase output signals of the complementary RO show that the maximum value of γ needs to be less than 0.5 T to achieve an acceptable jitter. Indeed, injection intensity is related to the duty cycle of the injection signal, which affects the injection performance. The best pulse signal width obtained to minimize the jitter of the ILCDR system is equal to a quarter-bit period ($T_b/4$) as shown in Figure 13 [4].

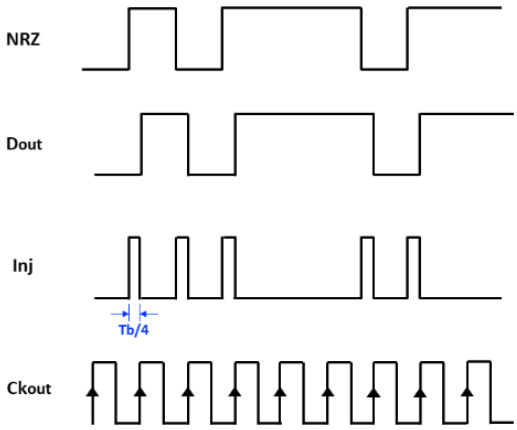


Figure 13. Timing diagram of the proposed ILCDR [4].

4.2. Architecture

Figure 14 illustrates the architecture of the proposed full-rate ILCDR, which includes a pulse signal generation block consisting of a DFF and an XNOR gate, an injection block, and a complementary RO block [4]. The incoming data, NRZ code, whose power spectral density is zero at the frequency component of the clock or its multiples, the clock signal cannot be extracted. By passing the NRZ data through a DFF and an exclusive-OR gate, RZ data can be obtained from which the clock frequency components may be extracted [21]. Injecting the pulse signal M_{inj} into a complementary ring oscillator outputs eight periodic signals with the same rate and different phases. One of these 8-phase signals is selected as the clock signal which contains a variable phase, so a variable delay consisting of several inverters is no longer required, which could simplify the circuit structure and thus reduce the power consumption and the chip size of the ILCDR. One of the 8 phases is manually selected in the simulation stage and is sent to the DFF. A binary selector and an 8-to-1 MUX will be used to select the phase for the manufacturing stage. The principle of manual selection is to obtain smaller jitter. Indeed, the output signal makes the injection pulse width match $T_b/4$ minimizing the jitter of the CDR circuit. The input data is XNORed with the output signal of the DFF to obtain a pulse signal with 2 times the bit rate. The recovery data D_{out} is obtained after the decision circuit DFF is clocked by the recovered clock CK_{OUT}.

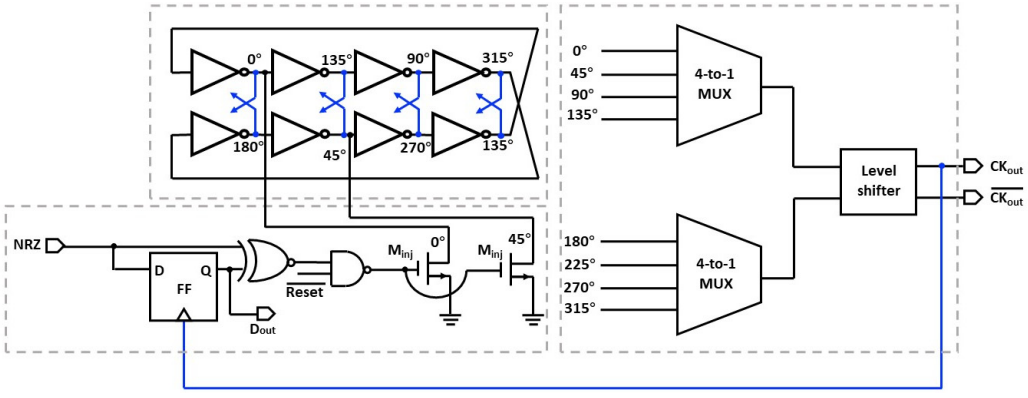


Figure 14. The architecture of the proposed ILCDR (DFF clocked by CK_{OUT} in blue) [4].

In general, the QRO takes advantage of the back-gate control structure that reduces the error in each transition. Random jitter (thermal noise, flicker noise, etc.) can be corrected periodically using injection techniques. Furthermore, a DFF was used to implement the functions of pulse signal generation and recovery data sampling simultaneously.

4.3. Schematic Simulation Results

We utilized the 28 nm UTBB-FDSOI transistor model of STMicroelectronics. It is important to note that the V_{DD} in this environment is set to 1 V. We modulated V_{DD} to control the oscillation frequency, as depicted in Figure 10. With a supply voltage of 0.5 V, the proposed ILCDR achieves a wide operation range of 868 Mbps. The dimensions of the RO transistors are 4.1 µm/30 nm for the PMOS and 2 µm/60 nm for the NMOS.

Figure 15 illustrates the results of transient simulations performed on the complementary ILCDR, where D_{in} is the input data, RO_{out} is the output of the injected complementary ring oscillator, CK is the recovered clock signal and D_{out} is the recovered data [4]. Simultaneously, Figure 16 shows the variation curve of frequency during the locking process. The figure illustrates that when the input data is PRBS7 random data with an 868 Mbps data rate, the locking time of the ILCDR is about 5 ns, and the clock frequency stabilizes around 868 MHz after locking [4].

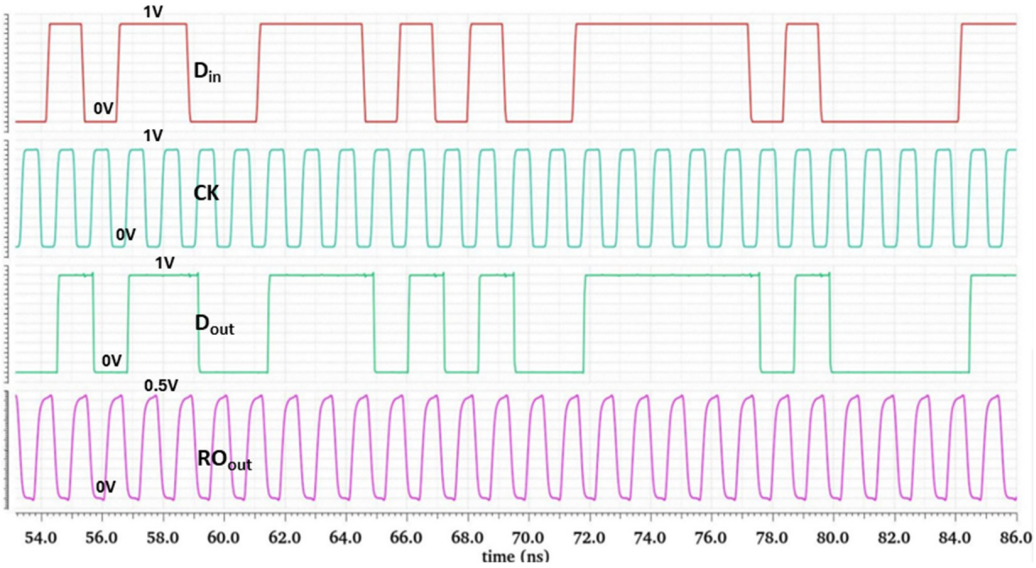


Figure 15. Transient simulation result of complementary ILCDR at 868 MHz [4].

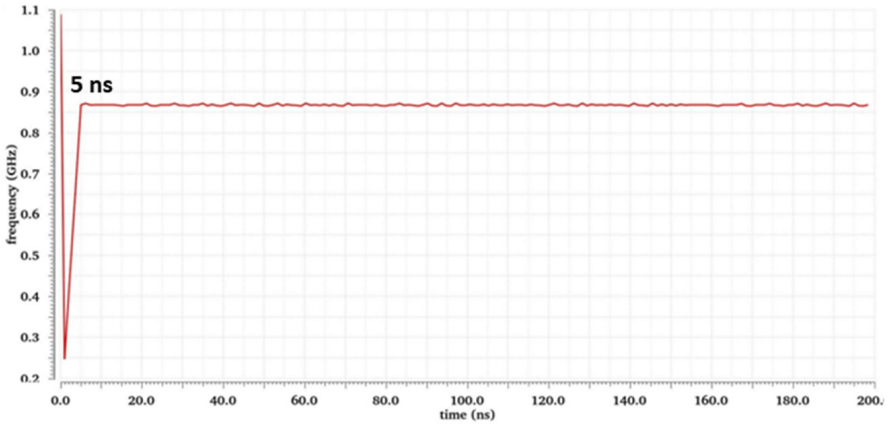


Figure 16. The frequency of the clock signal at 868 MHz [4].

Based on over 10,000 cycles of transient simulations, Figure 17 shows the jitter of the recovered clock and recovered data for the PRBS7 input data [4]. The jitter is 7.4 ps (0.6%UI) of the clock and 2.3 ps (0.2%UI) of the PRBS7 data. The locking range is 860–1100 Mbps without errors of the input PRBS7, which is 28% of 868 Mbps. After the level shifter, the output signal reaches 1 V.

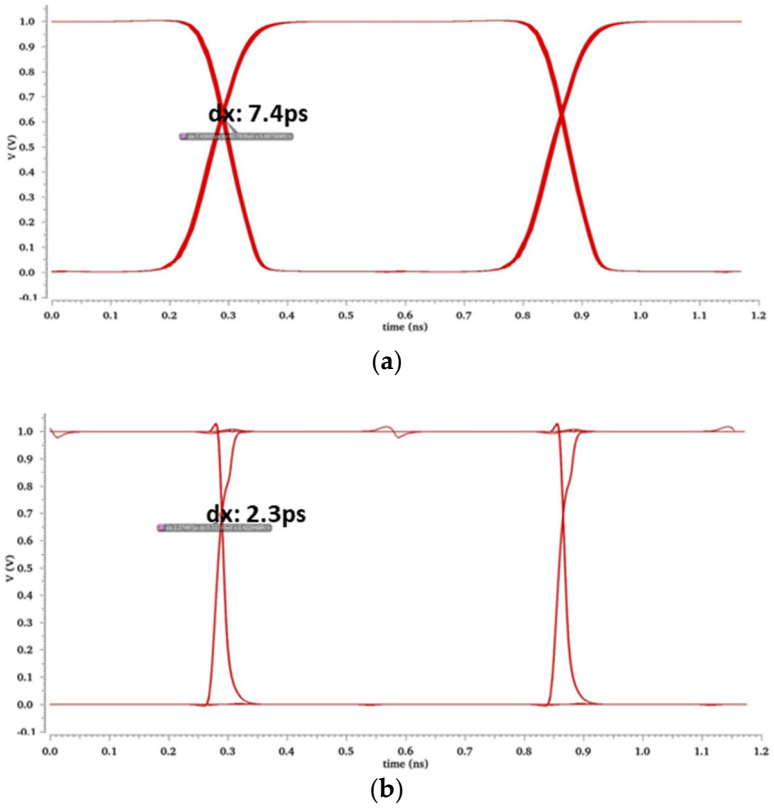


Figure 17. Eye diagram of (**a**) Recovered clock and (**b**) Recovered data [4].

Figure 18 presents the phase noise when a periodic injection signal is introduced. The phase noise for the injection circuit is −122 dBc/Hz@1 MHz [4].

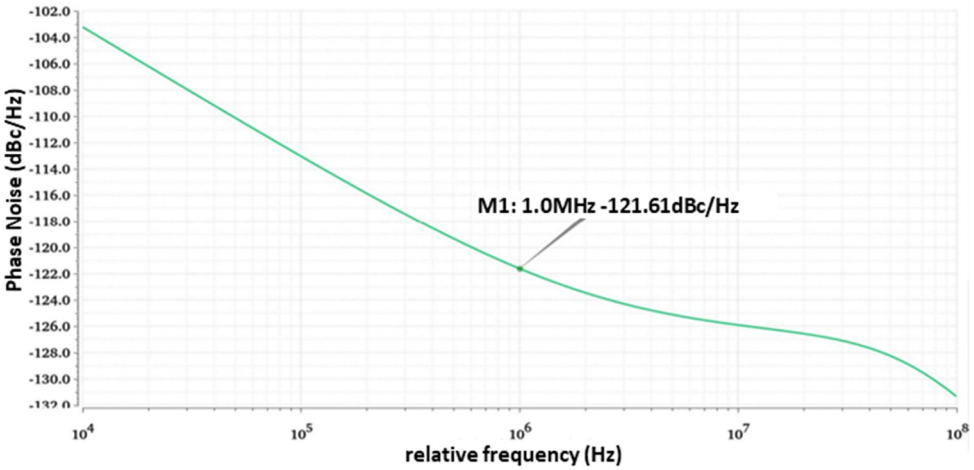


Figure 18. Phase noise of CDR as a function of relative frequency [4].

It is obtained from transient simulation that when the input data is a random code of PRBS7 at 868 Mbps, the power consumption is 235 µW when the CDR circuit is locked. The percentage of power consumption of each part of the circuit is shown in Figure 19, where the RO consumes 49 µW and the other modules consume 186 µW. The power efficiency of CDR is:

$$\text{Power efficiency} = \frac{0.235\ \text{mW}}{0.868\ \text{GHz}} = 0.27\ \text{pJ/bit} \quad (2)$$

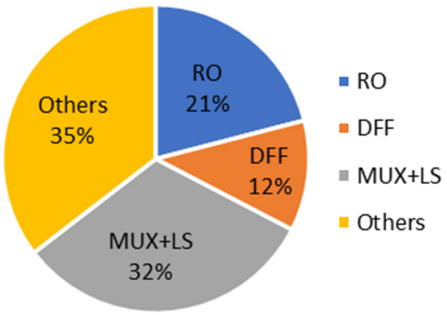


Figure 19. Percentage of power consumption of each part of the circuit.

In our CDR circuit, the frequency of the RO is directly controlled by V_{DD}. Therefore, our focus will be on process and temperature variations. Table 1 shows the output frequency of the CDR for the 868 Mbps PRBS7 input data in different cases, including the fastest case (FF corner with 125 °C) and the slowest case (SS with corner −40 °C) [22].

Table 1. Output frequency (GHz) of complementary ILCDR at different process corners and temperatures with 868 Mbps PRBS7 input data.

Process	V_{DD} (V)	Temperature (°C)	Ouput Frequency (GHz)
TT	0.5	27	0.868
	0.5	125	1.45
	0.5	−40	0.548
FF	0.5	27	1.09
	0.5	125	1.73
SS	0.5	27	0.712
	0.5	−40	0.425

Based on the results in Table 1, it can be observed that temperature has a more significant impact on the structure for an input rate of 868 Mbps, leading to harmonic injection in both the fastest and slowest cases. In the fastest case, the output frequency is close to 2 × 868 MHz, resulting in 1.736 GHz. Conversely, in the slowest case, the output frequency is close to 868 MHz/2, resulting in 434 MHz.

A Monte Carlo, incorporating random statistical variation, was conducted on the ILCDR to analyze the resulting clock frequency, involving 500 data points. The histogram plot in Figure 20 illustrates the approximate probability distribution [4].

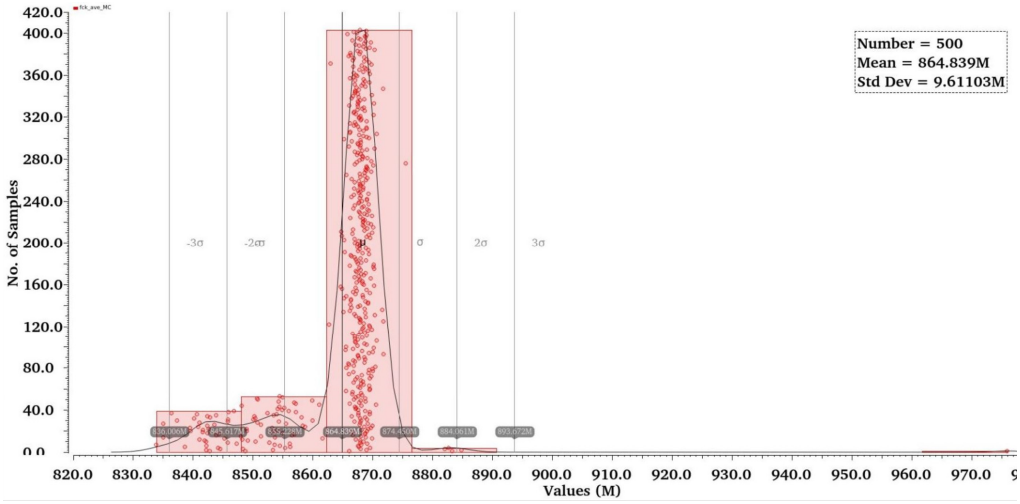


Figure 20. Monte Carlo result of clock frequency at 868 MHz with 500 data points [4].

Despite the mean of the output clock frequency is 865 MHz (i.e., 864.8 MHz), a significant concentration of data points is observed near 868 MHz. The standard deviation is calculated to be 9.6 MHz. The MC simulation reveals that the variability attributed to the manufacturing process on the oscillation frequency remains low, approximately $3\sigma/\text{Mean} = 27/868 = 3.1\%$ maximum relative deviation.

4.4. Layout Design and Post-Layout Simulation

Figure 21 illustrates the structural arrangement of the complementary inverter layout topology [4]. In this configuration, a symmetrical layout of four transistors and their corresponding ports is displayed, taking advantage of the balanced arrangement between the various circuit elements. This symmetry serves a dual purpose: firstly, it helps to simplify the complex circuit layout and secondly, it has a key role in enhancing the overall stability of the system.

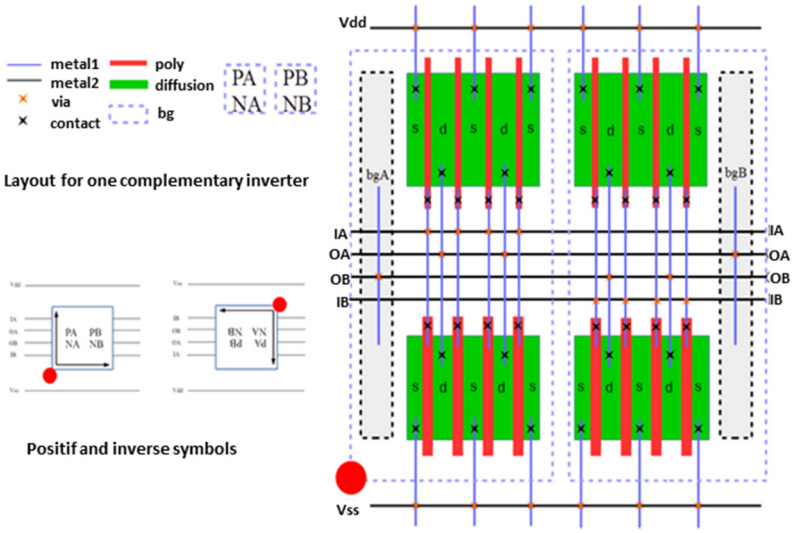


Figure 21. Layout topology of one complementary inverter [4].

Figure 22 illustrates the configuration of the complementary inverter, detailing the precise placement and interconnections of the transistors and ports, with a layout area of approximately 8×8 μm^2 [4].

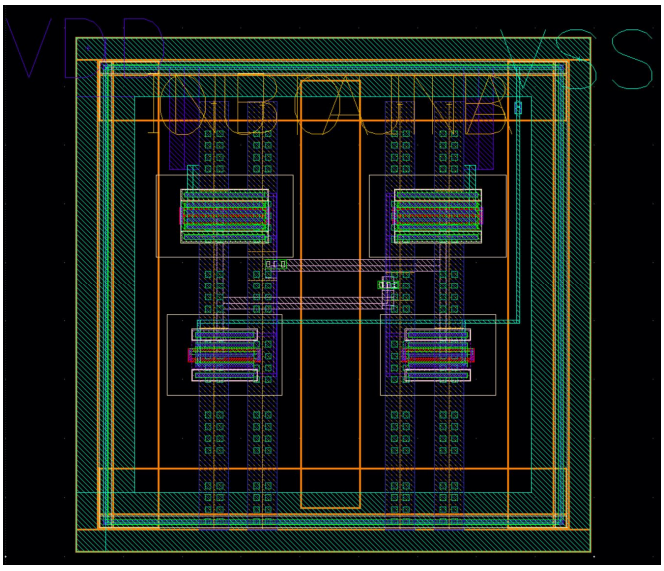


Figure 22. Layout design of complementary inverter (8×8 μm^2) [4].

Figure 23 graphically illustrates the layout configuration of a complementary RO [4]. In this case, the fundamental objective is to systematically organize the four complementary inverters into a symmetrical layout. The symmetrical arrangement is designed to minimize the variations in parasitic effects between each complementary inverter, ensuring uniform rise and fall times. This enhances both the signal integrity and overall performance stability of the complementary ring oscillator. Figure 24 provides a comprehensive view of the layout design of the complementary RO, including the start-up circuit [4].

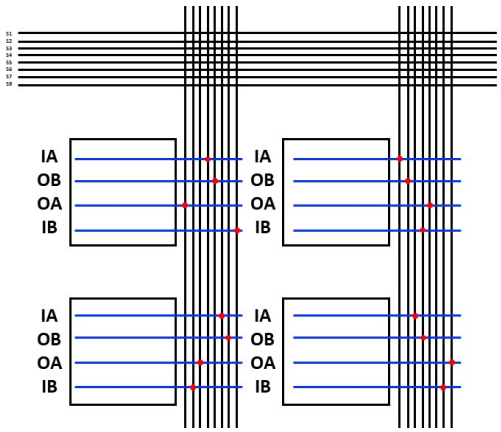


Figure 23. Layout topology of one complementary RO [4].

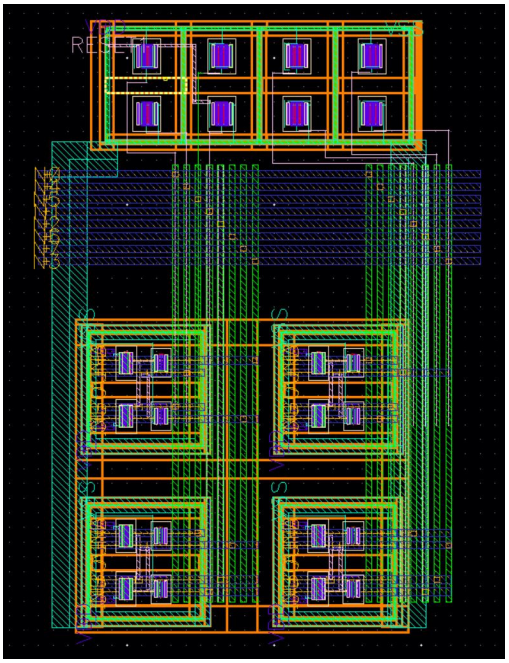


Figure 24. Layout design of complementary RO (40×30 μm^2) [4].

First, the schematic and layout of the complementary inverter were simulated for comparative analysis. The transient simulation results are shown in Figure 25 [4]. The results of the schematic simulation and the post-layout simulation are consistent to a large extent, with the main difference being that the rise time and the fall time of the post-layout simulation are both slightly extended.

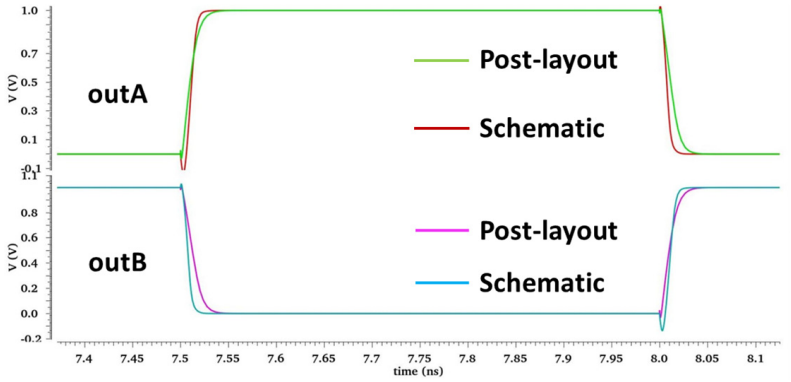


Figure 25. Transient simulation results for the complementary inverter [4].

Based on this framework, we performed a similar comparative analysis for the simulation of a complementary RO. In the schematic simulation, the oscillator operates at a frequency of 868 MHz with a supply voltage of 0.5 V. However, in post-layout simulations, the oscillation frequency decreases to 285 MHz with a supply voltage of 0.5 V. This reduction can be attributed to resistance effects and parasitic capacitance. Figure 26 depicts the transient simulation results.

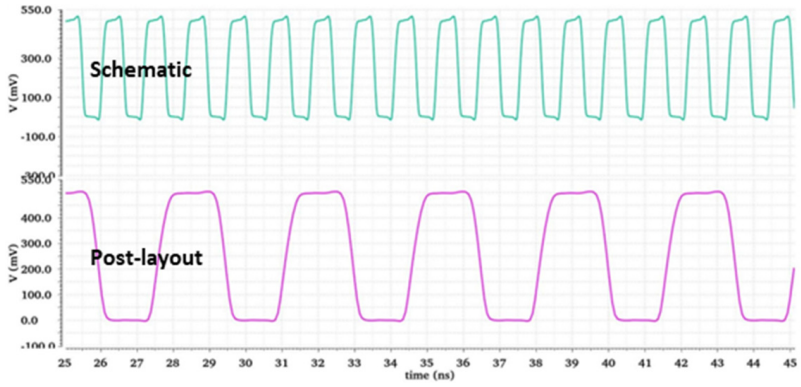
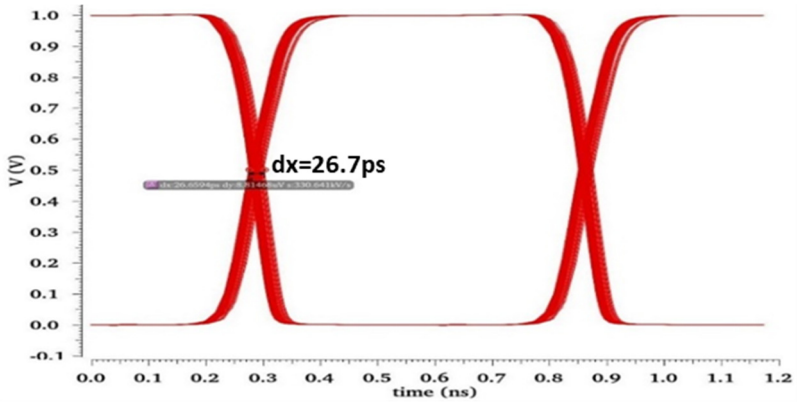


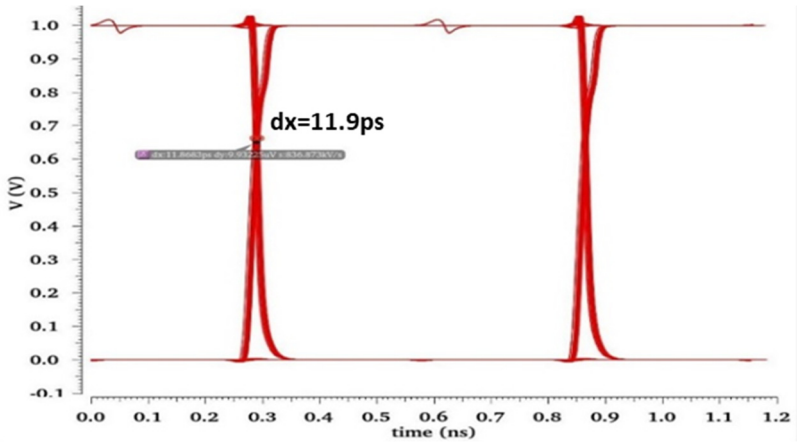
Figure 26. Transient simulation results for complementary RO.

To compensate for resistance effects and parasitic capacitance in the layout, we have adjusted the V_{DD} from 0.5 V to a higher level of 0.63 V based on the simulation data results. The aim was to achieve 868 MHz ILCDR operational functionality to compare with the schematic simulation result. This has been shown to help reduce the effects of parasitic components, thus contributing to the expected performance of the ILCDR. The adjusted ILCDR has a locking time of approximately 5 ns and the clock frequency is stabilized around the 868 MHz target frequency.

After confirming the proper functionality of the CDR circuit, we turned our focus to assessing the jitter performance of both the clock and the output data using eye diagram analysis. Figure 27 presents these findings, indicating a clock jitter of around 26.7 ps (2.3% UI) and a recovered data jitter of approximately 11.9 ps (1% UI) [4]. Moreover, when exposed to a periodic input signal, this CDR demonstrates a phase noise of −118 dBc/Hz@1 MHz. The ILCDR consumes 318 µW, and the power efficiency is 0.318/0.868 = 0.37 pJ/bit.



(**a**)



(**b**)

Figure 27. Eye diagram of (**a**) Recovered clock and (**b**) Recovered data [4].

Table 2 offers a performance comparison between the schematic and post-layout simulations. The post-layout results reveal an increase in phase noise and peak-to-peak jitter compared to the schematic outcomes. This difference is attributed to the impact of parasitic resistance and parasitic capacitance associated with the metal interconnects on the RO's performance. Furthermore, the elevation of V_{DD} to achieve the target frequency of 868 MHz leads to higher power consumption in post-layout simulation.

Table 2. Comparison between schematic and post layout of the ILCDR at 868 MHz.

	V_{DD} (V)	CK Jitter	PN (dBc/Hz@1 MHz)	Power Consumption (µW)
Schematic	0.5	0.6%UI	−122	235
Post-layout	0.63	2.3%UI	−118	318

Table 3 enumerates the schematic and post-layout simulation outcomes for the complementary ILCDR under various processes and temperatures. Notably, the post-layout simulation results exhibit relatively greater stability during the process and temperature variations compared to the schematic because the V_{DD} is increased to 0.63 V in the post-layout (0.5 V in the schematic). Indeed, in our CDR circuit, the frequency of RO is directly controlled by V_{DD}. To improve frequency stability with respect to temperature, we are considering implementing the solution proposed by [23], which is simple and low power.

Table 3. Output frequency of complementary ILCDR at different process corners and temperatures with 868 Mbps PRBS7 input data.

	TT, 27 °C (Typical)	**FF, 27 °C**	**FF, 125 °C (Fastest)**	**SS, 27 °C**	**SS, −40 °C (Slowest)**
Schematic	868 MHz	1.09 GHz	1.73 GHz	712 MHz	425 MHz
Post-layout	868 MHz	1.03 GHz	1.245 GHz	757 MHz	595 MHz

5. Conclusions and State-of-the-Art Comparisons

A performance comparison between some recently published CDRs and our work is presented in Table 4.

Table 4. CDR performance summary and comparison.

	[24]	[25]	[26]	[27]	[28]	**This Work**	
Technology (nm)	28	28	40	28	180	28	
Architecture	Half rate	Half rate	Half rate	Half rate	Full rate	Full rate	
CDR Type	PLL	Injection	PLL	PLL	Injection	Injection	
Supply Voltage (V)	1.0	0.9	1.2	1.0	1.8	0.6	0.7
Data rate (Gbps)	10	10	50	20	3.2	0.868	2.4
p-p Jitter (ps)	8.8	26.8	1.6	N/A	6.4 mUI	26.7	10.9
Power Dissipation (mW)	33	12.8	450	21.5	34.6	0.32	0.9
Power efficiency (pJ/bit)	3.3	1.28	9	1.08	10.81	0.37	0.37
Core area (mm^2)	0.48	0.03	N/A	N/A	0.10	0.0012 (RO) 0.0066 (CDR) *	

* Estimated value.

Thanks to FDSOI technology, we have proposed to implement a novel cross-coupled back-gate technique to improve analog and mixed-signal cells and to decrease the surface of the integrated circuit. Thanks to this technique, we implemented a QRO based on complementary logic and inverters. This type of QRO is very efficient for low-power and low-frequency applications. Based on the back-gate structure, the proposed ILCDR significantly simplifies the design and, therefore, greatly reduces power consumption and surface. The ILCDR extracts an 868 MHz clock signal for the same bit rate as random input data. Featuring back-gate and injection technology, it exhibits a desirable jitter performance.

Subsequently, we conduct a post-simulation analysis of the ILCDR. Despite the oscillation frequency being reduced to one-third of the schematic level due to resistance effects and parasitic capacitance in the post-simulation, we successfully achieved the expected frequency of the CDR by increasing the V_{DD}. In the post-layout simulations at 868 Mhz, the peak-to-peak jitter is 26.7 ps (2.3% UIp-p) and 11.9 ps (1% UIp-p) for the recovered clock and data signal, respectively. The power consumption for the ILCDR is 318µW and the power efficiency of 0.37 pJ/bit is relatively good. The power consumption rises by 35%, and the phase noise increases by 4 dB compared to the schematic simulation results. To provide a fairer comparison in Table 4, we also conducted measurements in the post-layout simulation at 2.4 Ghz for wireless communications using IoT protocols by increasing V_{DD} to 0.7 V. In this case, the peak-to-peak jitter is 10.9 ps (2.6% UIp-p) for the recovered clock signal and 5.8 ps (1.4% UIp-p) for the data signal. The power consumption for the ILCDR increases to 897 µW, while its power efficiency remains at 0.37 pJ/bit. The ILCDR maintains its attributes of low jitter, low power, small surface area, and substantial energy efficiency. Our next step is to add a circuit [23] to improve the stability of the frequency as a function of temperature.

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Conflicts of Interest: The authors declare no conflicts of interest.

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