



Article

A Power-Efficient 16-bit 1-MS/s Successive Approximation Register Analog-to-Digital Converter with Digital Calibration in 0.18 μm Complementary Metal Oxide Semiconductor

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Abstract: A power-efficient 16-bit 1-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) is presented in this paper. High-bit sampling makes the bridge capacitance in the digital-to-analog converter (DAC) a unit one, eliminating fractional capacitance mismatch. The high-precision comparator is composed of a four-stage preamplifier and a strong-arm latch, with auto-zeroing used to mitigate input offset further. Digital foreground calibration based on low-bit weight is implemented to correct DAC capacitance mismatch. The post-layout simulation results show that the core ADC achieves 95.61 dB SNDR and 105.1 dB SFDR with calibration, consuming 5.4 mW power under a 3.3 V supply voltage, corresponding to a Schreier figure of merit (FoM) of 175.3 dB. The ADC core area is 1.06 mm² in the 180 nm CMOS technology.

Keywords: analog-to-digital converter (ADC); successive approximation register (SAR); digital calibration; high precision



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1. Introduction

The majority of signals in nature are analog signals, and in order to take full advantage of the computing performance of digital circuits, an analog-to-digital converter (ADC) is essential. ADCs are responsible for converting an analog signal, which is continuous in both time and amplitude, into a discrete digital signal that can be processed by a digital circuit. ADCs are increasingly the performance bottleneck of overall electronic systems. In recent years, successive approximation register (SAR) ADCs become popular due to their low power consumption, small area and simple structure [1–3]. High-resolution SAR ADCs with relatively low speed are widely used in applications ranging from instrumentation and medical electronics to mobile wearable devices, etc. [4–8].

However, as the resolution exceeds 10 bits, the accuracy of the SAR ADC is affected by capacitance mismatch, comparator noise and offset, etc. [9–12]. To mitigate comparator offset, three techniques are employed: trimming, chopping and auto-zeroing. Trimming is used to measure and compensate offset voltage by a specific method after chip manufacturing, but it is not suitable for high-precision designs. Chopping [13] utilizes continuous-time modulation to shift the offset voltage to a higher frequency for filtering. This technique can not only eliminate the offset voltage of the comparator but also mitigate the noise. However, this method requires a higher frequency clock and results in a more complex circuit design. Auto-zeroing [14–16] is to store the offset voltage in the form of charge on the capacitance. The role of the capacitance is equivalent to that of a voltage source; its size is approximately equal to the size of the offset voltage, the polarity is opposite to the offset voltage, and then in the normal working stage the offset is eliminated. Auto-zeroing is classified as input offset storage (IOS) and output offset storage (OOS) based on the position of the capacitance in the preamplifier's input and output.

To mitigate the effect of capacitance mismatch, several calibrations have been explored. A classic self-calibrating technique is proposed in [17]. In the calibration phase, the voltage error caused by capacitance mismatch is firstly measured by an additional calibration digital-to-analog converter (DAC) and stored in a data register, and then used to correct the mismatch error of the capacitive digital-to-analog converter (CDAC) in the conversion phase. However, the implementation of this calibration requires an additional block circuit and a large area. A foreground digital calibration is proposed in [18,19], which considers low-bit capacitances as the ideal ones and uses them to estimate the weight of high-bit capacitances. However, the weight estimation errors of LSB capacitances will propagate exponentially to those of MSB ones. A background digital calibration technique based on dither is proposed in [20], which obtained two sets of digital output codes by stacking the offset of $+\Delta$ and $-\Delta$, respectively, in the sampling process and quantizing them twice. For linear systems, the disturbed signal can be eliminated without affecting the quantization of the input signal. However, an SAR ADC with capacitance mismatch is a nonlinear system, and its nonlinear part will have errors after quantization. Through this error value, the weight error of each capacitance can be obtained and the weight of each capacitance can be adjusted by the LMS algorithm until the error is zero. A double-conversion background calibration technique is proposed in [21], applied to a 20-bit 1-MS/s SAR ADC. This technique mainly converts each analog sample twice through a single SAR ADC and modulates the error between the two conversions. It is clear that with the rapid development of the technology, more and more calibration technologies are developing in the direction of digitalization.

This paper presents a 16-bit 1-MS/s SAR ADC. The segmented capacitance array is utilized to reduce the capacitance area and the mismatch caused by fractional capacitance is eliminated via high-bit sampling. To solve insufficient setting of high-bit capacitances, redundant bits are introduced to the capacitance array of the MSB segment. To minimize the comparator's input offset voltage, a four-stage preamplifier and a latch with the auto-zeroing technique are used. In order to reduce the accuracy degradation of the ADC due to capacitance mismatch, a digital foreground calibration technique based on low-bit weight is designed. The ADC is designed in 180 nm CMOS technology under a 3.3 V supply voltage.

This paper is organized as follows: the simulation results and comparisons are discussed in Section 2. Sections 3 and 4 describe the presented SAR ADC architecture and block circuit implementation, respectively. Finally, the conclusions are included in Section 5.

2. Simulation Results

The 16-bit SAR ADC has been designed in a 0.18 μm CMOS and its layout is shown in Figure 1; the area of the ADC core is 0.83 mm \times 1.28 mm. The layout of the timing part of the digital calibration algorithm is generated using a digital back-end layout routing tool and the active area of the layout of the digital calibration part is 0.21 mm \times 0.35 mm. Both the power supply and the reference voltage are 3.3 V. We assume that the circuit noise is smaller than other noise components in this paper. Figure 2 shows the effective number of bits (ENOB) of the ADC under 27 PVT conditions without capacitance mismatch at 476.56 kHz input frequency. The process corners are TT, SS and FF, with temperatures of -40°C , 40°C and 85°C and power supply voltages of 3 V, 3.3 V and 3.6 V, respectively. It can be seen that the ENOB of the ADC under all PVT conditions is greater than 15 bits, and the ADC features good robustness.

Figure 3 shows the post-simulated power spectrum density (PSD) of the ADC, which is driven by a 1 MS/s clock and a 475.56 kHz full-scale sine input signal. For comparison, simulation results both with and without digital calibration are presented. After calibration, large harmonic distortions are significantly suppressed, and the SAR ADC's signal-to-noise-distortion ratio (SNDR) and spurious-to-free dynamic range (SFDR) are improved from 76.68 dB and 82.83 dB to 95.61 dB and 104.96 dB, respectively. The core ADC consumes 5.4 mW, corresponding to an FoM of 175.3 dB. Table 1 shows the post-simulation results at different PVT conditions with and without calibration at 475.56 kHz input signal. Under the condition of SS 3.6 V -40°C , the ADC's ENOB is the lowest (14.98 bits) after calibration

and at other corners the ENOB is all greater than 15 bits after calibration, indicating that the calibration has good stability.

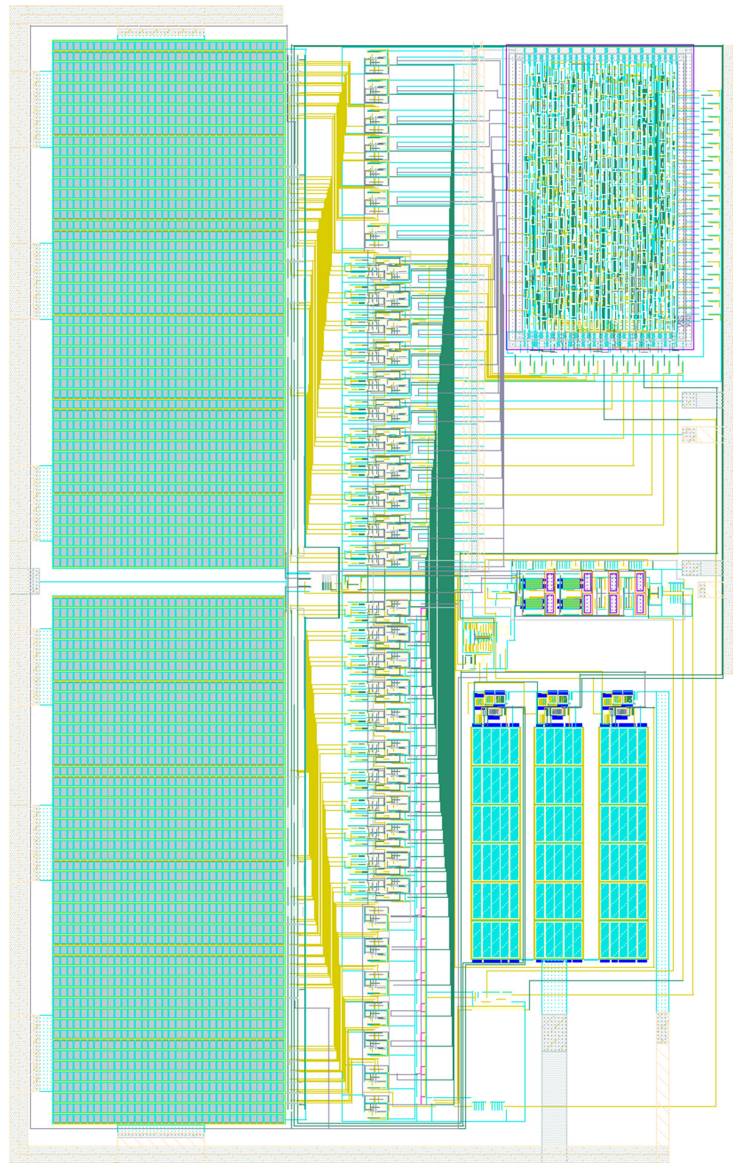


Figure 1. The layout of the presented SAR ADC.

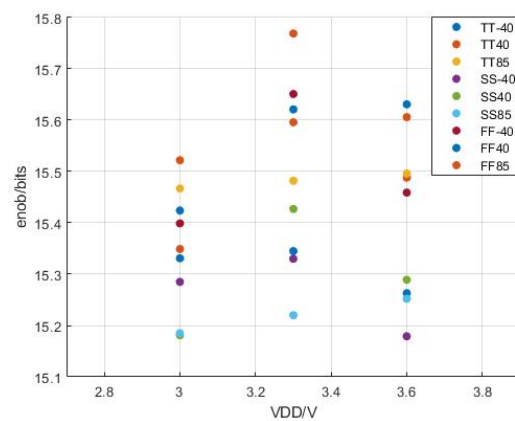


Figure 2. The ENOB of ADC under 27 PVT conditions without capacitance mismatch.

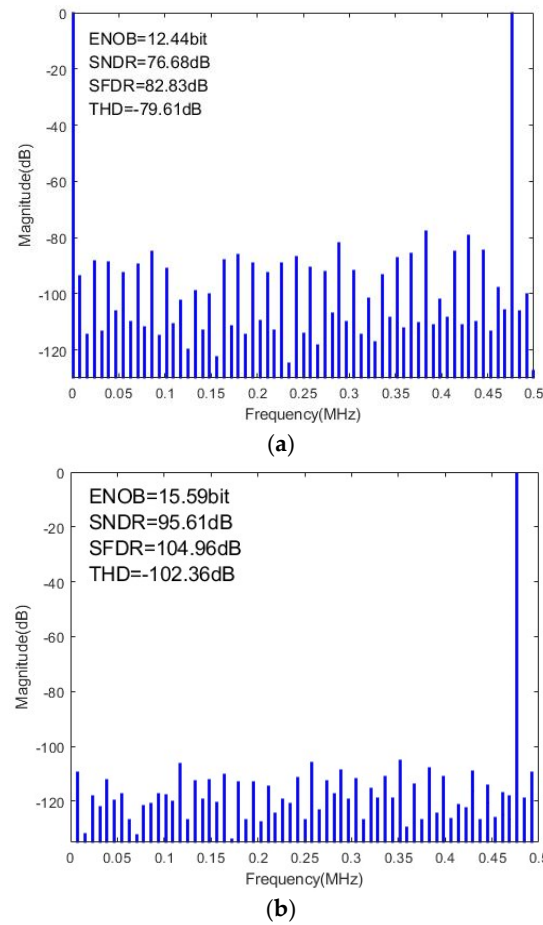


Figure 3. (a) Post-simulated SAR ADC PSD without digital calibration. (b) Post-simulated SAR ADC PSD with digital calibration.

Table 1. Post-simulation results under different PVT corners with and without calibration.

Corner	Supply Voltage (V)	Temperature (°C)	ENOB (bits)		SNDR (dB)		SFDR (dB)	
			with/without Calibration	with/without Calibration	with/without Calibration	with/without Calibration		
TT	3.3	40	15.50/12.50	95.06/77.01	105.00/83.49			
FF	3.3	85	15.11/12.46	92.73/76.76	100.97/83.35			
FF	3	−40	15.23/12.50	93.46/76.99	99.79/83.74			
SS	3.6	−40	14.98/12.56	91.97/77.40	99.99/84.60			
SS	3	85	15.42/12.40	94.62/76.44	105.36/83.05			

The power consumption breakdown of the SAR ADC is shown in Figure 4. The main power consumption is in the comparator, accounting for 77.7%, followed by the CDAC and sampling circuit, which consume 18.9% in total, and the digital logic circuit consumes 3.4%. The result of this design is added to Boris Murmann’s Schreier FoM vs. speed plot [22] for comparison, as shown in Figure 5. It shows that the designed 16-bit SAR ADC achieves good performance. Table 2 summarizes the performance of the presented SAR ADC and compares it with the state of the art. The results show that the proposed SAR ADC achieves competitive SNDR and SFDR after calibration. The ADC presented in [23] can operate at a higher sampling rate, but the proposed ADC has a higher resolution and consumes less power. Compared to the proposed ADC, the ADC in [4] features a similar resolution and sampling rate but it lacks the calibration circuit, which is implemented in an off-chip FPGA. Due to the use of a pipeline-SAR structure, the sampling rate of the ADCs presented in [24,25] is higher, but the proposed ADC has a higher resolution and SNDR.

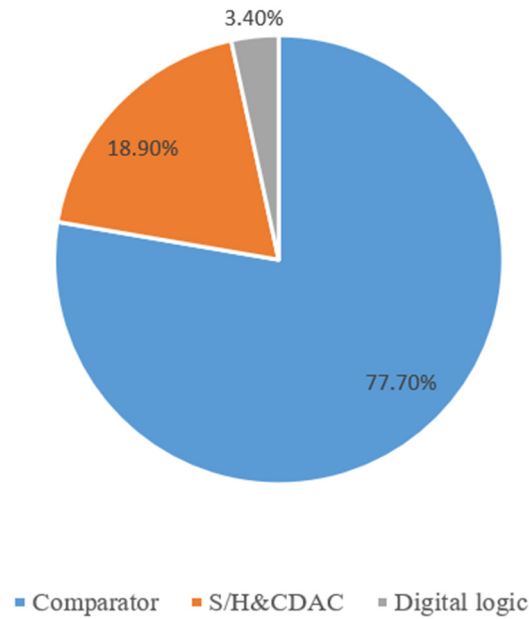


Figure 4. Power consumption breakdown of the SAR ADC.

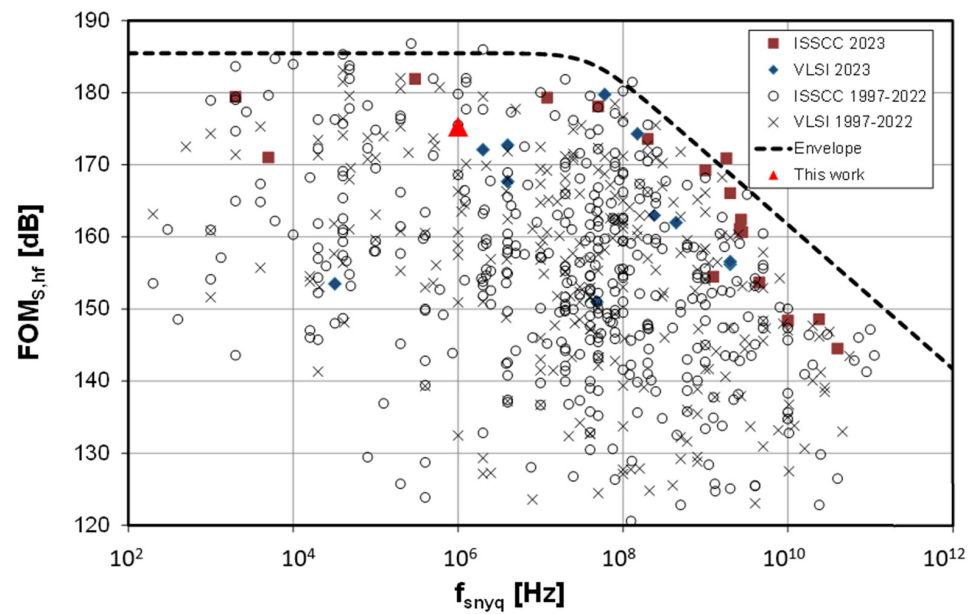


Figure 5. Boris Murmann’s Schreier FoM vs. speed plot with this design.

Table 2. Performance summary and comparison to state-of-the-art designs.

	This Work *	[23]	[26]	[4]	[24]	[25]	[27]
Type	SAR	SAR	Pipe SAR	SAR	Pipe SAR	Pipe SAR	BW-SAR
Resolution (bits)	16	16	18	16	14	15	16
Speed (MS/s)	1	16	5	1	75	60	1
Power (mW)	5.4	16.3	30.5	6.95	24.9	1.55	1.05
SNDR (dB)	95.61	78	99	91	70.8	76.9	83
SFDR (dB)	104.96	98	100	100	89.6	87.3	100
VDD (V)	3.3	3.3/1.2	5/1.8	1.2	1.8	1.1	1.8/3.3
Calibration	On chip	On chip	Off chip	Off chip	On chip	On chip	No
FoM (dB)	175.3	165	177.7	159.6	165.6	179.8	169.8
Process (nm)	180	55	180	55	65	65	180

* Post-simulation results. FoM = SNDR + 10 log(Fs/2/Power).

3. SAR ADC Architecture and Digital Calibration

3.1. SAR ADC Architecture

The simplified block diagram of the presented 16-bit 1-MS/s SAR ADC is shown in Figure 6, which consists of a pair of bootstrapped switches, a differential segmented CDAC with digital foreground calibration, a high-precision comparator with auto-zeroing, and SAR logic. Auto-zeroing is used to eliminate the offset voltage of the comparator, and the digital foreground calibration aims to minimize the performance degradation caused by CDAC capacitance mismatch.

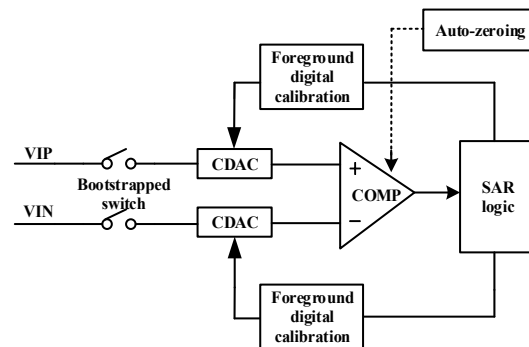


Figure 6. Architecture of the presented 16-bit 1 MS/s SAR ADC.

3.2. DAC Foreground Calibration

If no DAC calibration is applied, a unit capacitance of 600 fF and a total capacitance of 633 pF are required to guarantee 16-bit linearity. Such a large capacitance would result in a large chip area and a high power consumption to drive it. To overcome the design penalty, a differential DAC digital foreground calibration based on [18] is designed in this SAR ADC.

The capacitances in the LSB array are regarded as ideal capacitances and used as the calibration capacitance array ZDAC and to calibrate capacitances C_{6p} and C_{6n} . The calibration procedure is as follows: (1) The bottom plate of C_{6p} is connected to V_{ref} , the bottom of C_{6n} is connected to GND and those of all other capacitances are connected to the common-mode voltage (V_{cm}). The top plates of all capacitances are connected to V_{cm} . (2) C_{6p} and C_{6n} are switched to V_{cm} , and ZDAC is used to generate the digital code $D_{6,1}$. (3) The bottom plate of C_{6p} is switched to GND, and C_{6n} is switched to V_{ref} ; the operation is repeated in the second step and ZDAC is used to obtain the digital code $D_{6,0}$. The difference between these two codes is the estimated weight of C_{6p} and C_{6n} . The weight values of C_{6p} and C_{6n} are updated. (4) The new ZDAC capacitances are used to calibrate the next capacitances C_{7p} and C_{7n} ; the new ZDAC is now composed of $C_{0p}\sim C_{6p}$ and $C_{0n}\sim C_{6n}$, and so on, until the MSB capacitances C_{16p} and C_{16n} are calibrated, as shown in Figure 7. After the updated weight value of the MSB array capacitance is obtained, it is digitally processed with the output code in the normal conversion stage to reduce the influence of capacitance mismatch. In implementation, multiple measurements and averaging can be applied to reduce circuit noise and improve calibration accuracy.

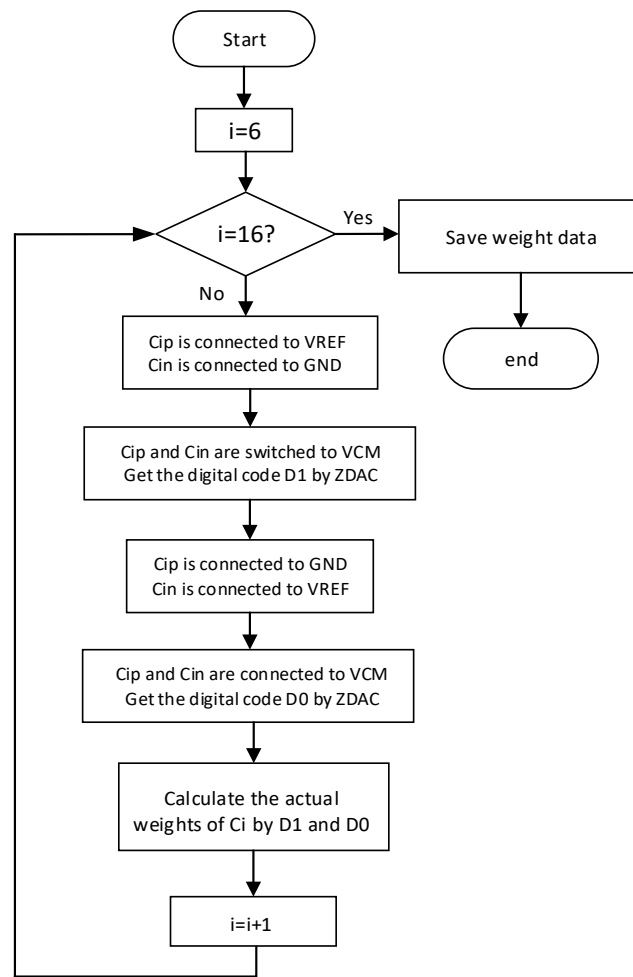


Figure 7. Foreground calibration procedure of the CDAC.

4. SAR ADC Circuit Implementation

4.1. Bootstrapped Switch

MOS switches introduce nonlinearity because their on-resistance will change with the input signal. In order to minimize the variation in switch on-resistance, the bootstrapped switch as shown in Figure 8 is adopted in this paper. CLK is the sampling clock, NCLK is the reverse signal of the sampling clock and an M_c transistor is used to act as the capacitance. In the holding stage, CLK is low and NCLK is high. Transistors NM5 and NM7 are on. The gate voltage of transistor NM1 is pulled to the ground, so NM1 is off, and the output voltage remains in the original state. The MOS capacitance M_c is charged to V_{DD} . In the sampling stage, CLK is high and NCLK is low. Transistors NM3 and PM3 are off and transistors NM2 and PM2 are on. As a result, the bottom plate of the MOS capacitance is connected to the source of NM1 through NM2, while the top plate of the MOS capacitance is connected to the gate of transistor NM1 through PM2. Due to the conservation of charge, the voltage difference between the top and bottom plates of the MOS capacitance remains V_{DD} . Therefore, the gate-to-source voltage of transistor NM1 remains at V_{DD} , so the gate voltage of the NM1 transistor is $V_{in} + V_{DD}$.

4.2. Capacitive DAC

For the traditional CDAC structure, the total capacitance increases exponentially as the number of bits increases. The use of a segmented capacitance array (SCA) with a bridge capacitance is a common solution for high-resolution SAR ADC, but the large number of bits in the LSB array increases with the nonlinearity of the circuit [28]. Based on the above trade-off, the MSB array and LSB array have 10-bit and 6-bit resolutions, respectively.

Moreover, the bridge capacitance of traditional segmented CDAC is usually a fractional capacitance, introducing capacitance mismatch and degrading ADC accuracy. In this paper, the two-segment capacitance array is designed and optimized, as shown in Figure 9. Because only capacitances of the high segment are used as sampling capacitances, the bridge capacitance (CB) can be designed as a unit capacitance. To solve the insufficient setting of high-bit capacitances, the binary-scaled recombination redundance algorithm is utilized in the MSB array [29,30]. Meanwhile, one-bit redundancy is assigned to the LSB array for CDAC calibration. Since the introduction of the redundant bit capacitance of the LSB array will cause the weight value of the LSB array relative to the MSB array to change, the bridge capacitance is changed to a value of twice the unit capacitance and the dummy capacitance of $C_{d1} = 15 C_u$ is introduced in the LSB array to ensure that the linear requirement of the ADC is met.

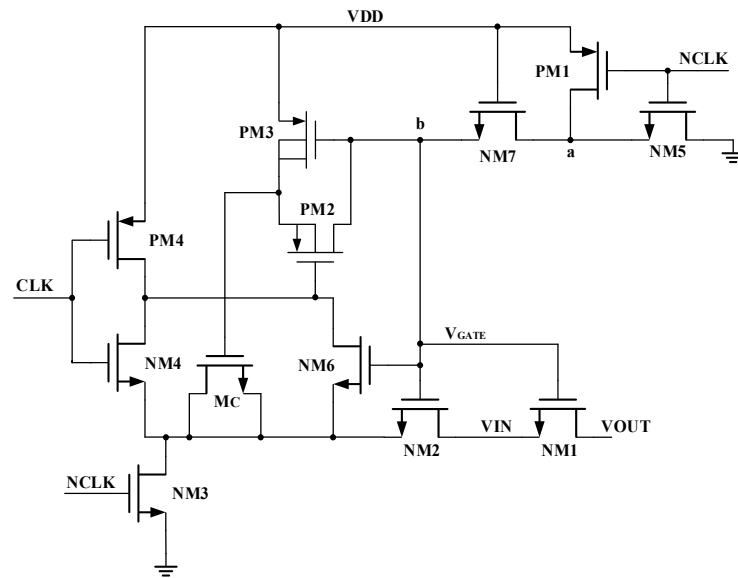


Figure 8. Schematics of the bootstrapped switch.

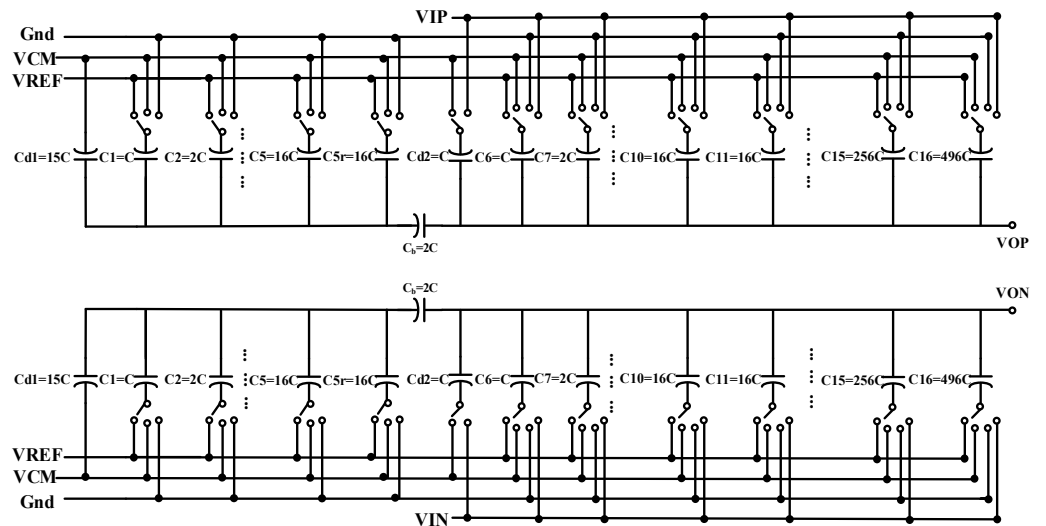


Figure 9. Schematics of the two-segment CDAC.

The value of the unit capacitance is mainly determined by two factors: sampling thermal noise and capacitance mismatch. The capacitance mismatch calibration technology is adopted in this paper, so the requirement of sampling thermal noise on unit capacitance can be mainly considered.

The kT/C noise power can be expressed as

$$\overline{V_{noise}^2} = \frac{kT}{C_S} \tag{1}$$

where k is the Boltzmann constant, T is the thermodynamic temperature and C_S is the total sampling capacitance.

Taking into account comparator noise, the sampling thermal noise of CDAC needs to be less than half of the quantization noise:

$$\overline{V_{noise}^2} < \frac{V_{quan,noise}^2}{2} = \frac{1}{2} \cdot \frac{LSB^2}{12} \tag{2}$$

To maintain the design margin, the value of unit capacitance is set as 30 fF.

4.3. Comparator

The structure of the comparator combined with the preamplifier and latch can take into account the speed and accuracy, so this structure is used as the comparator in this paper. The strong-arm latch is used in this paper, as shown in Figure 10. When CLK is high, transistor PM0 is off, and transistors NM1–NM4 are on, so Dn, Dp, Von and Vop are pulled to the GND, and the latch is in a reset state. When CLK is low, transistor PM0 is on and transistors NM1–NM4 are off. Von and Vop will be charged at different speeds due to different input voltage signals. If VIP is greater than VIN, the Vop will be charged faster. When the voltage of Vop and Von rises to the threshold voltage, transistors NM5 and NM6 will be switched on, so transistors PM3, PM4, NM5 and NM6 form positive feedback. Due to the faster charging speed of Vop, transistor PM3 will be turned off, and Von will not rise but fall to GND. Vop continues to rise to VDD. The output differential voltage of the latch can be expressed as

$$\Delta V = \Delta V_0 e^{\frac{t}{\tau}} \tag{3}$$

where τ is equal to gm/C . It can be seen from (3) that the differential output voltage of the latch increases exponentially, so in the actual working process, the whole process time is very short and can be completed in ns or even ps.

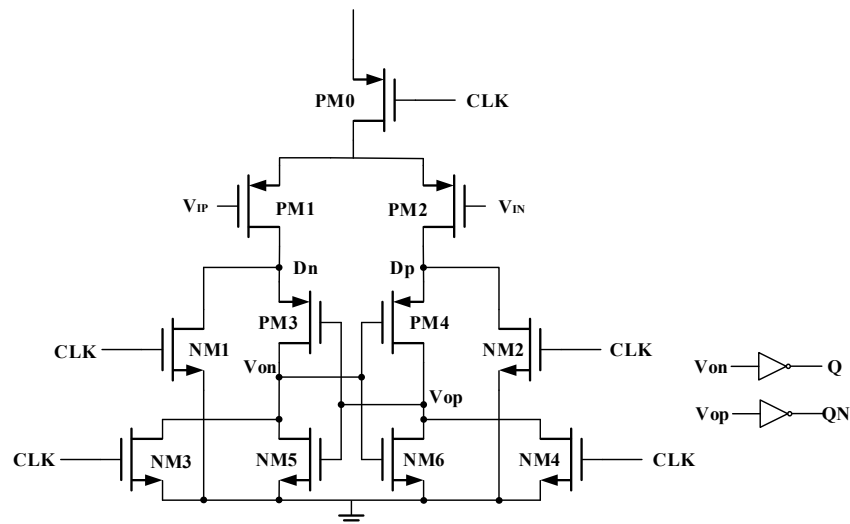


Figure 10. Schematics of the strong-arm latch.

The offset voltage of the strong-arm latch is simulated 200 times by Monte Carlo, and the simulation results are shown in Figure 11. The simulation method is as follows: One end of the comparator inputs V_{CM} and the other end inputs a ramp signal from $(V_{CM} - 0.05)$ V to $(V_{CM} + 0.05)$ V that slowly changes in a small step within the voltage range, observing

the output end of the comparator. The voltage difference of the input end when the low level jumps to the high level is the input offset voltage of the comparator. It can be seen that the standard deviation of the offset voltage of the latch is 4.55 mV, so its offset voltage is 13.65 mV. The gain of the preamplifier needs to be high enough to reduce the equivalent input offset voltage of the latch.

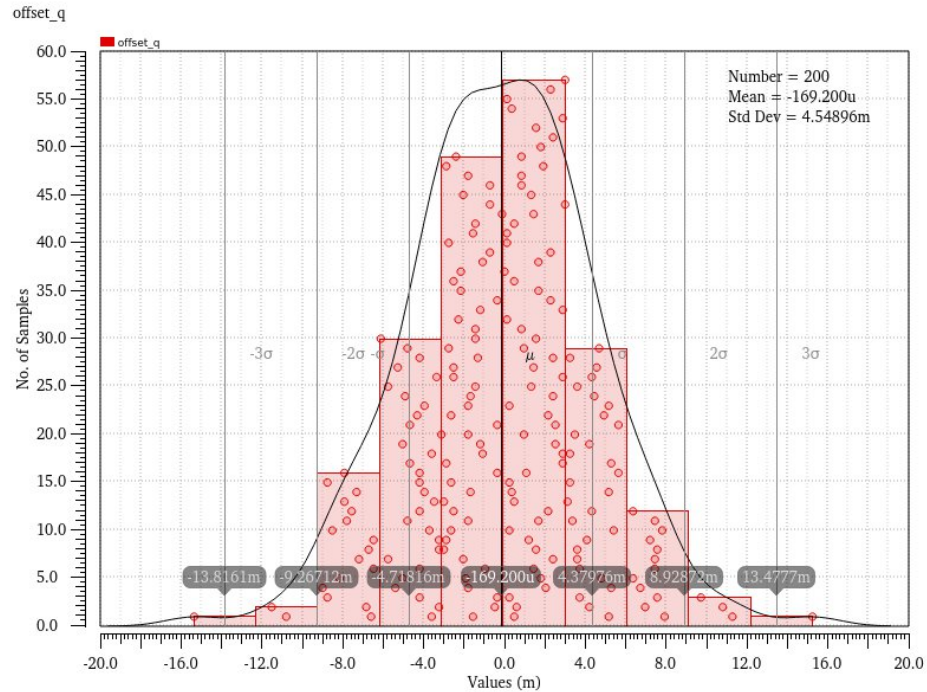


Figure 11. Monte-Carlo simulation of the strong-arm latch offset.

However, as the output offset storage is DC-coupled, the common-mode input voltage is limited. If the gain of the single-stage preamplifier is too large, the voltage of the capacitance may become saturated. To meet this contradictory demand, the comparator’s structure adopts a combination of a four-stage cascaded preamplifier and a strong-arm latch, as shown in Figure 12. Each preamplifier employs output offset cancellation to further reduce the offset voltage. Taking the first stage preamplifier as an example, its working process is divided into two stages: storage offset voltage stage and normal working stage. In the storage offset voltage stage, the switch S_0 is off, and switches CK and CK1 are on. The relationship between the input and output of the preamplifier can be expressed as

$$\begin{cases} V_X = V_Y = V_{CM} \\ V_A - V_B = -A_0 V_{OS} \end{cases} \quad (4)$$

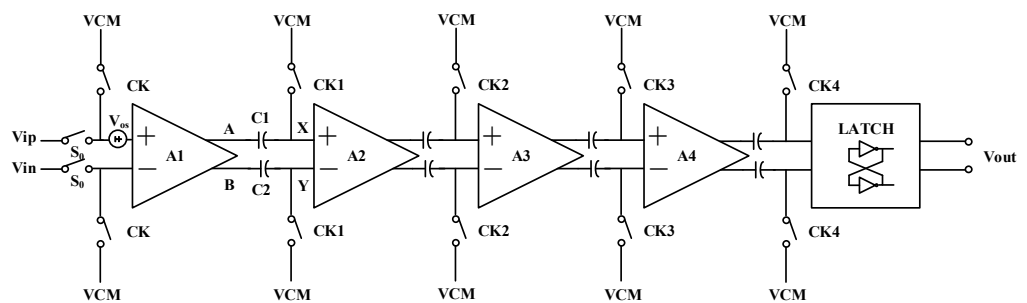


Figure 12. Structure of the comparator with auto-zeroing.

Charges Q_1 and Q_2 stored on capacitances C_1 and C_2 ($C_1 = C_2 = C$) are

$$\begin{cases} Q_1 = (V_A - V_{CM}) \cdot C \\ Q_2 = (V_B - V_{CM}) \cdot C \end{cases} \quad (5)$$

In the working stage, switch S_0 is on, and switches CK and CK_1 are off. The relationship between the input and output of the preamplifier can be expressed as

$$V_{A'} - V_{B'} = -A_0(V_{ip} - V_{in} + V_{OS}) \quad (6)$$

Charges Q_1 and Q_2 on capacitors C_1 and C_2 are

$$\begin{cases} Q_1' = (V_{A'} - V_X) \cdot C \\ Q_2' = (V_{B'} - V_Y) \cdot C \end{cases} \quad (7)$$

According to the conservation of charge, the differential output voltage is

$$V_X - V_Y = V_{A'} - V_{B'} - (V_A - V_B) = -A_0(V_{ip} - V_{in}) \quad (8)$$

It can be seen that the offset voltage is completely eliminated by the stored voltage.

In order to eliminate the charge injection effect caused by switches CK_1 , CK_2 , CK_3 and CK_4 when they are turned off, the switches should be turned off in sequence, as shown in Figure 13, so that the charge injection error generated by the previous switch can be stored on the capacitance and can be eliminated in the normal working stage. Since the comparator is in an idle state during the sampling stage, the offset voltage calibration stage of the comparator and the sampling stage can be combined; that is, the sampling clock not only controls the ADC for sampling but controls the comparator for offset calibration as well.

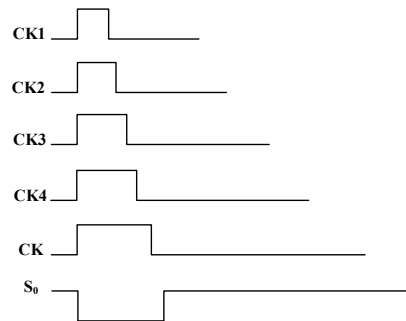


Figure 13. Timing diagram of the switches.

Figure 14 shows the Monte Carlo simulation result of the designed comparator; the standard deviation of the comparator offset voltage is as low as 4 μ V, which meets the design requirements of the 16-bit SAR ADC.

4.4. SAR Logic

The clock generation circuit of this design is shown in Figure 15. GT is a clock control signal, which avoids additional power consumption when the comparator does not generate a clock signal after one conversion is completed. When GT is low, the output signal NCK is low and CKC is high, the comparator is in the reset state, and the comparator outputs Q and QN are high. If GT is high, NCK becomes high, CKC becomes low and the comparator is in operation. After comparison, the levels of Q and QN are opposite, driving NCK down and the comparator into the reset phase. The above procedure is repeated in a cycle to produce an asynchronous clock CKC with alternating levels. The asynchronous clock frequency may vary in different process, voltage and temperature (PVT) conditions. If the frequency is too slow, the entire conversion process may not be completed, and if the

frequency is too fast, the DAC may not be fully established, resulting in a comparison error. In this paper, a delay module is used to adjust the asynchronous clock frequency flexibly to ensure that the SAR ADC can work normally under different PVT conditions. The delay module is based on the inverter with adjustable bias, and the discharge current of NMOS in the logic gate is controlled by the external bias current source so as to control the logic delay. Compared with the digital code control, the analog mode adjustment through the bias current is more accurate and the introduction of a long delay chain can be avoided.

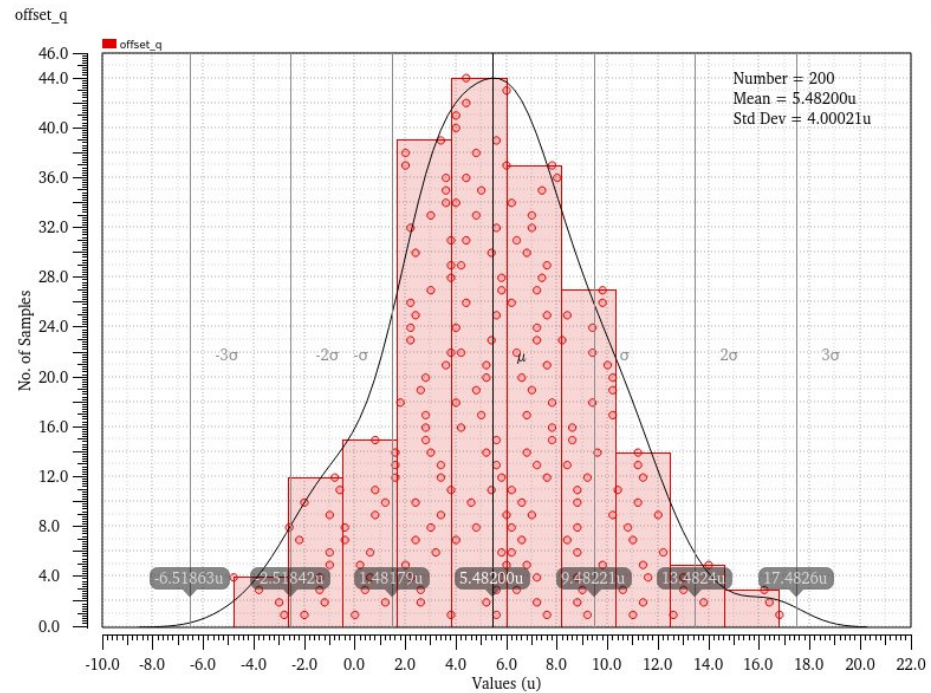


Figure 14. Monte-Carlo simulation of the comparator offset.

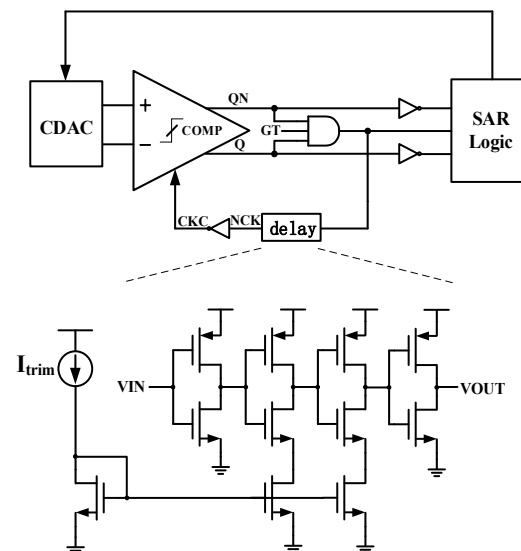


Figure 15. Schematics of the asynchronous clock generation.

5. Conclusions

This paper has presented a power-efficient 16-bit 1 MS/s SAR ADC in 180 nm CMOS, with a high-precision comparator and a DAC digital foreground calibration. Both a four-stage pre-amplifier and an auto-zeroing technique are applied to achieve 12 μ V comparator

input offset. The calibration based on low-bit weight improves the ADC's SNDR and SFDR from 72.56 dB and 78.64 dB to 93.21 dB and 105.1 dB, respectively. The power consumption of the core ADC is 5.4 mW, corresponding to an excellent Schreier figure of merit (FoM) of 175.3 dB.

Author Contributions: Research methodology, X.H.; circuit design, X.H.; calibration algorithm design, W.Q.; layout drawing, X.H.; writing—original draft preparation, X.H.; supervision, X.X. and H.F. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The original contributions presented in this study are included in the article material. The data presented in this study are available in this paper.

Conflicts of Interest: The authors declare no conflicts of interest.

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