Journal of
Low Power Electronics and Applications

MDPI

Article

0.35 V Subthreshold Bulk-Driven CMOS Second-Generation Current Conveyor

Muhammad Omer Shah, Manfredi Caruso and Salvatore Pennisi *

DIEEI (Dipartimento di Ingegneria Elettrica Elettronica e Informatica), University of Catania, 95125 Catania, Italy; muhammad.shah@phd.unict.it (M.O.S.); manfredicaruso1@gmail.com (M.C.)
* Correspondence: salvatore.pennisi@unict.it; Tel.: +39-095-7382318

Abstract: This study describes a high-performance second-generation Current Conveyor (CCII) operating at 0.35 V and achieving rail-to-rail operation at the Y terminal and class AB current drive at the X and Z terminals. The solution utilizes a low-voltage subthreshold bulk-driven CMOS OTA that was experimentally developed earlier, making systematic use of body terminals to improve small-signal and large-signal performance. The circuit has a high open-loop voltage gain and uses cascoded current mirror topologies, resulting in precise voltage and current transfer with bandwidths of 1.33 MHz and 2.13 MHz, respectively. The CCII offers a linear current drive up to 2.5 µA while consuming a total quiescent current of 2.86 µA (758 nA in the output branches), displaying one the highest figures of merit in terms of current utilization for sub 1 V solutions.

Keywords: bulk-driven; CMOS analog integrated circuits; low-voltage; operational transconductance amplifier

Citation: Shah, M.O.; Caruso, M.; Pennisi, S. 0.35 V Subthreshold Bulk-Driven CMOS Second-Generation Current Conveyor. *J. Low Power Electron. Appl.* **2024**, *14*, 36. https://doi.org/10.3390/jlpea14030036

Academic Editor: Orazio Aiello

Received: 5 June 2024
Revised: 4 July 2024
Accepted: 5 July 2024
Published: 7 July 2024

1. Introduction

Bulk-driven (BD) techniques have gained significant attention among circuit designers in recent years [1–5] because they eliminate the threshold voltage limitation when driving MOS field-effect transistor (MOSFET) devices via their bulk (body) terminals. The effectiveness of the BD approach has been particularly evident in implementing Operational Transconductance Amplifiers (OTAs) that function with supply voltages from 400 mV down to 250 mV [6–19]. This approach allows for the widest common-mode input range, nearly providing rail-to-rail limits. Furthermore, it often results in quiescent current consumption of only a few microamperes or less, which is achieved by properly biasing MOSFETs in their sub-threshold region. The above properties meet the rising demand for ultra-low-voltage, ultra-low-power integrated circuits (ICs) in portable, wearable, and implantable electronics [20–23] but also in the Internet of Things and in the automotive field, which require the development of new circuit topologies and design methodologies aimed at preserving the performance characteristics of established CMOS solutions while enhancing input/output voltage swing and reducing the necessary supply voltage, particularly in the analog domain.

In this framework, the second-generation Current Conveyor, CCII, is a versatile three-terminal (namely, Y, X, and Z terminals) block that provides distinctive performance as it brings together voltage-mode processing characteristics (the voltage follower action between the Y and X terminals) with current-mode ones (the current follower action between X and Z terminals). CCIIs have indeed been used for active filter implementation and are found to be building blocks of transimpedance and current feedback operational amplifiers, voltage, and current operational amplifiers [24–27].

A comprehensive review of the recent literature reveals that numerous publications explore novel CCII implementations with low-voltage and low-power capabilities that also exploit body-driven and subthreshold techniques to attain rail-to-rail performance [28–33].

In this paper, we present an alternative high-accuracy body-driven CCII solution supplied from 0.35 V and with a 2.86 µA total quiescent current (758 nA in the two output branches). Among the most relevant performances, thanks to the high open-loop gain and exploitation of cascoded current mirror topologies, the circuit provides accurate voltage (Y to X) and current (X to Z) transfers with a −3 dB frequency of 1.33 MHz and 2.13 MHz, respectively, and with an efficient current drive capability of around 2.5 µA.

Compared to other sub-1V solutions, the proposed design achieves superior current drive efficiency. This metric, defined as the ratio of maximum output current to total quiescent current, is particularly important in targeted battery-operated or even battery-less applications.

The rest of the paper is organized as follows. The presented solution is described in Section 2, where particular focus is directed towards elucidating the primary novel design solutions and fundamental design equations. Section 3 delves into the simulations conducted to assess the proposed solution, while in Section 4 the paper concludes with the authors presenting their findings and drawing conclusions.

2. The Proposed Solution

The proposed solution is depicted in Figure 1 and was derived from the OTA configuration presented by one of the authors in a recently published work that employs MOSFETs in the subthreshold region and strategically leverages the body terminals to enhance small-signal and large-signal performance [19].

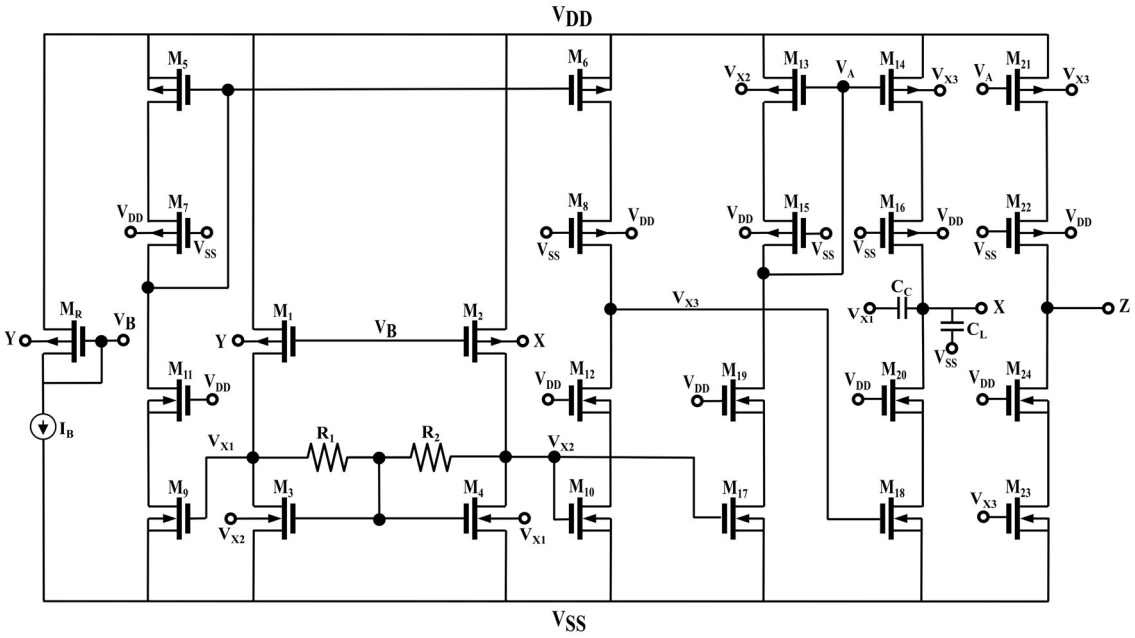

Figure 1. Schematic diagram of the proposed BD CCII.

Our proposed current-conveyor circuit introduces several key modifications compared to the design presented in [19]. Firstly, we introduce a current branch replicating current at terminal X in terminal Z. Secondly, we remove the Slew-Rate Enhancer section of [19] to eliminate nonlinearities inherent to this highly nonlinear circuit. Finally, we employ extensive transistor cascoding to achieve superior DC and AC matching, while also optimizing loop gain and the equivalent resistance at terminal Z. Moreover, while reference [19] focuses on off-chip, high-drive applications, our CCII is specifically designed for on-chip, low-load capacitance applications. This necessitates a distinct design approach to optimize for these contrasting use cases.

The solution is based on local positive feedback for improved input transconductance which is achieved through the bodies of M_3–M_4, and dynamic threshold voltage control to

boost the current drive capability is implemented with the bodies of M_{13}–M_{14}. It is to be noted that a trade-off among simplicity, current transfer accuracy, linearity, high impedance, and voltage compliance is achieved through supply-biased cascode structures. In other words, all the n-channel (p-channel) cascode transistors have their gates connected to V_{DD} (V_{SS}).

Specifically, the solution is made up of four sections: the BD rail-to-rail input stage (M_1–M_4, R_1–R_2), the second gain stage with a differential-to-single-ended function (M_5–M_{12}) the third noninverting gain stage (M_{13}–M_{20}), and a replica of the output branch (M_{21}–M_{24}) which, working in class AB, mirrors the current from terminal X into terminal Z.

The input stage utilizes transistors M_1 and M_2, forming a minimum-supply tail-less body-driven pair without a dedicated current source transistor. A constant current (I_B) establishes the quiescent current through this pair via the diode-connected transistor M_R (with the body connected to terminal Y). The actual current flowing through M1 and M2 is determined by the mirror ratio $(W/L)_{1,2}/(W/L)_R$, where W and L represent the width and length of the transistors. Due to the virtual short at the input of the OTA ($V_X = V_Y$), these transistors share the same body voltage at DC, resulting in the same threshold voltage.

The active load for the input stage comprises transistors M_3 and M_4, with negative feedback resistors R_1 and R_2 playing a crucial role in amplifying differential signals. This load configuration allows the inherently pseudo-differential pair (M_1 and M_2) to effectively handle differential inputs. Local positive feedback is implemented by connecting the body of M_3 to the drain of M_4 and vice versa, enhancing the overall transconductance of the input stage.

The second stage, designed for high output impedance and for converting differential to single-ended output, consists of transistors M_5–M_{12}. The quiescent current in this stage mirrors the current in the first stage through M_9 and M_{10} because M_3 and M_4 act as diode-connected devices at DC, ensuring no current flows through R_1 and R_2 at DC.

Given that $V_{BS3,4} = V_{GS3,4}$ while $V_{BS9,10} = 0$, the current mirror gain is reduced compared to a conventional current mirror, where this factor equals 1 [19].

The third gain stage, consisting of common-source transistor M_{17} with cascode M_{19} and active loads M_{13}–M_{16} and M_{18}, M_{20}, regulates the X branch's quiescent current through the current mirror gains of $M_{3,4}$ to M_{17}, and of M_{13} to M_{14}. Notably, the pull-down i_X current from M_{18} can exceed the quiescent value, like the pull-up i_X current from M_{14}, although to a lesser extent. In fact, both M_{14} and M_{18} operate in class AB but the positive-going output step responds slower than the negative-going step due to the limited variation of the gate voltage of M_{17} compared to the gate voltage of M_{18}. To address this asymmetry, the gain in the current mirror formed by transistors M_{13}–M_{14} is dynamically adjusted based on the required current level. This is achieved by connecting the body of M_{13} to the drain of M_4 and the body of M_{14} to the drain of M_8 (M_{12}), as shown in Figure 1. This configuration leverages the dependence of the threshold voltage of M_{13} and M_{14} on variations in V_{X2} and V_{X3}, boosting the current mirror gain when the output stage supplies current, as explained in [19].

The output of this stage is tied to the inverting input of the input pair M_1–M_2 providing unity gain configuration through high-gain negative feedback and hence ensuring virtual short between voltages at nodes Y and X.

The current flowing in terminal X through M_{14} and M_{18} is mirrored to terminal Z thanks to the class-AB current mirror made up of transistors M_{21}–M_{24} replicating the branch formed by M_{14}, M_{16}, M_{18}, and M_{20}.

Capacitor C_c provides frequency compensation. Transistor dimensions and other design parameters are summarized in Tables 1 and 2.

Table 1. Transistor dimensions of circuit in Figure 1.

Device	W/L (µm/µm)
M_R, M_1, M_2	34/0.5
M_3, M_4	8/1
M_5, M_6	160/1
M_7, M_8	9/0.5
M_{11}, M_{12}	2/0.5
M_9, M_{10}	32/1
M_{13}	50/0.5
M_{15}	5/0.5
M_{17}	16/1
M_{18}	1.5/0.5
M_{14}, M_{21}	200/0.5
M_{16}, M_{22}	20/0.5
M_{18}, M_{23}	60/2
M_{20}, M_{24}	6/1

Table 2. Other design parameters of circuit in Figure 1.

Param	Value
V_{DD}–V_{SS}	0.35 V
I_B	200 nA
R_1, R_2	250 kΩ
C_C	200 fF
C_L	1 pF

Small-Signal Analysis and Noise

Owing to the negative feedback, the CCII voltage transfer from terminal Y to X is as follows:

$$\frac{V_X}{V_Y} = \frac{1}{1+\frac{1}{T(s)}} \approx \frac{1}{1+\frac{1}{T(0)}} \frac{1}{1+\frac{s}{\omega_{GBW}}} \quad (1)$$

where $T(0)$ is the loop gain $G_{mEQ} r_{oX3} g_{m17} r_{oX}$, in which r_{oX3} and r_{oX} are equivalent resistances at the drain of M_8, M_{12} and M_{16}, M_{20}, respectively, and G_{mEQ} is given by $g_{mb1,2}/(1 - g_{mb3,4} r_{X1,2})$, due to the local positive feedback operated by the bodies of M_3 and M_4, and as detailed in [19]. As usual, ω_{GBW} is given by G_{mEQ}/C_c.

It is seen that the DC value of (1) tends to be 1 for high values of $T(0)$.

The equivalent (closed loop) small signal resistance at terminal X is approximately given by the following equation:

$$r_X \approx \frac{r_{oX}}{T(0)} = \frac{g_{m20} r_{o18} r_{o20} \,//\, g_{m16} r_{o14} r_{016}}{T(0)} \quad (2)$$

and the small signal equivalent resistance at terminal Z is simply as follows:

$$r_Z = g_{m24} r_{o23} r_{024} \,//\, g_{m22} r_{o21} r_{022} \quad (3)$$

The CCII noise performance can be modeled by considering the equivalent input noise voltage of the voltage buffer (v_{nY}, in series to terminal Y) and the equivalent input noise current of the current buffer (i_{nX}, in parallel to terminal X), as shown in Figure 2 [34].

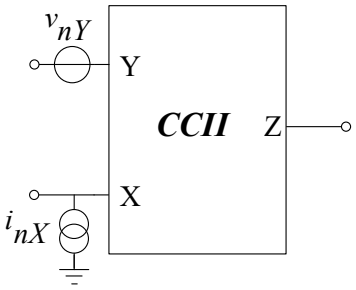

Figure 2. CCII with noise sources.

The equivalent input-referred noise voltage spectral density of the CCII, $\overline{v_{nY}^2}$, accounts for the contribution of transistors M_1 and M_2, that of transistors M_3 and M_4, and of resistors $R_{1,2}$. It can be approximated as in Equation (4), considering only white noise for simplicity [9].

$$\begin{aligned}\overline{v_{nY}^2} &\approx 2\overline{v_{n1,2}^2}\left(\frac{g_{m1,2}}{g_{mb1,2}}\right)^2 + 2\overline{v_{n3,4}^2}\left(\frac{g_{m3,4}}{g_{mb1,2}}\right)^2 + \overline{v_{nR1,2_Y}^2} \\ &= 2\tfrac{2}{3}4kT\frac{1}{g_{mb1,2}}\left(\frac{g_{m1,2}}{g_{mb1,2}} + \frac{g_{m3,4}}{g_{mb1,2}}\right)\Delta f \\ &+4kTR_{1,2}\left(\frac{1}{g_{mb1,2}r_{o1}}\right)^2\left[1+\left(1+\frac{2r_{o1}}{R_{1,2}}\right)^2\right]\Delta f\end{aligned} \tag{4}$$

where $\overline{v_{ni}^2}$ is the gate-referred noise voltage spectral density of the i-th transistor, $\overline{v_{nR1,2Y}^2}$ is the input-referred noise contribution of the resistors R_1 and R_2, r_{o1} is the output resistance of $M_{1,}$ and k and T are the Boltzmann's constant and the absolute temperature.

In the above expression, noise from M_R is neglected since it is seen as a common-mode signal and is rejected. Additionally, the noise from the $R_{1,2}$ results is considered to be negligible by the following equation:

$$(g_{m1,2}+g_{m3,4})r_{o1} \gg \frac{3}{4}\frac{R}{r_{o1}}\left[1+\left(1+\frac{2r_{o1}}{R}\right)^2\right] \tag{5}$$

Unfortunately, (5) is not fulfilled in our design.

The noise current generator, i_{nX}, is equal to the output noise at terminal Z when terminal X is floating. The mean-square value can easily be calculated as follows:

$$\overline{i_{nX}^2} \approx g_{m14}^2\overline{v_{n14}^2} + g_{m21}^2\overline{v_{n21}^2} + g_{m18}^2\overline{v_{n18}^2} + g_{m23}^2\overline{v_{n23}^2} \tag{6}$$

3. Simulation Results

The circuit was designed and simulated using a standard 65 nm CMOS technology supplied by TSMC and accessed through EUROPRACTICE. The supply voltage is 350 mV and the total current consumption is 2.86 µA, with the current in the X and Z output branches equal to 758 nA each.

Figure 3a,b shows the Bode plots, magnitude, and phase, of the open loop gain from the body of M_2 and the drain of M_{16} and M_{20}, with a load capacitance of 1 pF. The DC gain is around 70 dB and the unity gain bandwidth is 600 kHz, with more than 70° phase margin.

The Bode plots of the (closed-loop) voltage transfer (from Y to X) are shown in Figure 4a,b. The low-frequency gain is −4.096 mdB. Montecarlo simulations on 1000 iterations show 68 mdB of standard deviation. The −3 dB frequency is 1.33 MHz.

Additional simulations indicate little changes in the low-frequency gain with different DC levels of the voltage at the Y terminal in the range [20 mV–350 mV]. The same marginal variations are found for different operating temperatures in the range [−40 °C–120 °C].

The Bode plots of the current transfer (from X to Z) are shown in Figure 5a,b. The low-frequency gain is −2.087 mdB. Montecarlo simulations on 1000 iterations show 72.5 mdB of standard deviation. The −3 dB frequency is 2.13 MHz. A 14.1 dB peak is observed at 1.38 MHz.

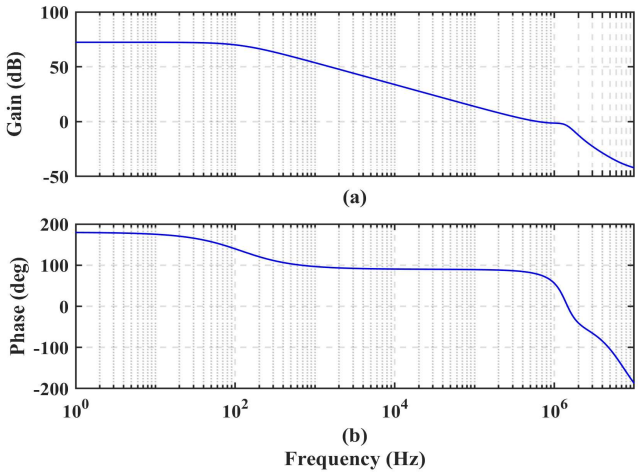

Figure 3. Gain (**a**) and phase (**b**) of open loop Y to X voltage transfer.

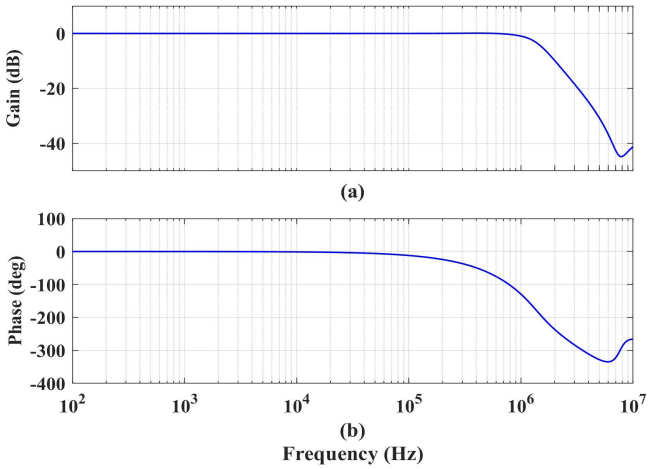

Figure 4. Magnitude (**a**) and phase (**b**) of voltage transfer (Y to X) versus frequency.

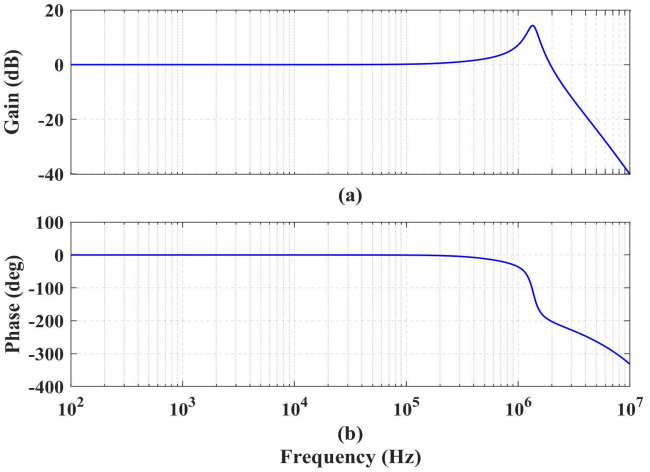

Figure 5. Magnitude (**a**) and phase (**b**) of current transfer (X to Z) versus frequency.

The magnitude of the impedance at terminal Y versus the frequency is shown in Figure 6. It decreases with the frequency while maintaining a substantial high value. For example, it is 118 GΩ at 10 Hz, 150 MΩ at 10 kHz, and 1.6 MΩ at 1 MHz. The parasitic capacitance at this terminal is evaluated to be 96.5 fF.

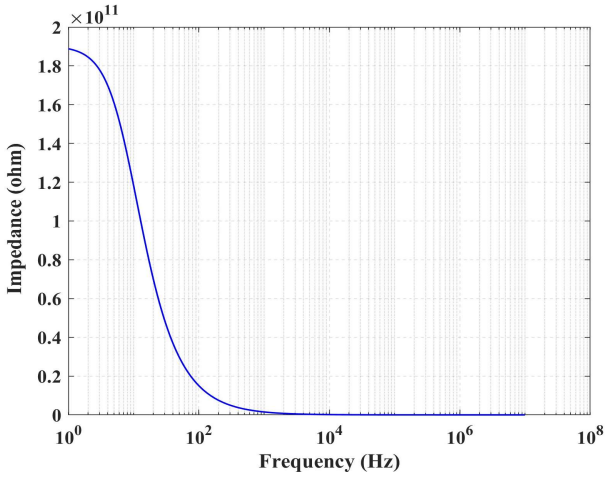

Figure 6. Magnitude of impedance at node Y versus frequency.

Figure 7 shows the input current at terminal Y as a function of V_Y. Under a 175 mV V_Y, the input current is 378.9 fA (with 189 fA flowing into each bulk of M_R and M_1). The maximum input current, for V_Y equal to 0, is 26 pA.

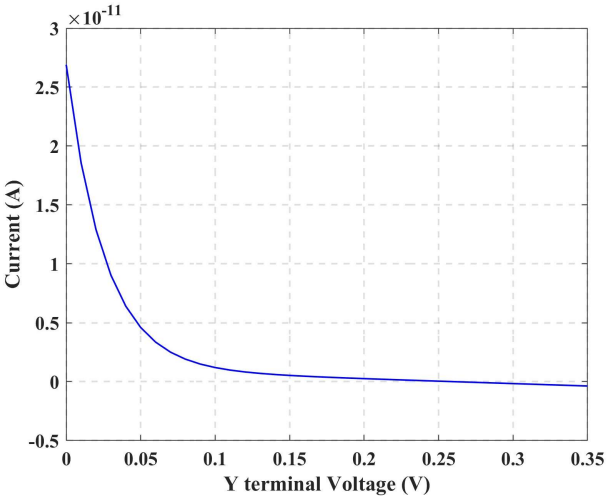

Figure 7. Leakage current at terminal Y versus V_Y.

The magnitude of the impedance at terminal X versus frequency is shown in Figure 8. The low-frequency impedance is 1.8 kΩ. The inductive behavior is apparent because of the peaking of around 520 kΩ at around 1.5 MHz. The magnitude of the impedance at terminal Z versus frequency is shown in Figure 9, and the low-frequency value is 7.46 MΩ.

The DC transfer characteristic of the voltage transfer V_X versus V_Y and of the current transfer I_Z versus I_X are illustrated in Figures 10 and 11, respectively. The rail-to-rail input (Y) and output (X) voltage ranges are apparent from Figure 10. Figure 11 shows that the linear current range is around ±2.5 µA (the quiescent current in the two branches with nodes X and Z is around 758 nA each). The systematic offset current at terminal Z is 1.1 pA.

The Total Harmonic Distortion (THD) of the voltage at terminal X for different input sinusoidal amplitudes and frequencies is shown in Figure 12. It shows that the THD at 1 kHz and 10 kHz equals 1% at about 340 mV_{p-p} and 305 mV_{p-p} input, respectively. The THD of the current at terminal Z (tied to a voltage equal to $V_{DD}/2$) for different input sinusoidal amplitudes and frequencies is shown in Figure 13. It shows that the THD at 1 kHz and 10 kHz equals 1% at about 2.8 µA and 2.7 µA input, respectively.

As discussed in the previous section, two equivalent noise sources are necessary to characterize a CCII. The equivalent noise voltage generator (at terminal Y) and the

equivalent noise current generator (at terminal X) spectral densities are plotted in Figure 14a and Figure 14b, respectively. White noise levels are, respectively, 849 $\frac{nV}{\sqrt{Hz}}$ and 943 $\frac{fA}{\sqrt{Hz}}$. In agreement with (5) and (7), the noise voltage main contributions are due to $R_{1,2}$ (44%), $M_{1,2}$ (27%), and $M_{3,4}$ (16%). The noise current main contributions are due to M_{14}, M_{21}, M_{18}, and M_{23}, giving more than 50% of the total.

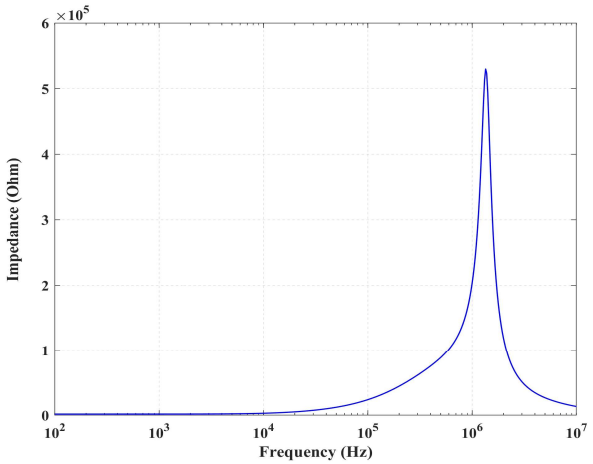

Figure 8. Magnitude of impedance at node X versus frequency.

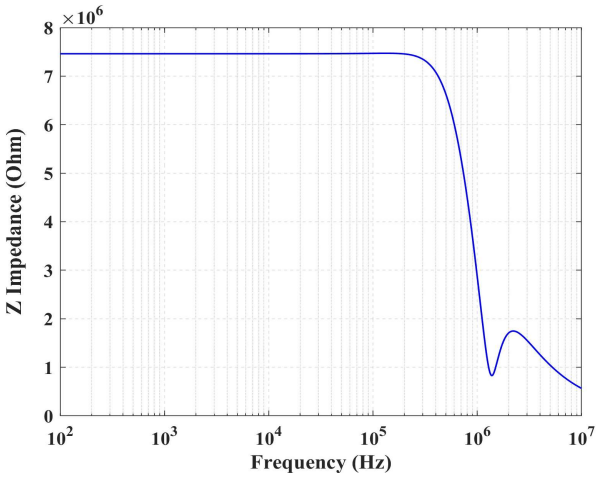

Figure 9. Magnitude of impedance at node Z versus frequency.

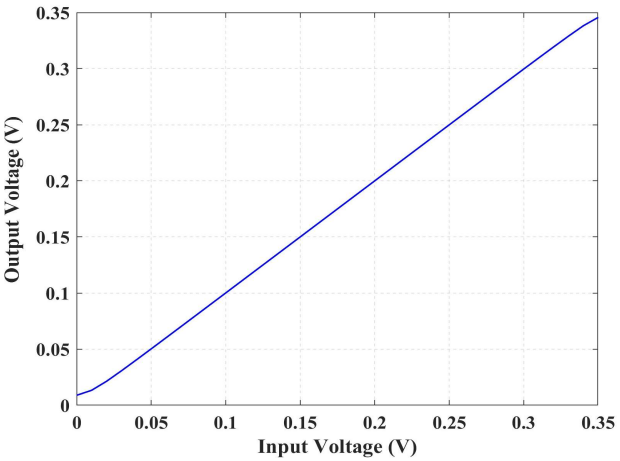

Figure 10. DC voltage transfer characteristic, V_X versus V_Y.

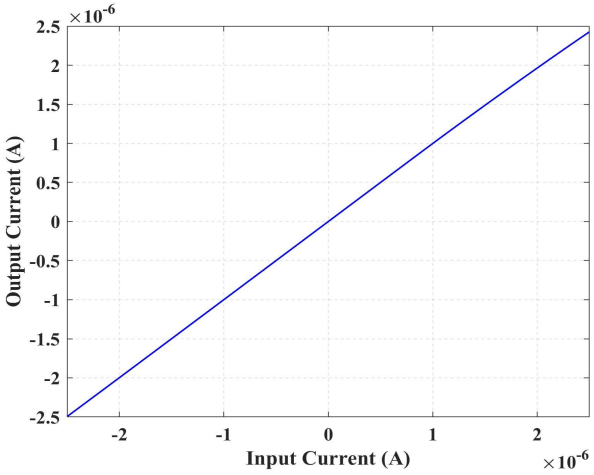

Figure 11. DC current transfer characteristic, I_Z versus I_X.

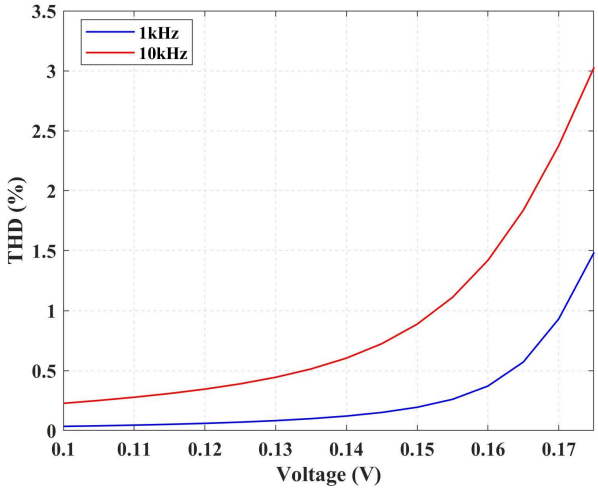

Figure 12. THD of voltage at terminal X versus magnitude of applied input voltage at Y.

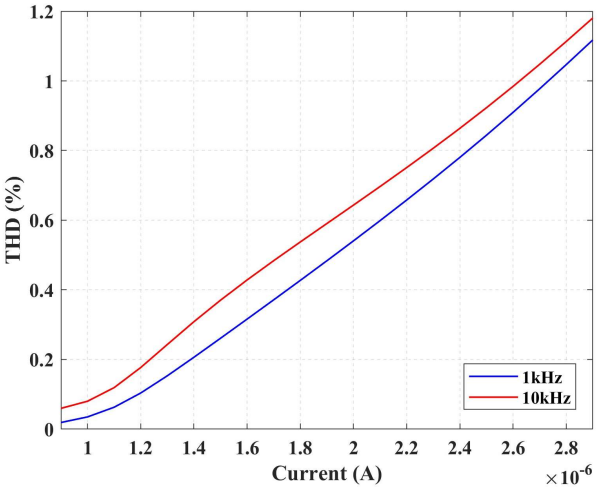

Figure 13. THD of current flowing from terminal Z versus magnitude of applied input current at X.

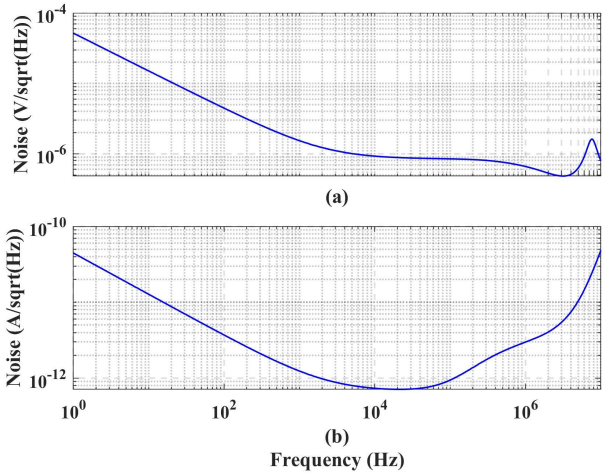

Figure 14. Input noise spectral density: (**a**) noise voltage at terminal Y (**a**) and (**b**) noise current at terminal X.

Table 3 summarizes the performance of the proposed CCII (last column) compared to recent low-voltage, low-power CCII implementations [28–33]. Notably, reference [33] is the only fully fabricated and measured design in the table. While both designs utilize a class AB configuration, reference [33] operates at a supply voltage exceeding 1 V. It can be observed that the trend favors reduced supply voltage and lower DC power consumption. However, maintaining acceptable values of equivalent resistance R_X, −3 dB frequencies for voltage and current transfer, and input current range at node X (which corresponds to the current drive capability at node Z) necessitates a trade-off between these parameters and current consumption. The proposed solution demonstrates good current utilization efficiency which can be defined as the ratio between the maximum input/output linear current ($I_{Xmax,Zmax}$) and the total quiescent current (I_Q). This efficiency metric highlights the proposed CCII's ability to achieve high performance while maintaining low power consumption. Moreover, the −3 dB frequency of the voltage transfer is also good in comparison to the low I_Q utilized.

Table 3. Performance comparison of low voltage CCIIs.

Ref.	[33] *	[28]	[29]	[30]	[31]	[32]		Proposed
Year	2003	2011	2012	2012	2017	2019		2024
Tech. (nm)	350	180	180	180	90	180		65
V_{DD} (V)	1.5	0.8	1	0.5	0.4	0.3	0.5	0.35
I_Q (µA)	173	80	10	60	4.5	63.3×10^{-3}	1.01	2.86
DC Power (µW)	2595	64	10	30	1.8	0.019	0.509	1
Y-Input voltage range (%VDD)	73	95	100	80	n.a.	100	100	97
X-Input current range (µA)	±900	±7	±3	±15	n.a.	±0.024	±0.4	2.5
$I_{Xmax,Zmax}/I_Q$	5.2	8.75×10^{-2}	0.3	0.25	n.a.	0.379	0.396	0.87
R_Y (MΩ)	∞	∞	∞	∞	n.a.	703	664	150 @10 kHz
R_X (Ω)	150	27	42	260	106	56×10^3	3×10^3	1.8×10^3
R_Z (MΩ)	0.3	0.89	53	0.113	n.a.	94.7	8	7.46
Voltage gain V_X/V_Y (mdB)	−20	0	0	−17.4	34.7	−11.3	−8.69*	−4.1
Current gain I_Z/I_X (dB)	−40	0	0	−34.8	0	−8.69	−8.69	−2.1
−3 dB BW V_X/V_Y (MHz)	2.4 @C_L = 10 pF	14	4.8	11	1	4.1×10^{-3} *	56.4×10^{-3} * @C_L = 30 pF	1.33 @C_L = 1 pF
−3 dB BW I_Z/I_X (MHz)	1.2	13	8.2	10	1.25	39.2×10^{-3}	578×10^{-3}	2.13

* Measured results.

As a final remark in the conclusion of this section, being the solution based on the topology in [19] that was experimentally characterized and found in reasonable agreement with the simulations, we are confident that also the simulations of this CCII, implemented in the same CMOS technology, provide meaningful and quite accurate results, even under MOSFETs' subthreshold regime.

4. Conclusions

This work demonstrated a 0.35 V high-performance CCII achieving rail-to-rail voltage operation at the Y terminal and class AB current operation at the Z terminal. The design leverages a previously developed low-voltage subthreshold bulk-driven CMOS OTA which strategically utilizes body terminals for enhanced small-signal and large-signal performance. The resulting circuit boasts high open-loop gain and cascoded current mirror topologies, leading to accurate voltage and current transfer with bandwidths of 1.33 MHz and 2.13 MHz, respectively. Under a total quiescent current consumption of 2.86 μA, the CCII provides a linear current drive of up to 2.5 μA, with one of the best figures of merit concerning current utilization.

This work contributes to the growing body of research on CCII implementations suitable for portable and implantable electronics and for emerging applications requiring high performance and sub-1V, low-power consumption.

Author Contributions: Conceptualization, S.P.; methodology, M.O.S. and M.C.; validation, M.O.S. and M.C.; writing—original draft preparation, S.P.; writing—review and editing, M.O.S. and M.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was developed under project SAMOTHRACE (ECS00000022) and funded by the European Union (NextGeneration EU), through the MUR-PNRR.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Chatterjee, S.; Tsividis, Y.; Kinget, P. 0.5-V Analog Circuit Techniques and their Application in OTA and Filter Design. *IEEE J. Solid-State Circuits* **2005**, *40*, 2373–2387. [CrossRef]
2. Monsurrò, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. Biasing technique via bulk terminal for minimum supply CMOS amplifiers. *Electron. Lett.* **2005**, *41*, 779–780. [CrossRef]
3. Monsurró, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. Exploiting the Body of MOS Devices for High Performance Analog Design. *IEEE Circuits Syst. Mag.* **2011**, *11*, 8–23. [CrossRef]
4. Khateb, F.; Dabbous, S.B.A.; Vlassis, S. A Survey of Nonconventional Techniques for Low-voltage Low-power Analog Circuit Design. *Radioengineering* **2013**, *22*, 415–427.
5. Moghaddam, A.K.; Chuah, J.H.; Ramiah, H.; Ahmadian, J.; Mak, P.-I.; Martins, R.P. A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 992–1002. [CrossRef]
6. Blalock, B.; Allen, P.; Rincon-Mora, G. Designing 1-V Op Amps Using Standard Digital CMOS Technology. *IEEE Trans. Circuits Syst. II Analog. Digit. Signal Process.* **1998**, *45*, 769–780. [CrossRef]
7. Ferreira, L.H.C.; Sonkusale, S.R. A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2014**, *61*, 1609–1617. [CrossRef]
8. Abdelfattah, O.; Roberts, G.W.; Shih, I.; Shih, Y.-C. An Ultra-Low-Voltage CMOS Process-Insensitive Self-Biased OTA With Rail-to-Rail Input Range. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 2380–2390. [CrossRef]
9. Cabrera-Bernal, E.; Pennisi, S.; Grasso, A.D.; Torralba, A.; Carvajal, R.G. 0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1807–1815. [CrossRef]
10. Kulej, T.; Khateb, F. Design and Implementation of Sub 0.5-V OTAs in 0.18-μm CMOS. *Int. J. Circuits Theor. Appl.* **2018**, *46*, 1129–1143. [CrossRef]
11. Khateb, F.; Kulej, T. Design and Implementation of a 0.3-V Differential Difference Amplifier. *IEEE Trans. Circuits Syst. I Regul. Papers* **2019**, *66*, 513–523. [CrossRef]
12. Kulej, T.; Khateb, F. A 0.3-V 98-dB Rail-to-Rail OTA in 0.18 mm CMOS. *IEEE Access* **2020**, *8*, 27459–27467. [CrossRef]
13. Woo, K.-C.; Yang, B.-D. A 0.25-V Rail-to-Rail Three-Stage OTA with an Enhanced DC Gain. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 1179–1183. [CrossRef]

14. Ballo, A.; Grasso, A.D.; Pennisi, S. 0.4-V, 81.3-nA Bulk-Driven Single-Stage CMOS OTA with Enhanced Transconductance. *Electronics* **2022**, *11*, 2704. [CrossRef]
15. Centurelli, F.; Della Sala, R.; Monsurró, P.; Tommasino, P.; Trifiletti, A. An Ultra-Low-Voltage class-AB OTA exploiting local CMFB and Body-to-Gate interface. *AEU-Int. J. Electr. Comm.* **2022**, *145*, 154081. [CrossRef]
16. Akbari, M.; Hussein, S.M.; Hashim, Y.; Tang, K.-T. 0.4-V Tail-Less Quasi-Two-Stage OTA Using a Novel Self-Biasing Transconductance Cell. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2022**, *69*, 2805–2818. [CrossRef]
17. Kulej, T.; Khateb, F.; Arbet, D.; Stopjakova, V. A 0.3-V High Linear Rail-to-Rail Bulk-Driven OTA in 0.13 µm CMOS. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, *69*, 2046–2050. [CrossRef]
18. Ballo, A.; Grasso, A.D.; Pennisi, S.; Susinni, G. A 0.3-V 8.5-µ a Bulk-Driven OTA. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2023**, *31*, 1444–1448. [CrossRef]
19. Ballo, A.; Carvajal, R.G.; Grasso, A.D.; Luján-Martínez, C.I.; Pennisi, S.; Venezia, C. 0.35-V SR-Enhanced Bulk-Driven OTA for Loads up to 10 nF. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2024**. *in print*. [CrossRef]
20. He, T.; Lee, C. Evolving Flexible Sensors, Wearable and Implantable Technologies Towards BodyNET for Advanced Healthcare and Reinforced Life Quality. *IEEE Open J. Circuits Syst.* **2021**, *2*, 702–720. [CrossRef]
21. Das, R.; Moradi, F.; Heidari, H. Biointegrated and Wirelessly Powered Implantable Brain Devices: A Review. *IEEE Trans. Biomed. Circuits Syst.* **2020**, *14*, 343–358. [CrossRef] [PubMed]
22. Shi, Q.; Dong, B.; He, T.; Sun, Z.; Zhu, J.; Zhang, Z.; Lee, C. Progress in Wearable Electronics/photonics—Moving toward the Era of Artificial Intelligence and Internet of Things. *InfoMat* **2020**, *2*, 1131–1162. [CrossRef]
23. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Design of Digital OTAs with Operation Down to 0.3 V and nW Power for Direct Harvesting. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2021**, *68*, 3693–3706. [CrossRef]
24. Ferri, G.; Guerrini, N. *Low-Voltage Low-Power CMOS Current Conveyors*; Springer: Berlin/Heidelberg, Germany, 2003.
25. Colucci, P.; D'amico, A.; De Marcellis, A.; Falconi, C.; Ferri, G.; Giovannelli, F.; Parente, F.R.; Stornelli, V. CCII-based voltage amplifier optimization for reduced relative gain error. *Circuits Syst. Signal Process.* **2018**, *37*, 1315–1326. [CrossRef]
26. Stornelli, V.; Ferri, G.; Pantoli, L.; Barile, G.; Pennisi, S. A rail-to-rail constant-gm CCII for instrumentation amplifier applications. *AEU-Int. J. Electron. Commun.* **2018**, *91*, 103–109. [CrossRef]
27. De Marcellis, A.; Ferri, G.; Mantenuto, P. A CCII-based non-inverting Schmitt trigger and its application as astable multivibrator for capacitive sensor interfacing. *Int. J. Circuit Theory Appl.* **2017**, *45*, 1060–1076. [CrossRef]
28. Khateb, F.; Khatib, N.; Kubánek, D. Novel low-voltage low-power high-precision CCII± based on bulk-driven folded cascode OTA. *Microelectron. J.* **2011**, *42*, 622–631. [CrossRef]
29. Khateb, F.; Khatib, N.; Kubánek, D. Novel ultra-low-power class AB CCII+ based on floating-gate folded cascode OTA. *Circuits Syst. Signal Process.* **2012**, *31*, 447–464. [CrossRef]
30. Raikos, G.; Vlassis, S.; Psychalinos, C. 0.5V bulk-driven analog building blocks. *AEU-Int. J. Electron. Commun.* **2012**, *66*, 920–927. [CrossRef]
31. Eldeeb, M.A.; Ghallab, Y.H.; Ismail, Y.; Elghitani, H. Low-voltage subthreshold CMOS current mode circuits: Design and applications. *AEU-Int. J. Electron.* **2017**, *82*, 251–264. [CrossRef]
32. Khateb, F.; Kulej, T.; Kumngern, M. 0.3V Bulk-Driven Current Conveyor. *IEEE Access* **2019**, *7*, 65122–65128. [CrossRef]
33. Mita, R.; Palumbo, G.; Pennisi, S. 1.5-V CMOS CCII+ with high current-driving capability. *IEEE Trans. Circuits Syst. II Analog. Digit. Signal Process.* **2003**, *50*, 187–190. [CrossRef]
34. Arbel, A. Comparison between the Noise Performances of Current-Mode and Voltage-Mode Amplifiers. *Int. J. Analog. Integr. Circuits Signal Process.* **1995**, *7*, 221–242. [CrossRef]