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An Ultra-Low-Voltage Approach to Accurately Set the Quiescent Current of Digital Standard Cells Used for Analog Design and Its Application on an Inverter-Based Operational Transconductance Amplifier

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Abstract: An approach to design analog building blocks based on digital standard cells is presented in this work. By ensuring that every CMOS inverter from a standard-cell library operates with a well-defined quiescent current and output voltage, the suggested method makes it possible to construct analog circuits that are resistant against PVT variations. The method uses the local supply voltages connected to the source terminals of the p-channel and n-channel MOS transistors of the standard-cell inverters as control inputs. It is based on adaptive supply voltage generator (ASVG) reusable blocks, which are comparable to those used in digital applications to handle process variations. All of the standard-cell inverters used for analog functions receive the local supply voltages produced by the ASVGs, which enable setting each cell's quiescent current to a multiple of a reference current and each cell's static output voltage to an appropriate reference voltage. Both the complete custom design of the ASVG blocks and a theoretical study of the feedback loop of the ASVG are presented. An application example through the design of a fully synthesizable two-stage operational transconductance amplifier (OTA) is also provided. The TSMC 180 nm CMOS technology has been used to implement both the OTA and the ASV generators. Simulation results have demonstrated that the proposed approach allows to accurately set the quiescent current of standard-cell inverters, dramatically reducing the effect of PVT variations on the pmain performance parameters of the standard-cell-based two-stage OTA.

Keywords: ultra-low voltage; ultra-low power; IoT; OTA; body driven; replica bias; CMFF

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1. Introduction

The evolution of technology has made electronics more and more pervasive [1–3]. Modern electronic systems are essentially digital systems [4] with analog interfaces, enabling them to interact with the real world [5–7]. However, even if the analog part often constitutes just a small fraction of the overall system, its design typically requires the most effort since it is a custom, trial-and-error process, compared to the fully automated design and layout of the digital part [8–15]. For this reason, research is ongoing to automate the design of analog blocks, or at least use automatic place and route tools for the layout phase, to speed up the marketing time and improve the portability of designs across different technologies [16]. In this context, an interesting research field concerns the use of digital standard cells to design analog blocks that are compatible with the automatic place and route tools of the digital design flow [17–21].

Two approaches are possible to design standard-cell-based analog blocks: the analog functions can be rethought from basic principles to implement them in the digital domain (e.g., DIGOTA [13,14,20,22], dyadic pulse DAC [23–26]). On the other hand, standard cells can be exploited to mimic the basic analog building blocks and reproduce analog circuit

topologies [9,18,19,27,28]. The latter approach allows a better control of the circuits' analog performance and is more familiar to the analog designer; however, it requires the designer to cope with the variations of process parameters, temperature, and supply voltage (PVT).

A typical field of application for such circuits is that of ultra-low-voltage (ULV) and ultra-low-power (ULP) systems [29] for biomedical and Internet of Things (IoT) systems [30–36] that include a large digital part, with a low supply voltage (0.3–0.5 V) limiting the use of standard analog approaches such as differential pairs and cascode [37–40]. To implement analog functions such as amplifiers and filters [41–44], body driving and inverter-based stages are the most common options [37,45–56]. For blocks at the edge of the analog and digital worlds, such as comparators, the use of standard cells allows an efficient implementation of low-voltage latches [57–61].

In absence of the tail current generator, which is not compatible with the ULV environment, controlling the bias point of gain stages and hence the performance of the amplifiers (gain, gain–bandwidth product)—with respect to variations in PVT and input common-mode voltage—is extremely difficult [19,27]. Body biasing is a solution that is often adopted in inverter-based stages [45,62], but it is compatible only with standard-cell families where body voltage rails are explicitly accessible.

An approach to center the input–output transfer characteristic of standard-cell inverters to keep the DC output voltage constant has been recently proposed in [27]. This allows us to design robust amplifiers, such as a cascade of inverter stages, keeping them optimally biased [18,28]; however, this also provides no control of the inverters' quiescent current and hence on their transconductance (and consequently on the gain–bandwidth product of amplifiers based on such inverters). The quiescent current is in fact affected by PVT variations of the threshold voltage of devices [51], and this causes huge variations of the transconductance, especially in standard-cell inverters biased in the sub-threshold region [9,45].

Adaptive supply voltage scaling (ASV) is often utilized by digital designers to cope with PVT variations and to reduce the spread of the maximum operating frequency and power consumption of digital circuits [63–65]. In these approaches, specific adaptive supply voltage generators (ASVGs) are exploited to provide local supply voltage for optimizing the speed/power consumption trade-off [66]. These blocks are typically designed following a full-custom approach, similarly to the standard cells in the digital libraries of a given technology. Once all the needed files are available, ASVGs can be used in a semi-custom design flow, where the layout step is performed by an automatic place and route tool.

In this work, we propose a novel approach in which suitable ASVGs are exploited to keep the bias current of digital standard cells used for analog design constant by generating suitable values of local supply voltages $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ in order to counteract the effects of PVT variations on the quiescent current. The proposed approach is applied to the design of a simple two-stage inverter-based OTA implemented with standard-cell inverters. Simulation results referring to the standard-cell library of a 180 nm CMOS technology highlight the capability of the proposed methodology to dramatically reduce the spread of main OTA performance parameters with respect to the conventional design. In Section 2, we present both a theoretical study and simulation results of the conventional standard-cell-based two-stage OTA operating in sub-threshold to highlight the strong impact of PVT variations on the main OTA parameters. The proposed approach to set the quiescent current of standard-cell inverters and its application to a standard-cell-based two-stage OTA are discussed in Section 3, the results of parametric and Monte Carlo simulations are presented in Section 4, and some conclusion are drawn in Section 5.

2. Two-Stage Standard-Cell-Based OTA Operating in Sub-Threshold

To explain the proposed approach in detail, we refer, as a case study, to the conventional two-stage inverter-based OTA implemented with standard-cell inverters. The topology of the two-stage inverter-based OTA is depicted in Figure 1. The first stage is composed using $I_{1–4}$, which implement a standard-cell-based differential to a single-ended

converter [19], whereas the second stage is composed using I_5, implementing the inverting output stage. Although it is simple, this architecture is very effective for highlighting the main limitations that come from the adoption of a standard-cell approach to analog design, in which analog blocks are directly connected to the supply voltages V_{DD} and V_{SS}, without any control of the bias current of standard-cell inverters.

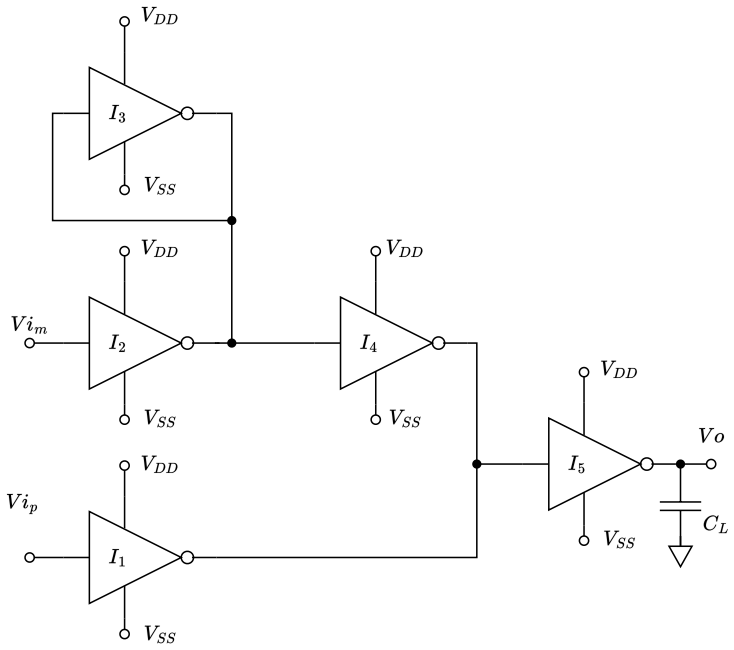


Figure 1. Conventional two-stage standard-cell-based OTA.

2.1. Characterization of the CMOS Inverter Operating in Sub-Threshold and Transfer Matrix

For the following analysis, we denote the input capacitance of the generic *i*-th inverter with C_{gs_i}, which is given by the sum of the gate-source capacitances $C_{gs_{n,p_i}}$ of the NMOS and PMOS transistors of the inverter, with C_{gd_i} being the sum of the gate-drain capacitances $C_{gd_{n,p_i}}$, gm_i being the sum of the transconductances gm_{n,p_i} of the NMOS and PMOS transistors of the inverter, and with gds_i being the sum of output conductances gds_{n,p_i} of the NMOS and PMOS transistors of the inverter. By using this notation, the inverter's transfer matrix input voltage, output voltage, and currents can be written as follows:

$$\begin{bmatrix} V_{In} \\ I_{In} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \times \begin{bmatrix} V_{Out} \\ -I_{Out} \end{bmatrix} \tag{1}$$

where

$$A = \frac{gds_i}{gm_i}\left(1 + s\, C_{gd_i}/gds_i\right) \tag{2}$$

$$B = \frac{s \cdot \left(Cgs_i + gm_i/gds_i \cdot Cgd_i\right) \cdot gds_i}{gm_i} \cdot \left(1 + s\, C_{gd_i}/gds_i\right) \tag{3}$$

$$C = 1/gm_i \tag{4}$$

and, finally,

$$D = \frac{s \cdot \left(Cgs_i + gm_i/gds_i \cdot Cgd_i\right)}{gm_i} \tag{5}$$

As it can be observed, the coefficients of the inverter's transfer matrix depend on terms gm_i and gds_i. These terms rely on the quiescent current of the NMOS and PMOS transistors

of the inverter which, due to the operation in the sub-threshold region, can be expressed as follows:

$$\begin{cases} I_{d_n} = I_{d_{0n}} e^{\frac{Vgs_n - Vth_n}{n\ Ut}} \left(1 - e^{-\frac{Vds_n}{Ut}}\right) & \text{NMOS} \\ I_{d_p} = I_{d_{0p}} e^{\frac{Vsg_p + Vth_p}{n\ Ut}} \left(1 - e^{-\frac{Vsd_p}{Ut}}\right) & \text{PMOS} \end{cases} \tag{6}$$

where usual notation is adopted for gate-source, drain-source, and threshold voltages of NMOS and PMOS transistors; Ut denotes the thermal voltage; and $n = 1 + C_{depl}/C_{ox}$ and I_{d_0} can be written as follows:

$$I_{d_{0n,p}} = \mu_{n,p}(n-1)C_{ox}\frac{W_{n,p}}{L_{n,p}}U_t^2 \tag{7}$$

where $\mu_{n,p}$ and C_{ox} are the mobility and oxide capacitance per unit area, whereas $W_{n,p}$ and $L_{n,p}$ are the gate width and gate length of NMOS and PMOS devices, respectively.

It is evident from the above equations that the quiescent current of MOS devices, and therefore the small signal parameters of the inverter, are strongly dependent on PVT variations. This has a strong impact on the performance parameters of the conventional two-stage standard-cell-based OTA, as it will be better pointed out in the next subsections.

2.2. Analytical Characterization of the Standard-Cell-Based Two-Stage OTA

The most important performance parameters of an OTA are the gain–bandwidth product (GBW), the phase margin ($m\varphi$), the differential voltage gain (Av_D), the power consumption (P_d), and the average slew rate (SR_{avg}). Referring to the OTA in Figure 1, using the notation introduced in Section 2.1, and denoting the load capacitance of the OTA with C_L, the main performance parameters of the OTA can be easily expressed as follows:

$$Av_D = \frac{1}{2}\left(1 + \frac{gm_2}{gm_3}\right) \cdot \frac{gm_1}{gds_4 + gds_1} \cdot \frac{gm_5}{gds_5} \cdot \frac{1}{1 + sC_L/gds_5} \tag{8}$$

$$GBW = \frac{1}{2}\left(1 + \frac{gm_2}{gm_3}\right) \cdot \frac{gm_1}{gds_4 + gds_1} \cdot \frac{gm_5}{C_L} \tag{9}$$

$$m\varphi = 180 - arctan\left\{GBW \cdot \frac{gds_4 + gds_1}{C_{gs_5}}\right\} - arctan\left\{GBW \cdot \frac{gds_5}{C_L}\right\} \tag{10}$$

$$SR_{avg} = \frac{Id_0\ e^{\frac{V_{DD} - Vth_n}{n\ Ut}} + Id_0\ e^{\frac{V_{DD} - Vth_p}{n\ Ut}}}{2} \tag{11}$$

As it can be observed, all the terms in the above equations depend on gm_i and gds_i of the inverters, which, as discussed in Section 2.1, are strongly dependent on the supply voltages, which set the value of gate-source and drain-source voltages, the temperature (due to the temperature dependence of parameters such as Ut or $I_{d_{0n,p}}$), and process variations (due to the dependence of V_{th} on process steps).

All these considerations allow us to conclude that the conventional standard-cell-based two-stage OTA exhibits performance parameters that strongly dependent on PVT variations. This point will be further assessed in the next section through transistor-level simulations.

2.3. Simulation Results on the Conventional Standard-Cell-Based Two-Stage OTA Operating in Sub-Threshold without Quiescent Current Control

The two-stage standard-cell-based OTA reported in Figure 1 was designed in reference to the standard-cell library of the TSMC 180 nm CMOS technology with a nominal supply voltage $V_{DD} - V_{SS}$ of 0.35 V. Transistor-level simulations were carried out within the Cadence Virtuoso environment. To quantify the dependence of performance parameters on PVT variations, parametric and corner simulations were executed. The results are summarized in Table 1, where V_{off} denotes the error with respect to the ideal DC output

voltage of the OTA in a unity–gain feedback configuration and where Itot is the total current drawn by the OTA. The first five columns in the table (from Typ to FS) refer to the five process corners of the technology, the sixth and seventh column refer to supply voltage variations, and the last two columns refer to temperature variations.

Table 1. Performance parameters of the conventional standard-cell-based OTA under PVT variations.

	Typ	**FF**	**SS**	**SF**	**FS**	**90% V_{DD}**	**110% V_{DD}**	**0°**	**80°**
V_{off} [mV]	2.2	2	2.3	−0.5	7.1	7.6	2.9	2.2	2.2
Pd [nW]	1.688	6.958	0.371	1.599	3.338	1.013	1.505	0.536	9.713
Itot [nA]	4.221	17.39	0.927	3.998	8.345	3.217	3.909	1.341	24.28
Av_d [dB]	52.12	49.53	56.41	51.95	51.18	48.71	51.78	52.9	50.55
GBW [kHz]	53.56	217.8	12.12	66.63	39.58	13.32	42.22	18.05	265.8
$m\varphi$ [deg]	60.41	63.03	56.38	53.67	71.71	72.89	63.92	60.9	60.46
SR_{avg} [V/ms]	144.5	546.2	34.17	149.5	394.1	21.59	101.1	90.86	368.1

The results of process-only and mismatch-only Monte Carlo simulations are reported in Table 2 and Table 3, respectively. The histograms of GBW, Pd, and $m\varphi$ under process-only and mismatch-only Monte Carlo simulations are reported in Figure 2 and Figure 3, respectively.

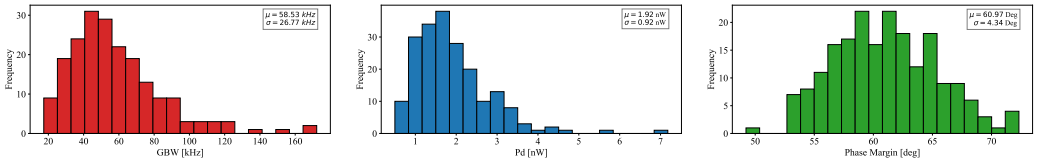
Table 2. Performance parameters of the conventional standard-cell-based OTA under process-only Monte Carlo simulations.

	Mean	**Std Dev**
V_{off} [mV]	2.3	0.99
Pd [nW]	1.92	0.92
Itot [nA]	4.379	2.319
Av_d [dB]	51.12	0.90
$m\varphi$ [deg]	60.97	4.34
GBW [kHz]	58.53	26.77
SR_{avg} [V/ms]	147.5	80.44

Table 3. Performance parameters of the conventional standard-cell-based OTA under mismatch-only Monte Carlo simulations.

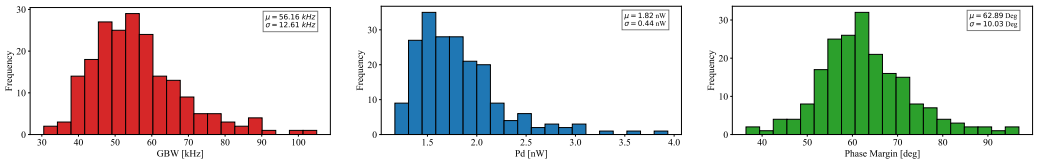
	Mean	**Std Dev**
V_{off} [mV]	3.1	18.11
Pd [nW]	1.82	0.44
Itot [nA]	4.314	1.106
Av_d [dB]	49.11	10.11
$m\varphi$ [deg]	62.89	10.03
GBW [kHz]	56.16	12.61
SR_{avg} [V/ms]	146	30.52

As it can be observed in all the above tables and figures, the quiescent current of the standard-cell inverters operating in a sub-threshold exhibits huge variations, resulting in large variations in the GBW and $m\varphi$ of the OTA. Due to this behavior, the applicability of this OTA to signal processing systems presents many difficulties and drawbacks, and its usage is not justified. In order to make this standard-cell-based OTA usable in real applications, the quiescent current of the inverters should be controlled to at least reduce variations with respect to temperature and process variations.



(**a**) (**b**) (**c**)

Figure 2. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the conventional standard-cell-based OTA under process-only Monte Carlo simulations.



(**a**) (**b**) (**c**)

Figure 3. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the conventional standard-cell-based OTA under mismatch-only Monte Carlo simulations.

3. Proposed Approach to Set the Quiescent Current of Standard-Cell Inverters and Application to a Standard-Cell-Based OTA

In the conventional approach, standard-cell inverters are directly supplied with two constant voltages V_{DD} and V_{SS}. However, standard-cell inverters with constant supply voltages V_{DD} and V_{SS} exhibit huge variations in their transconductance, especially if operating in a sub-threshold. This, as demonstrated in the previous section, results in large variations in the main OTA parameters, such as the gain–bandwidth product, the power dissipation, and the phase margin.

In order to properly set the quiescent current of standard-cell inverters, the approach proposed here takes advantage of two locally generated supply voltages, $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$, whose main role is to accurately set the DC current of all the standard-cell inverters used for analog design through a replica-bias approach, thus strongly reducing the variability of the transconductance and output conductance gm_i and gds_i of the standard-cell inverters operating in a sub-threshold. The simplified schematic of the proposed approach to set the quiescent current of standard-cell inverter is reported in Figure 4. The two circuits in the upper and lower right corner of the figure act as ASV generators to produce the $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$, respectively. These voltages are then routed as local supply voltages to all the standard-cell inverters used for analog purposes (i.e., the inverters implementing the two-stage OTA in this example). Referring to Figure 4, transistors Mn_3 and Mp_3 implement a replica of the NMOS and PMOS device of the minimum area standard-cell inverter, respectively, whereas Mn_1–Mn_2 and Mp_1–Mp_2 implement conventional current mirrors that force a reference current I_{bias} in Mn_3 and Mp_3. The gate voltage of the replica devices Mn_3 and Mp_3 is set to a reference voltage V_{ref} (usually set at the midpoint between V_{DD} and V_{SS}), and their drain voltage is compared with the same reference voltage V_{ref} through the two error amplifiers EA_1 and EA_2. The task of amplifiers EA_1 and EA_2 is to generate the two control voltages, $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$, which close the loops at the source nodes of Mp_3 and Mn_3, respectively. In this way, the two control voltages $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ are changed by the feedback loops in order to set the bias current of Mn_3 and Mp_3 to I_{bias} and the drain voltages of Mn_3 and Mp_3 to V_{ref} despite PVT variations, as will be better assessed in the next sections.

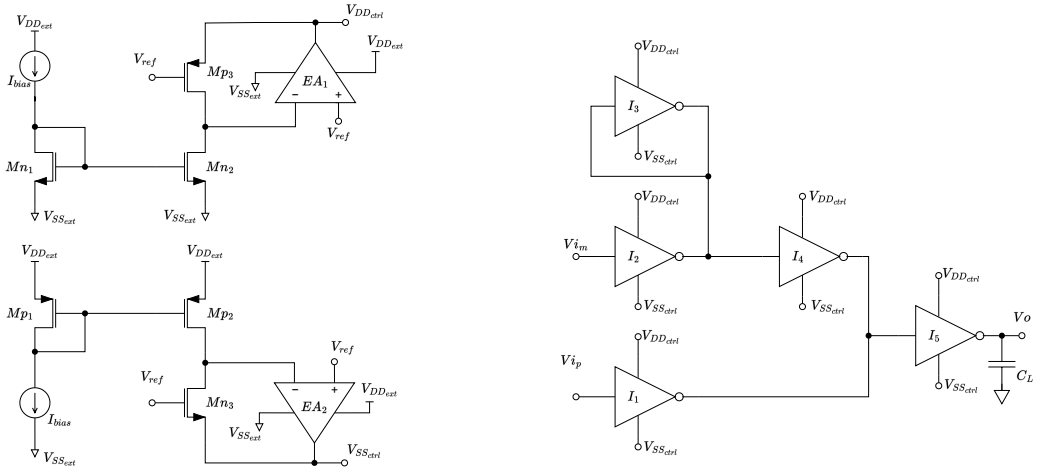


Figure 4. Proposed approach to set the quiescent current of standard-cell inverters and application to the standard-cell-based two-stage OTA.

3.1. Analysis of the Feedback Loop in the ASV Generators

In the following section, we derive a simplified model of the feedback loop implementing the ASV generator for the $V_{DD_{ctrl}}$ (see the upper right corner of Figure 4). A similar model can be developed for the ASV generator for the $V_{SS_{ctrl}}$. The block scheme derived for the feedback loop in the upper right corner of Figure 4 is depicted in Figure 5: Id_{p_3} is the current that flows in Mp_3 when the supply voltage $V_{DD_{ctrl}}$ has its nominal value, and Vx is the variation of $V_{DD_{ctrl}}$ with respect to such value. I_{bias} is the reference current, mirrored through $Mn_{1,2}$.

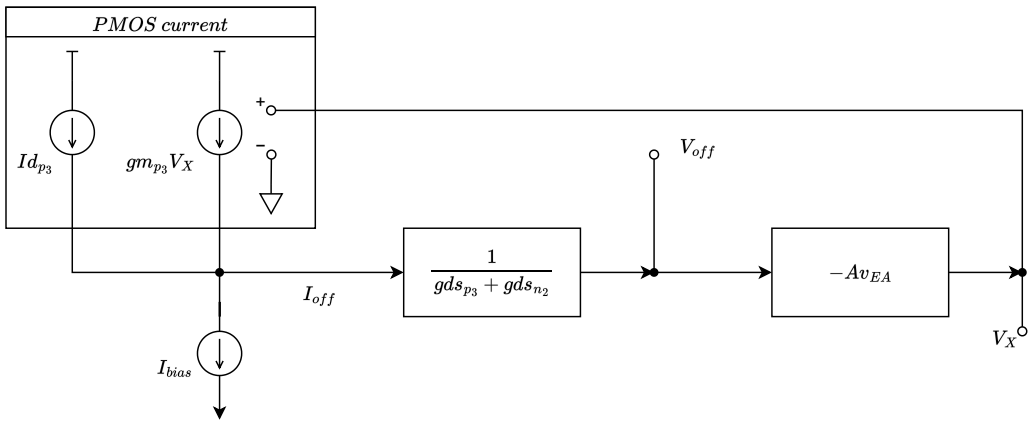


Figure 5. Block scheme derived for the feedback loop of the $V_{DD_{ctrl}}$ ASV generator.

The comparison between the drain current of Mp_3 and I_{bias} generates an offset current I_{off} which, flowing through the output conductance $gds_{p3} + gds_{n2}$, turns into an offset voltage (V_{off} in Figure 5 is the difference between the DC output voltage and V_{ref}). The error amplifier EA_1, with gain Av_{EA}, closes the loop, modifying the supply voltage $V_{DD_{ctrl}}$, hence the current in Mp_3, to cancel the offset. Due to the finite loop gain, the residual offset current is

$$I_{off} = \frac{Id_{p_3} - Id_{bias}}{1 + \frac{gm_{p3}Av_{EA}}{gds_{p3}+gds_{n2}}} \tag{12}$$

By performing the same analysis on the feedback loop in the ASV generator for the $V_{SS_{ctrl}}$, the offset current in Mn_3 can be expressed as follows:

$$I_{off} = \frac{Id_{n_3} - Id_{bias}}{1 + \frac{gm_{n3} Av_{EA}}{gds_{n3} + gds_{p2}}} \tag{13}$$

Equations (12) and (13) show that the proposed feedback loops suppress the offset current by a factor given by the gain of the auxiliary amplifier times the gain of the replica stage. This means that the feedback loops allow us to set the quiescent current of Mp_3 and of Mn_3 to I_{bias}, strongly reducing the effect of PVT variations (which give rise to the component I_{off}). It has to be pointed out that, since Mp_3 and of Mn_3 are a replica of the transistors of the standard-cell inverter, the quiescent current of all the standard-cell inverters using $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ as local supply voltages will also be set approximately equal to I_{bias} despite PVT variations.

3.2. Implementation of the Error Amplifier

The error amplifier was implemented according to Figure 6. It is a two-stage OTA with a Miller compensation. The transistors' sizes are reported in Table 4. Since V_{ref} = 0.2 V, V_{DD} = 0.5 V, and Mp_3 and Mp_4 are biased in a sub-threshold, the current source Mp_2 is properly biased in saturation. The compensation capacitance C_{comp} is 10 pF, whereas Co_{EA} is the parasitic capacitance seen at the output of the error amplifier, which is in the order of hundreds fF (it depends on the C_{gs} and C_{gd} seen at the source terminals of transistors).

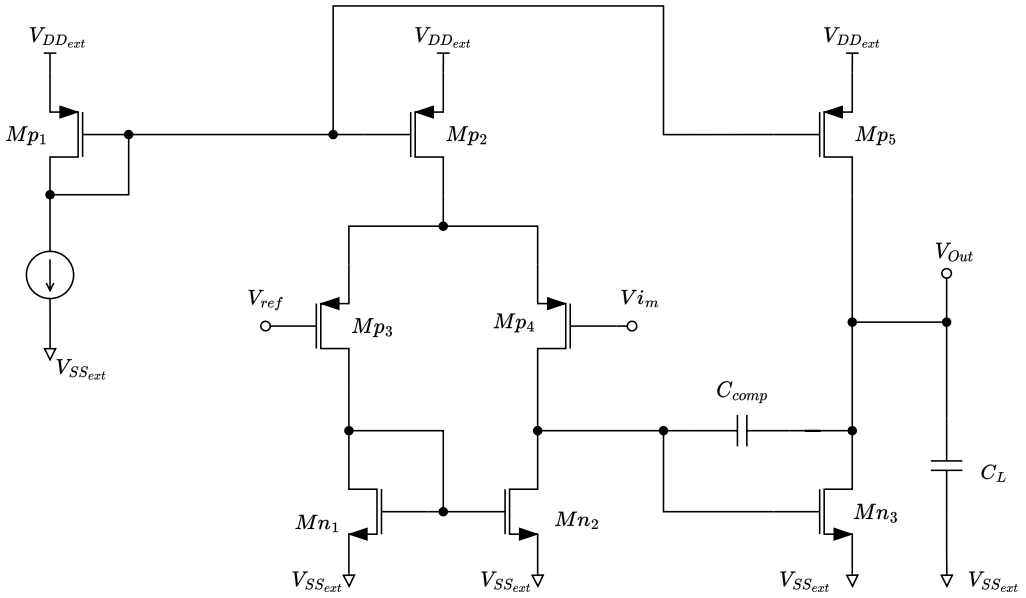


Figure 6. Schematic of the error amplifier.

Table 4. Transistor sizing of the error amplifier.

	$Mp_1 = Mp_2$	$Mp_3 = Mp_4$	$Mn_1 = Mn_2$	Mn_3	Mp_5
W [m]	1 µ	1 µ	440 n	3.52 µ	4 µ
L [m]	500 n	500 n	1 µ	220 n	500 n

To effectively bias multiple stages, it is crucial to properly size the error amplifier's output stage, which has to supply a current to all the standard cells. In the design phase, by estimating the overall system requirements, the error amplifier can be appropriately sized to bias all cells simultaneously, eliminating the need for additional stages.

3.3. Impact of the $V_{DD_{ctrl}}$ and $V_{SS_{ctrl}}$ ASV Generators on the PSRR

By using the proposed approach to stabilize the bias current of standard-cell-based analog blocks, the supply voltage to such blocks is provided by the ASV generators. This affects the power supply rejection ratio (PSRR) of the analog block, since disturbances from the overall supply voltages are filtered by the ASVGs: the overall gain from the global positive supply voltage to the output of the analog block can be written as

$$A_{dd,tot} = A_{ASV1,dd}A_{dd} + A_{ASV2,dd}A_{ss} \tag{14}$$

and

$$A_{ss,tot} = A_{ASV1,ss}A_{dd} + A_{ASV2,ss}A_{ss} \tag{15}$$

where A_{dd} and A_{ss} are the gains from positive and negative supply voltages to the output of the analog block (e.g., an OTA), and $A_{ASV1,dd}(A_{ASV1,ss})$ and $A_{ASV2,dd}(A_{ASV2,ss})$ are the gains from the positive (negative) supply voltage to the outputs of the positive and negative (positive) ASVGs, respectively. An analog expression can be written for the negative supply voltage.

The analysis of the ASVG circuit in Figure 4 shows that the gains $A_{ASV1,dd}$ and $A_{ASV2,ss}$ are approximately inversely proportional to the intrinsic gain A_0 of MOS devices, thus resulting in an improvement of the order of A_0 in the PSRR. If we define the positive and negative PSRRs of the analog block as $PSRRd$ and $PSRRs$, the overall positive and negative PSRRs are approximately given by

$$PSRRd_{tot} = \frac{A_0}{\frac{1}{PSRRd} - \frac{1}{PSRRs}\left(1 + \frac{gm_p}{gm_n}\right)} \tag{16}$$

$$PSRRs_{tot} = \frac{A_0}{\frac{1}{PSRRs} - \frac{1}{PSRRd}\left(1 + \frac{gm_n}{gm_p}\right)} \tag{17}$$

where the generic transconductance gain of MOS devices is denoted with gm_p and gm_n.

In Figure 7, the gain $A_{ASV1,dd}$ is reported in a blue color, gain $A_{ASV2,dd}$ is reported in a green color, gain $A_{ASV1,ss}$ is reported in a red color, and gain $A_{ASV2,ss}$ is reported in a purple color.

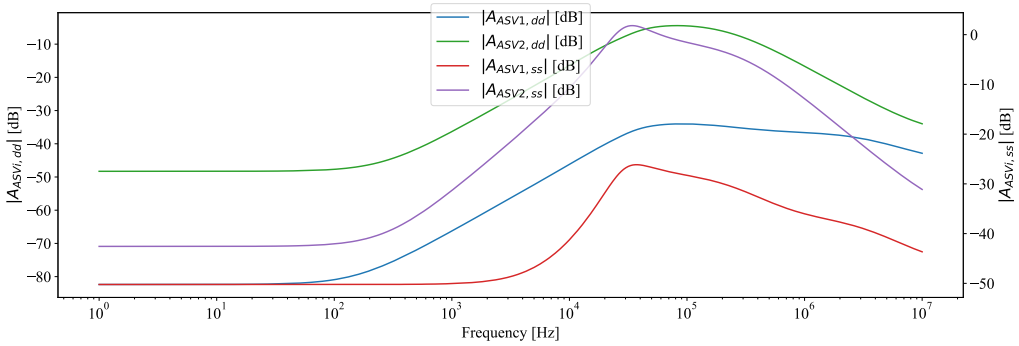


Figure 7. Gain $A_{ASV1,dd}$ is reported in a blue color, gain $A_{ASV2,dd}$ is reported in a green color, gain $A_{ASV1,ss}$ is reported in a red color, and gain $A_{ASV2,ss}$ is reported in a purple color.

4. Simulation Results on the Standard-Cell-Based Two-Stage OTA Operating in Sub-Threshold with the Proposed Quiescent Current Control

The two-stage standard-cell-based OTA with the proposed quiescent current control scheme reported in Figure 4 was also designed in reference to the TSMC 180 nm CMOS technology, with a global supply voltage $V_{DD} - V_{SS}$ of 0.5 V for the ASV generators and a nominal local supply voltage $V_{DD_{ctrl}} - V_{SS_{ctrl}}$ of 0.35 V for the standard-cell invert-

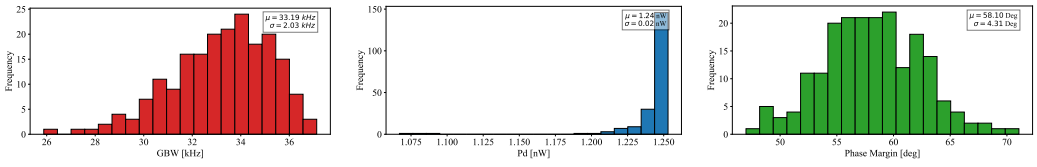
ers used in the OTA. Transistor-level simulations were carried out within the Cadence Virtuoso environment.

To highlight the effectiveness of the proposed approach in strongly reducing the effects of PVT variations, the same parametric and corner simulations executed for the OTA without the quiescent current control were also carried out on the OTA, exploiting the proposed current control approach. Results of these simulations are summarized in Table 5, where Itot is the total current drawn by the OTA. The first five columns in the table refer to the five process corners of the technology, the sixth and seventh columns refer to global supply voltage variations, and the last two columns refer to temperature variations. As it can be observed, with respect to the conventional OTA without quiescent current control, both current dissipation and the GBW are much more stable. To further improve the robustness of the proposed circuit to temperature variations, the reference current I_{bias} was assumed to be generated by a proportional to absolute temperature (PTAT) current source, which set a bias DC in the standard-cell inverter to approximately 500 pA in typical conditions. The usage of the PTAT current source is evident from the the last two columns of Table 5, in which Itot results varied from 1.945 nA to 3.56 nA in order to keep the GBW almost constant in the specified temperature range from 0° to 80°.

Table 5. Performance parameters of the standard-cell-based OTA with the proposed quiescent current control scheme under PVT variations.

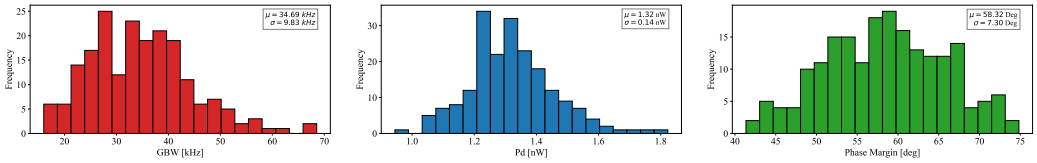
	Typ	**FF**	**SS**	**SF**	**FS**	**90% V_{DD}**	**110% V_{DD}**	**0**	**80**
V_{off} [mV]	0.01	0.04	0.2	−0.1	0.023	0.02	0.13	0.04	0.03
Itot [nA]	2.497	2.505	2.167	2.399	2.499	2.477	2.499	1.945	3.56
Pd [nW]	1.249	1.253	1.084	1.199	1.249	1.239	1.25	0.972	1.78
Av_d [dB]	51.29	45.72	58.65	51.19	50.72	51.27	51.29	53.59	45.41
$m\varphi$ [deg]	57.8	69.8	40.79	58	59.12	57.83	57.82	52.75	69.71
GBW [kHz]	33.67	27.42	36.04	31.91	33.48	33.42	33.68	31.25	31.42
SR_{avg} [V/ms]	30.1	12.27	114.6	19.27	55.41	33.83	29.32	70.82	7.218

In addition, the results of process-only and mismatch-only Monte Carlo simulations are reported in Table 6 and Table 7, respectively. The histograms of GBW, Pd, and $m\varphi$ under process-only and mismatch-only Monte Carlo simulations are also reported in Figure 8 and Figure 9, respectively. As it can be observed, the power dissipated. Moreover, the current consumption and the GBW were characterized by an extremely small standard deviation, especially if compared with the same topology characterized without a control loop, confirming the extreme robustness achieved by the standard-cell-based OTA exploiting the proposed ASV-based quiescent current control approach.



(**a**) (**b**) (**c**)

Figure 8. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the standard-cell-based OTA with the proposed quiescent current control scheme under process-only Monte Carlo simulations.



(**a**) (**b**) (**c**)

Figure 9. Gain–bandwidth product (**a**), power consumption (**b**), and phase margin (**c**) of the standard-cell-based OTA with the proposed quiescent current control scheme under mismatch-only Monte Carlo simulations.

Table 6. Performance parameters of the standard-cell-based OTA with the proposed quiescent current control scheme under process-only Monte Carlo simulations.

	Mean	**Std Dev**
V_{off} [mV]	0.03	0.022
Pd [nW]	1.248	0.022
Itot [nA]	2.497	0.044
Av_d [dB]	51.22	1.90
$m\varphi$ [deg]	58.18	4.31
GBW [kHz]	33.41	2.03
SR_{avg} [V/ms]	31.49	10.48

Table 7. Performance parameters of the standard-cell-based OTA with the proposed quiescent current control scheme under mismatch-only Monte Carlo simulations.

	Mean	**Std Dev**
V_{off} [mV]	−0.9	15.82
Pd [nW]	1.32	0.14
Itot [nA]	2.62	0.27
Av_d [dB]	51.32	2.54
$m\varphi$ [deg]	58.32	7.30
GBW [kHz]	34.69	9.83
SR_{avg} [V/ms]	31.88	10.48

5. Conclusions

In most cases, the existing ways to implement analog building blocks from digital standard-cell libraries do not provide enough control over the quiescent operating point. This makes the same solutions vulnerable to significant fluctuations in performance when PVT conditions are changed. This research offered a technique for biasing through the development of ASV generators, which appears to be a workable way to create analog circuits based on standard cells that have output voltages and quiescent currents that are well defined. A fully synthesizable two-stage OTA was designed in a 180 nm CMOS process to illustrate the application of the proposed approach. Excellent stability of the GBW, power consumption, and phase margin of the OTA exploiting the proposed quiescent current control strategy were demonstrated by the simulation results. More specifically, the ratio between the mean value and the standard deviation ($\frac{\sigma}{\mu}$) of the GBW (Pd) obtained from process-only Monte Carlo simulations for the OTA designed with the proposed approach was about 0.06 (0.017). These values, when compared with the $\frac{\sigma}{\mu}$ values of the GBW (Pd) obtained from the conventional standard-cell-based OTA without ASVGs, which were 0.5 (0.53), confirm the dramatic reduction in the $\frac{\sigma}{\mu}$ of main performance parameters under process variations that was allowed by the proposed approach.

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Abbreviations

The following abbreviations are used in this manuscript:

ASV	Adaptive Supply Voltage
ASVG	Adaptive Supply Voltage Generator
DAC	Digital-to-Analog Converter
DIGOTA	Digital Operational Transconductance Amplifier
GBW	Gain–Bandwidth Product
IoT	Internet of Things
OTA	Operational Transconductance Amplifier
PSRR	Power Supply Rejection Ratio
PVT	Process, Supply Voltage, and Temperature
ULP	Ultra-Low Power
ULV	Ultra-Low Voltage

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