

Article

A 0.7 V, Ultra-Wideband Common Gate LNA with Feedback Body Bias Topology for Wireless Applications

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Abstract: An ultra-wideband (UWB) low noise amplifier (LNA) for 3.3–13.0 GHz wireless applications using 90 nm CMOS is proposed in this paper. The proposed LNA uses an improved common-gate (CG) topology utilizing feedback body biasing (FBB), which improves noise figure (NF) by a considerable amount. Parallel-series tuned LC network was used between the common-gate first stage and the cascoded common-source (CS) stage to achieve the maximum signal flow from CG to CS stage. Improved CS topology with a series inductor at the drain terminal in the second stage connected and cascoded CS third stage provides high power gain (S_{21}) and bandwidth enhancement throughout the complete UWB. A common-drain buffer stage at the output provides high output reflection coefficient (S_{22}). It achieves an average power gain (S_{21}) of 14.7 ± 0.5 dB with a noise figure (NF) of 3.0–3.7 dB. It has an input reflection coefficient (S_{11}) less than -11.7 dB for 3.3–13.0 GHz frequency and output reflection coefficient (S_{22}) of less than -10.6 dB with a very high reversion isolation (S_{12}) of less than -72.4 dB. It consumes only 5.2 mW from a 0.7 V power supply.

Keywords: common-gate; feedback body bias; low noise amplifier; low power; UWB; wireless communication

1. Introduction

The Federal Communications Commission (FCC), in 2002, offered a 3.1–10.6 GHz ultra-wideband frequency (UWB) range, for the implementation of very high data rate wireless communication links [1]. The FCC set an upper limit on highest power spectral density to -41.3 dBm/MHz over the 3.1–10.6 GHz frequency range, so that the newly designed wireless communication devices could not interfere with the wireless services existing in the same local area network [1–3]. This upper limit for power spectral density makes the UWB technology suitable for many interesting wireless applications, such as wireless personal area networks (WPAN), medical imaging, short-range radars for vehicles and wireless sensor nodes [4,5]. It gives reasons for low-power very-large scale integration (VLSI) design industries and researchers to develop low-power, low-noise, and reliable UWB radio-frequency integrated circuits (RFICs) for these applications. Moreover, continuous shrinking in complementary metal oxide semiconductor (CMOS) chip fabrication technologies and split manufacturing techniques in RF designs [6,7], makes it possible to design and fabricate RFICs on the nanometer scale [8,9].

LNA as a primary module of UWB wireless communication receiver requires designers to meet many challenges like 50Ω input matching, a low noise figure, flat gain, low power, and the receiver's

stability across the complete UWB frequency range [2,3,9]. Two frequently used UWB LNA topologies by many researchers are common-source (CS) [8,10–16] and common-gate (CG) [2–5,17] (Figure 1). The CS-topology is suitable to design LNAs for narrow and wide-band matching with high power gain (S_{21}). However, using the proper band-pass network, CS topologies can also be used for wideband LNA designs, but it degrades the gain and noise performance of the LNA. A common-source LNA with impedance feedback topology (Figure 1c) is also famous among some researchers [10–13,17]. However, the noise figure of a resistive feedback LNA is higher than that of CS topology. Distributed amplifiers (DA) (Figure 1d) are favored by some researchers to realize flat gain LNA for UWB [18,19]. The average power gain of DA is around 8–10 dB [18,19]. Active inductor-based input matching techniques (Figure 1e) can also be used for gain flatness in CG-topology [20]. However, due to the inclusion of an additional metal-oxide semiconductor (MOS) device used as an active inductor at the input, it increases NF as compared to traditional CG-LNA. For example, NF of the LNA proposed in [20] is greater than 4.5 dB.

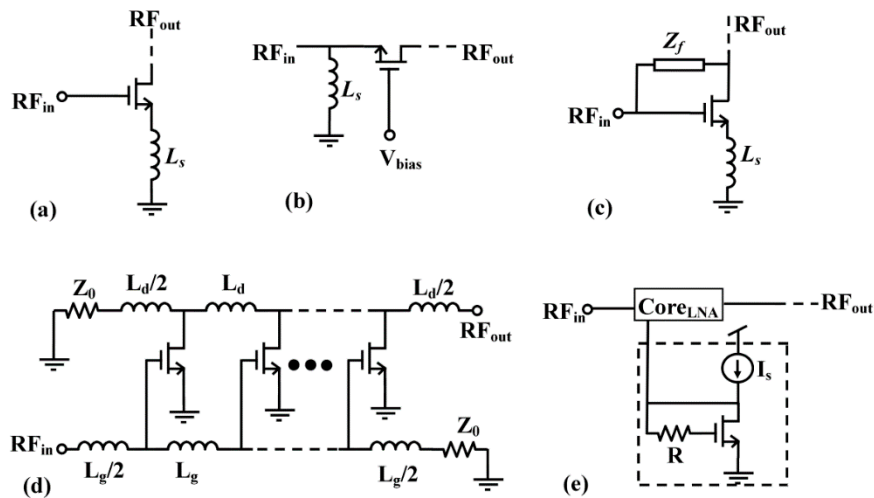


Figure 1. Basic LNA topologies: (a) Common source; (b) common gate; (c) CS with impedance feedback; (d) distributed LNA; (e) active inductor LNA.

This paper reports a design of a low-power LNA using CG feedback-body biased topology for an UWB frequency. A CG configuration provides a very simple technique for UWB input impedance matching by setting $1/g_m$ equal to $50\ \Omega$, where g_m is the transconductance of CG transistor. Implementation of feedback-body biasing for input CG transistor leads to the further decrease in the power supply (V_{dd}) due to the decrease in threshold voltage, which results from a decrease in power consumption. The advantage of a wideband input matching capability and utilizing the body-biasing to decrease power consumption brought our attention to the traditional CG LNA topologies for the 3.1–10.6 GHz UWB frequency. This paper is organized as follows: Section 2 describes the proposed LNA design methodology for the proposed LNA. In Section 3, the results of the proposed LNA circuit and comparison with the previous work are presented. Finally, Section 4 concludes this paper.

2. Operational Principle and Circuit Implementation

The circuit diagram of the proposed UWB LNA shown in Figure 2 consists of four stages. At the input side, a common-gate cascode topology has been used to achieve wideband input matching. The source inductor (L_{s1}) and gate-source parasitic capacitance (C_{gs1}) dictates the input resonance frequency of the CG-stage. The transistor M_1 has been configured to feedback-body biasing through the feedback resistor R_1 connected to drain terminal of M_2 , to boost-up the noise figure performance and the power consumption, whereas the transistor M_2 is cascoded with M_1 to enhance the gain of the first stage. The CG first stage has been cascoded with two stages of common source configuration using transistors M_3 and M_4 respectively, to enhance the gain and bandwidth proposed for UWB LNA.

In first CS stage, L_{d3} serves as a series peaking inductor, which increases the gain flatness. At the output side, a buffer stage has been used for enhancing the output matching (S_{22}) performance of the proposed LNA. The output of the transistor is tuned by a parallel LC resonating circuit, in which an inductor (L_{d4}) resonates with the total gate-drain parasitic capacitances (i.e., $C_{gd4} + C_{gd5}$) of the transistors M_4 and M_5 , respectively. The output is taken from the source terminal of transistor M_5 whereas M_6 behaves as a saturated load.

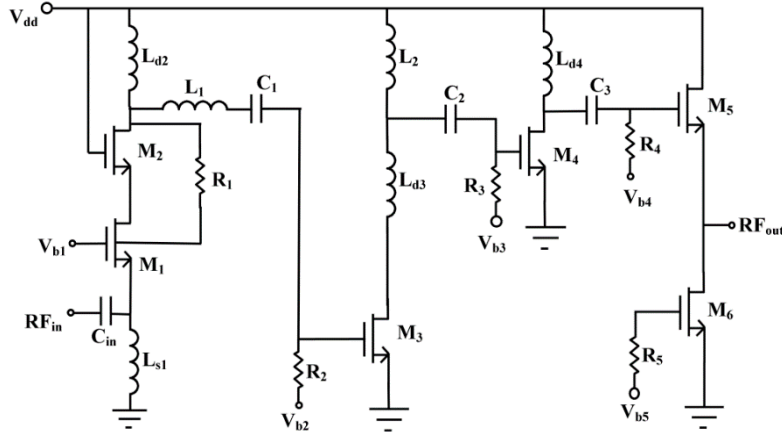


Figure 2. Circuit diagram of the proposed UWB LNA.

The capacitors C_{in} , C_1 , C_2 and C_3 are the coupling capacitors, whereas the resistors R_2 to R_5 are used as biasing resistors. Maximum power flow from receiver end to the load end is one of the important requirements for an LNA design, and for this purpose, a parallel to series LC network has been used between common gate first stage's output and the input of second stage. In this, drain inductor (L_{d2}) and gate-drain parasitic capacitance (C_{gd2}) of M_2 are figured as parallel resonance circuit resonating at $1/\sqrt{L_{d2}C_{gd2}}$, whereas inductor L_1 and the capacitance C_1 are used to form series resonance circuit resonating at $1/\sqrt{L_1C_1}$. A frequency response equivalent to a band-pass filter can be achieved when parallel LC tank resonates at the same centerfrequency at which series LC tank does. This condition can be achieved when $(L_{d2}C_{gd2})^{-\frac{1}{2}} = (L_1C_1)^{-\frac{1}{2}}$, i.e., $L_{d2}C_{gd2} = L_1C_1$. Table 1 provides the parameter values for the proposed LNA design.

Table 1. Parameters for the proposed LNA.

Transistors W (μm) \times L (μm)	Inductance (nH)	Resistance (K Ω)	Capacitance (pF)
M_1 30 \times 0.09	L_{s1} 5.5	R_1 0.5	C_{in} 1.0
M_2 45 \times 0.09	L_{d2} 8.5	R_2 5.0	C_1 1.0
M_3 35 \times 0.09	L_1 5.0	R_3 5.0	C_2 1.5
M_4 18 \times 0.09	L_{d3} 10.0	R_4 0.5	C_3 1.5
M_5 21 \times 0.09	L_2 8.5	R_5 5.0	
M_6 35 \times 0.09	L_{d4} 7.1		

2.1. Forward Body Biasing to Decrease Power Consumption

Due to the cascode architecture of transistors M_1 and M_2 , it demands high V_{dd} supply. This limits the design of LNA to low power consumption. To mitigate this problem, the forward-body bias technique has been implemented in this paper, to operate the proposed UWB LNA at lower V_{dd} supply of 0.7 V. The transistor M_1 is the key-element in deciding the input impedance matching and noise figure of the complete LNA circuit, and to isolate it from transistor M_2 , the forward-body bias technique has been applied only to M_1 . This provides more degrees of freedom in finalizing the device dimensions

of M_2 , to keep transconductance (g_{m2}) constant and to provide constant current to primary amplifying transistor M_1 [19–21]. The threshold voltage V_{th} of the transistor M_1 can be characterized by:

$$V_{th} = V_{t0} + \gamma_0(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}) \quad (1)$$

where V_{t0} is the threshold voltage for zero body-to-source voltage (i.e., $V_{BS} = 0$), γ_0 is a constant that describes body-effect and usually has a value in the range of 0.3–0.4 V and ϕ_f is the bulk Fermi-potential. It is clear from Equation (1) that applying a forward voltage to body terminal will reduce the threshold voltage of MOS device which in turn helps in reducing the power consumption.

2.2. Frequency Response of S_{11} and S_{22}

In this section, the proposed LNA design has been analyzed for the frequency response of the input reflection coefficient (S_{11}) and the output reflection coefficient (S_{22}). The approximate expressions for S_{11} and S_{22} have been derived here using the small-signal model of the proposed LNA shown in Figure 3, where the effect of the input capacitor (C_{in}) on the overall input impedance (Z_{in}) has been neglected.

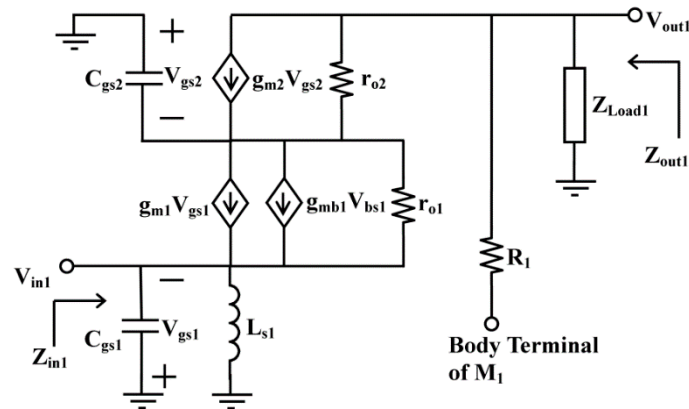


Figure 3. Small signal model of stage-1.

After using fundamental network theorems, the input impedance of the proposed LNA design can be obtained as:

$$Z_{in}(\omega) \approx \left(\frac{j\omega L_{s1}}{1 - \omega^2 L_{s1} C_{gs1}} \right) || Z_X(\omega) = Z_{s1}(\omega) || Z_X(\omega) \quad (2)$$

where $Z_{s1}(\omega)$ is impedance of parallel LC tank and $Z_X(\omega)$ can be expressed as:

$$Z_X(\omega) = \frac{\left[r_{o1}(1 + g_{m2}r_{o2} + j\omega C_{gs2}(r_{o2} + Z_{Load1}(\omega)) + g_{mb1}Z_{Load1}(\omega)) + r_{o2} + Z_{Load1}(\omega)(1 + g_{mb1}r_{o1}g_{m2}r_{o2}) \right]}{[1 + r_{o1}(g_{m1} + g_{mb1})][1 + g_{m2}r_{o2} + j\omega C_{gs2}(r_{o2} + Z_{Load1}(\omega))]} \quad (3)$$

where g_{m1} , g_{m2} are transconductances and $1/r_{o1}$, $1/r_{o2}$ are drain-to-source channel conductance of M_1 and M_2 respectively. Back-gate transconductance of M_1 is denoted by g_{mb1} and Z_{Load1} is the total load impedance connected at the drain of transistor M_2 . In Equation (3), assuming $r_{o1} \gg 1$ and $r_{o2} \gg 1$, then at the input parallel resonance condition set up by L_{s1} and C_{gs1} and the input impedance $Z_{in}(\omega)$ can be approximated as:

$$Z_{in}(\omega) \approx \frac{g_{m2} + j\omega C_{gs2} + Z_{Load1}(\omega)g_{mb1}g_{m2}}{(g_{m1} + g_{mb1})(g_{m2} + j\omega C_{gs2})} \quad (4)$$

The input reflection coefficient (S_{11}) can be expressed as:

$$S_{11} = (Z_{in}(\omega) - R_s) \times (Z_{in}(\omega) + R_s)^{-1} \quad (5)$$

In general, $S_{11} \leq -10$ dB is an essential requirement for the entire frequency of interest. From Equations (4) and (5) we have:

$$S_{11} \text{ dB} = 20 \log_{10} \sqrt{\frac{(g_{m2} - R_s g_{m2}(g_{m1} + g_{mb1}))^2 + |j\omega C_{gs2}(1 - R_s(g_{m1} + g_{mb1})) + Z_{Load1}(\omega)g_{mb1}g_{m2}|^2}{(g_{m2} + R_s g_{m2}(g_{m1} + g_{mb1}))^2 + |j\omega C_{gs2}(1 + R_s(g_{m1} + g_{mb1})) + Z_{Load1}(\omega)g_{mb1}g_{m2}|^2}} \leq -10 \text{ dB} \quad (6)$$

For the output reflection coefficient (S_{22}), output impedance estimated by looking into the output buffer transistor M_5 is keeping input of the buffer stage as zero. The output impedance of the proposed LNA can be expressed as:

$$\begin{aligned} Z_{out}(\omega) &\approx \frac{1 + j\omega Z_4(\omega)C_{gs5}}{g_{m5} + j\omega C_{gs5}} \| r_{o5} \| r_{o6} \\ &\approx \frac{1 + j\omega Z_4(\omega)C_{gs5}}{g_{m5} + j\omega C_{gs5}} \end{aligned} \quad (7)$$

where $Z_4(\omega)$ is the impedance of the LC tank formed by L_{d4} with $(C_{gd4} + C_{gd5})$. C_{gd4} is the gate-to-drain parasitic capacitance of transistor M_4 , whereas C_{gs5} and g_{m5} are the gate-source parasitic capacitance and transconductance of the transistor M_5 , respectively. The output reflection coefficient (S_{22}) is given by:

$$S_{22} = \frac{Z_{out}(\omega) - R_s}{Z_{out}(\omega) + R_s} \quad (8)$$

2.3. Noise Figure Analysis

The noise equivalent model of the proposed UWB is shown in Figure 4. The input CG transistor M_1 plays a significant role in overall the noise figure of the LNA while the noise contribution of cascoded transistor M_2 and other successive stages is very small. In Figure 4, the main noise sources included are: the thermal noise due to signal source resistance R_s represented by $\overline{V_{n,Rs}^2} = 4kTR_s\Delta f$, the gate-induced noise of M_1 represented by $\overline{i_{n,g1}^2} = 4kT\delta g_{g1}\Delta f$ and the channel-induced thermal noise of M_1 represented by $\overline{i_{n,d1}^2} = 4kT\gamma g_{d0}\Delta f$ where, k is the Boltzmann constant, T is the temperature in Kelvin, Δf is noise bandwidth, δ is the coefficient of gate-induced noise and γ is the coefficient of channel-induced thermal noise. The g_g and g_{d0} are given by $g_g = (\omega^2 C_{gs1}^2) / (5g_{d0})$ and $g_{d0} = g_{m1} / \alpha$ respectively, where g_g is the equivalent gate conductance and g_{d0} is the zero-bias drain conduction of transistor M_1 . Another important noise source of MOS transistor of noise due to the bulk-resistance (R_B) given by $\overline{i_{nb1}^2} = 4kTR_B g_{mb1}^2 \Delta f$ [22]. This bulk-resistance is distributive in nature, which is very difficult of analyze quantitatively [23]. Furthermore, this noise is also not correlated with the gate induced noise and the channel induced thermal noise. However, the effect of noise due to bulk resistance can be decreased by decreasing the value of g_{mb1} and is clear from the expression of g_{mb1} given by:

$$g_{mb1} = \frac{\partial I_D}{\partial V_{BS}} = g_m \cdot \frac{\gamma_0}{2\sqrt{|2\phi_f|} + V_{SB}} \quad (9)$$

This will be possible if we apply a forward voltage to the body terminal of M_1 . The correlation coefficient c between induced gate noise ($\overline{i_{n,g1}^2}$) and channel induced thermal noise ($\overline{i_{n,d1}^2}$) is also ignored here for simplifying our noise figure analysis. The noise figure of the proposed LNA can be expressed as:

$$NF = 1 + \frac{\overline{V_{n,out,g1}^2} + \overline{V_{n,out,d1}^2}}{\overline{V_{n,out,Rs}^2}} \quad (10)$$

where $\overline{V_{n,out,Rs}^2}$, $\overline{V_{n,out,g1}^2}$ and $\overline{V_{n,out,d1}^2}$ are the rms output noise voltages at the drain terminal of M_2 due to $\overline{V_{n,Rs}^2}$, $\overline{i_{n,g1}^2}$ and $\overline{i_{n,d1}^2}$, respectively. The $\overline{V_{n,out,Rs}^2}$, $\overline{V_{n,out,g1}^2}$ and $\overline{V_{n,out,d1}^2}$ can be expressed as:

$$\overline{V_{n,out,Rs}^2} = \overline{V_{n,Rs}^2} \times \frac{g_{m2}^2 (g_{m1} + g_{mb1})^2 |Z_{s1}(\omega) \cdot Z_{Load1}(\omega)|^2}{\left| (g_{m2} + j\omega C_{gs2})(R_s + Z_{s1}(\omega) + R_s Z_{s1}(\omega)(g_{m1} + g_{mb1})) + g_{mb1} g_{m2} Z_{Load1}(\omega)(R_s + Z_{s1}(\omega)) \right|^2}, \quad (11)$$

$$\overline{V_{n,out,g1}^2} = \frac{\alpha \delta \omega^2 C_{gs1}^2 R_s}{5g_{m1}} \times \overline{V_{n,out,Rs}^2}, \quad (12)$$

and:

$$\overline{V_{n,out,d1}^2} = \frac{\gamma g_{m1}}{\alpha R_s (g_{m1} + g_{mb1})^2} \left[1 + \frac{R_s^2}{|Z_{s1}(\omega)|^2} \right] \times \overline{V_{n,out,Rs}^2} \quad (13)$$

Respectively. Substituting the Equations (11)–(13) in Equation (10), we get the noise figure expression of the proposed UWB LNA as:

$$NF \approx 1 + \frac{\alpha \delta \omega^2 C_{gs1}^2 R_s}{5g_{m1}} + \frac{\gamma g_{m1}}{\alpha R_s (g_{m1} + g_{mb1})^2} \left[1 + \frac{R_s^2}{|Z_{s1}(\omega)|^2} \right] \quad (14)$$

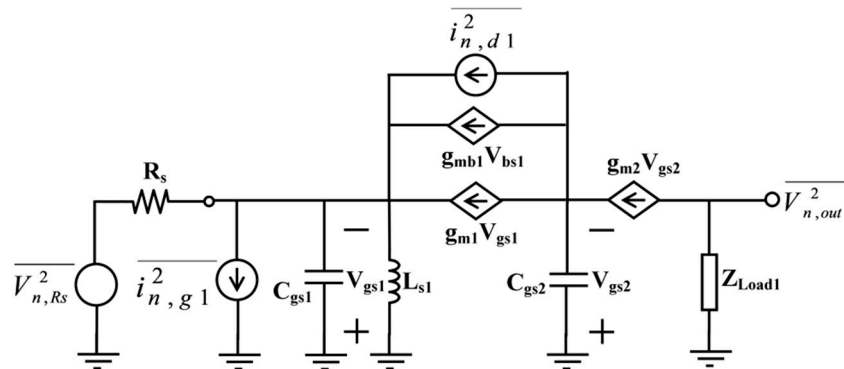


Figure 4. Simplified noise-model of the first stage of the proposed UWB LNA (excluding the noise sources of M_2).

3. Simulation Results

The proposed LNA is designed and simulated using a 90 nm CMOS process for 3–14 GHz UWB frequency range. The simulation results for S -parameters, noise figure and stability of the proposed FBB UWB LNA are shown in Figure 5. It can be observed from Figure 5a that the proposed LNA UWB input matching with S_{11} has less than -10.6 dB for a frequency range of 3.3 GHz to 13.0 GHz. For this purpose, the transconductance (g_{m1}) of M_1 was set to 26 mS so that $1/g_{m1} \approx 38.4 \Omega$, so that the difference from the 50Ω antenna impedance will be contributed to by the successive stages in the LNA architecture. Due to the CG cascode topology the proposed UWB LNA has a very high reverse isolation (S_{12}) of less than -72.4 dB was achieved throughout the complete UWB range (Figure 5b).

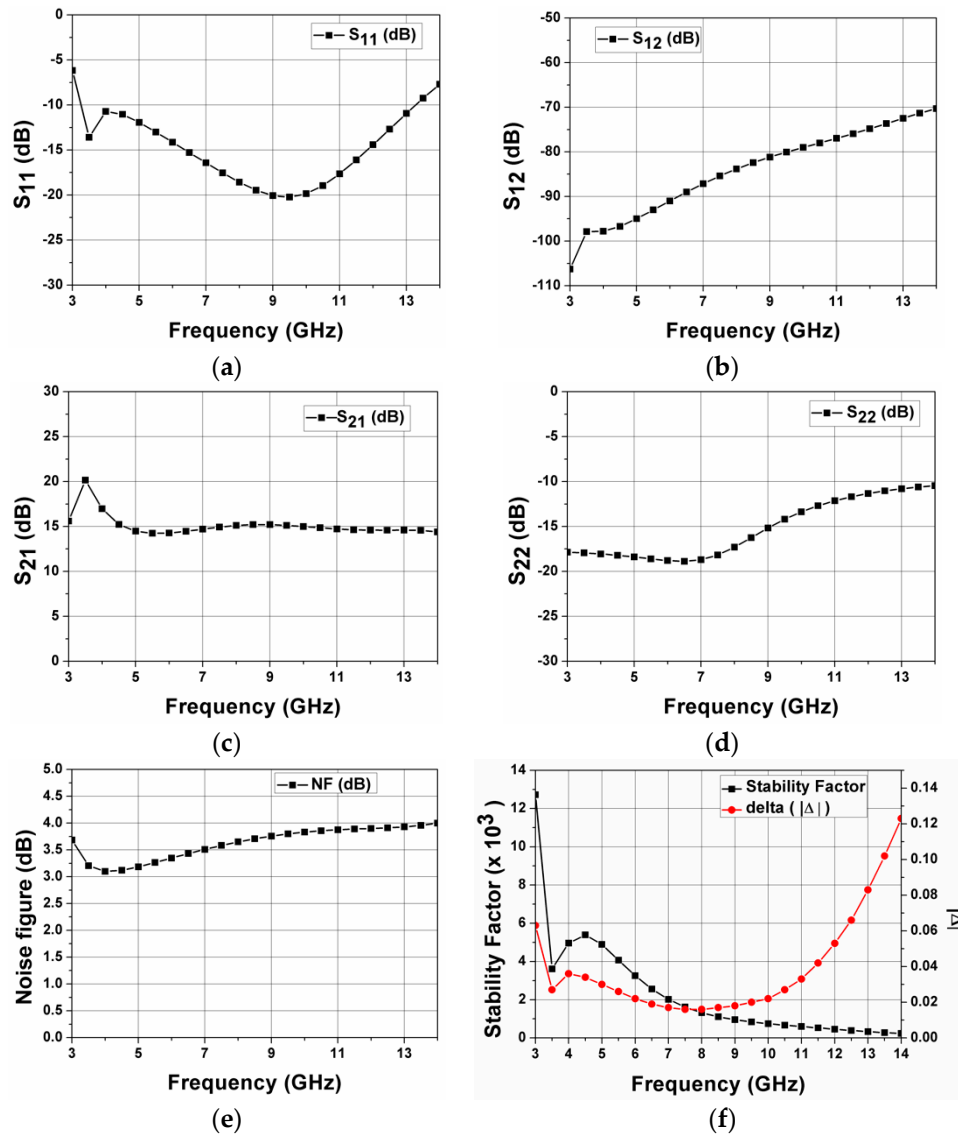


Figure 5. (a) S_{11} vs. frequency, (b) S_{12} vs. frequency, (c) S_{21} vs. frequency, (d) S_{22} vs. frequency, (e) NF vs. frequency, and (f) stability factor (K) and magnitude of delta ($|\Delta|$) vs. frequency.

The frequency response for power gain (S_{21}) is shown in Figure 5c and it can be observed from the figure that S_{21} was greater than 14.2 dB throughout the frequency range of 3.0 GHz to 13.0 GHz. The proposed LNA shows a flat S_{21} for 15.7 ± 0.5 dB for a frequency range of 4.5 GHz to 13.0 GHz whereas, the output reflection coefficient (S_{22}) was less than -10.8 dB for the 3.0 GHz to 13.0 GHz frequency range (Figure 5d). The noise figure plot of the LNA proposed is shown in Figure 5e and it can be observed from the noise figure versus frequency plot, NF was ranging from 3.0 dB to 4.0 dB for the complete UWB frequency range.

In extension to the parameters discussed earlier for the designing of LNA, another significant parameter to be considered is the Stability factor (K). The absolute stability is an essential requirement for the designed LNA. The stability factor can be expressed as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \quad (15)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (16)$$

The stability factor (K) should be greater than 1 and the delta ($|\Delta|$) should be less than 1 for an unconditional stability of a system throughout the complete UWB frequency range. Figure 5f shows the stability of the proposed LNA design, where minimum value obtained for K was equal to 330 at 13.0 GHz, which is far greater than unity and the value of delta ($|\Delta|$) at less than 0.12.

To evaluate the effect of feedback body bias technique on noise figure, power gain and input reflection coefficient, the proposed LNA has been simulated with feedback body bias at V_{dd} supply of 0.7 V and without body biasing at V_{dd} supply of 0.7 V and 0.9 V. It can be observed from Figure 6 that noise figure, power gain and input matching performance of the proposed LNA was improved with a CG FBB topology with the advantage of requirement of lower V_{dd} supply.

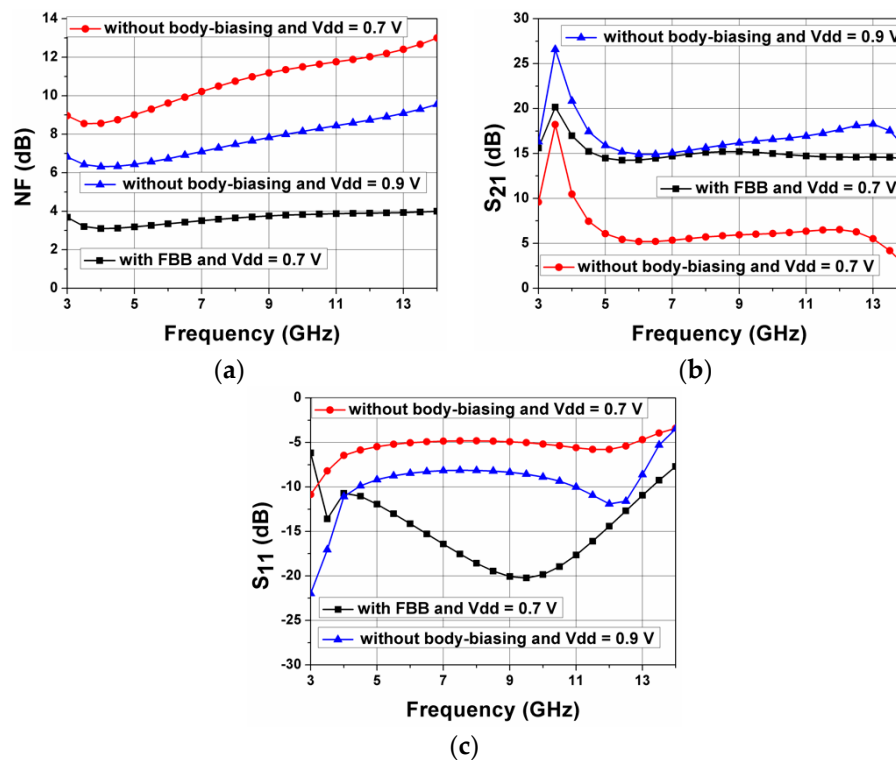


Figure 6. Frequency response with feedback body bias and without body-bias. (a) NF vs. frequency, (b) S21 vs. frequency, and (c) S11 vs. frequency.

Another significant parameter to be considered is linearity. The input signal received from the antenna must be linearly amplified by the designed LNA. As LNAs are usually biased at a very low voltage, at this low voltage the linearity survives due to transconductance (g_m) and drain-conductance (g_{ds}) nonlinearities of the MOS device. Linearity of the proposed LNA has been analyzed graphically in terms of a 1-dB compression point ($P1dB$), and a third order intercept point ($IIP3$) for which input power was swept from -40 dBm to -10 dBm. It can be observed from Figure 7a that $P1dB$ at the fundamental frequency of 7.0 GHz was -23.0 dBm. A two tone test was performed at a center frequency of 7.0 GHz that gave two tones at $f_1 = 6.995$ GHz and $f_2 = 7.005$ GHz with frequency spacing of 10 MHz to find $IIP3$. Extrapolating the fundamental signal and third order signal outputs and finding out the intersection of the two gives the approximate value of $IIP3$. It can be observed from Figure 7b that $IIP3$ of the proposed LNA was -19 dBm.

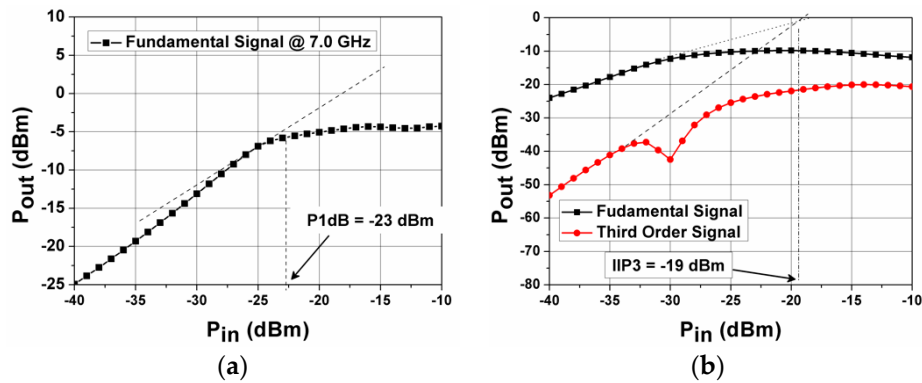


Figure 7. (a) 1-dB compression point (P_{1dB}), and (b) Input third order intercept point (IIP3).

The designed UWB LNA must be stable against temperature variations. To ensure this, the designed LNA was simulated at nominal, slow-slow (SS), and fast-fast (FF) process corners and at different temperatures of -25° , 25° and 50° Celsius (Figure 8). It can be observed from Figure 8a,b that the feedback of the proposed UWB LNA had a minimum NF that varied from 2.87–3.75 dB to 3.0–4.0 dB at the FF and SS corners respectively, and it varied from 3.1–3.6 dB to 3.3–4.3 dB for -25° C to -50° C temperature variations, respectively. Figure 8c,d shows the frequency responses of the input reflection coefficient against process and temperature variations. It can be observed that S_{11} was less -9.0 dB for 4–13 GHz for all process corners, and was less than 9.1 dB for 5–13 GHz for the temperature range of -25° C to 50° C. The power gain frequency response of the proposed LNA is shown in Figure 8e–f, which confirmed the robustness of the proposed UWB LNA against temperature variations.

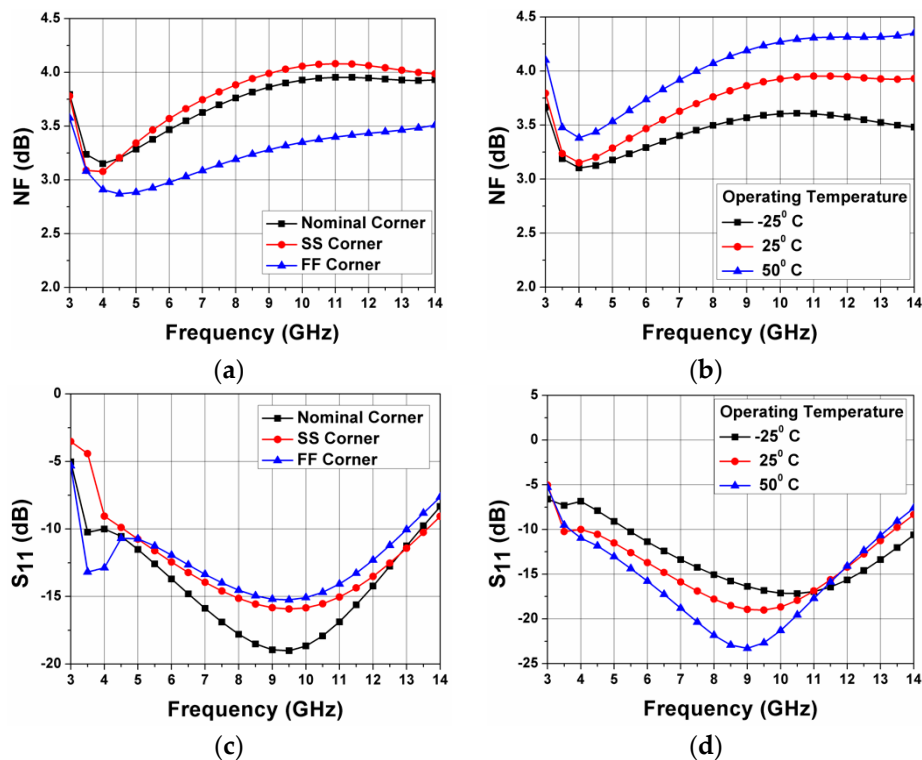


Figure 8. Cont.

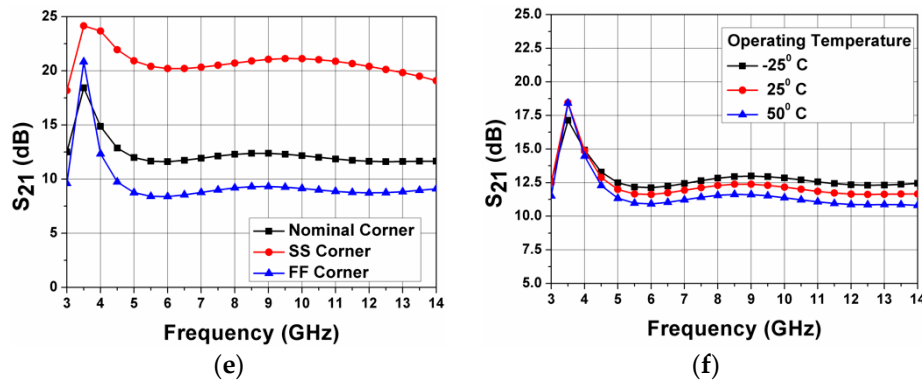


Figure 8. Simulation results for process and temperature variations. (a,b) NF vs. frequency, (c,d) S_{11} vs. frequency, and (e,f) S_{21} vs. frequency.

Results in this study were obtained with theoretical calculations and simulations with standard model files in 90 nm technology. The chip-layout of the proposed LNA is shown in Figure 9, which is designed using the Cadence Layout tool using a 90 nm CMOS process. The dimensions of all the inductors have been calculated using the expression from Mohan et al. (1999) [24]. All the inductors have been designed using metal-1 layer with a turn width and turn spacing of 5 μm and an outer diameter (D_{out}) of 300 μm for each. As the designed LNA is required to achieve a large bandwidth, the Q-factor of the inductors used in the proposed LNA was very small and ranges from 0.6–1.5. The capacitors C_{in} and C_1 were designed using metal-insulator-metal using metal-2 and metal-3 layers. The capacitors C_2 and C_3 were designed using a N-type MOS device, whereas the N-diffusion resistors were used to decrease the layout area. The chip layout occupied 1.318 mm^2 of area. In order to evaluate and compare the overall performance of the proposed UWB LNA with previous work, a figure-of-merit (FOM) has been evaluated. The figure-of-merit can be obtained as [14,22,23]:

$$FOM[\text{GHz}/\text{mW}] = \frac{|S_{21}|_{\text{abs}} \times BW_{\text{GHz}}}{(F - 1) \times P_{\text{mW}}} \quad (17)$$

where $|S_{21}|_{\text{abs}}$ is the absolute value of S_{21} , BW is the 3-dB bandwidth measured in GHz, F is noise factor and P_{mW} is the power consumption in mW.

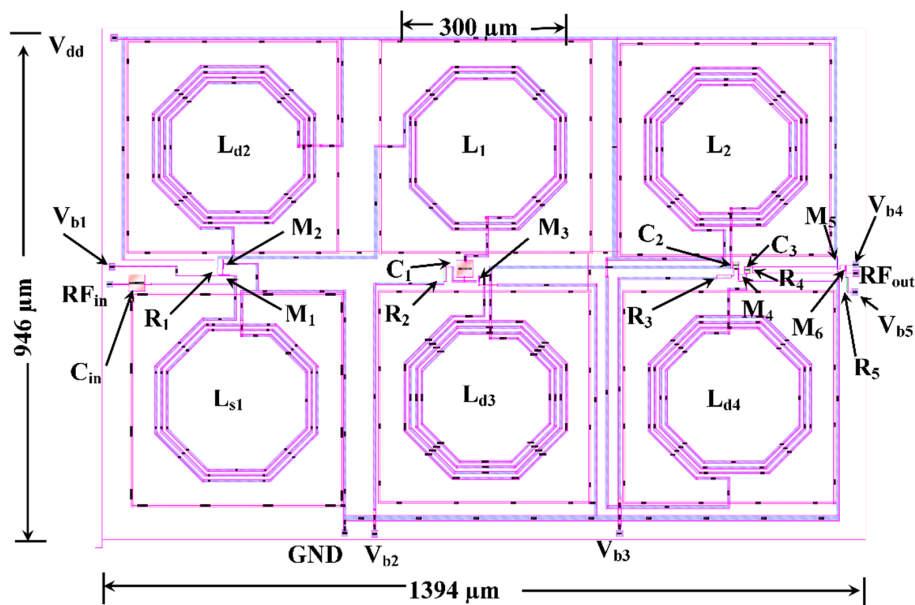


Figure 9. Chip Layout of the proposed FBB UWB LNA.

The simulation results of the proposed UWB LNA were compared with the previous published work from a wide literature in Table 2. Comparison mainly focused on noise figure (NF), input reflection coefficient (S_{11}), output reflection coefficient (S_{22}), power gain (S_{21}) and power consumption for 3.1–10.6 GHz UWB frequency. The LNAs implemented in References [8,23,25] uses common-source resistive feedback topology for wideband input matching, but the noise figure was in 3.0–5.3 dB range and consumed more power as compared to the LNA proposed in this paper. A noise cancelling technique was utilized in References [14,23] with a high power consumption of 9.97 mW and 23.23 mW respectively. CS with an FBB technique was used in References [20,26,27], however, the power consumed by the LNA proposed in References [20,26] was greater than 9 mW and 13.0 mW, respectively. Due to the use of the small power supply LNA proposed in References [27] it consumed less power but had S_{11} of ≤ -5 dB. It can be observed from Table 2 that the proposed LNA design had better overall performance in terms of the noise figure, S_{11} , S_{21} , S_{22} , bandwidth and the power consumption.

Table 2. Comparison of the simulation results of proposed LNA with previously published work.

Ref. & Year	Topology	Tech (nm)	V_{dd} (V)	BW (GHz)	S_{11} (dB)	S_{21} (dB)	S_{22} (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FOM ₁
This work ^s	CG Feedback Body Bias	90	0.7	3.3–13.0	< -10.6	14.7 ± 0.5 @ 4.5–13.0 GHz	< -10.8	3.0 ± 0.5	-19 @ 7.0 GHz	5.2	8.54
[10], 2010 ^m	CS-resistive feedback	90	1.2	3.1–10.6	< -14.1	10.4 ± 0.2 *, 10.68 ^{\$}	-	3.075 ± 0.155	+4	21.6	-
[28], 2011 ^m	Current-reused	90	1.2	2.6–10.2	< -9	12.5 ^{\$}		3–7	-	7.2	-
[16], 2008 ^m	CS-resistive feedback	90	1.2	0.2–9	< -10	10	-	4.2 [#]	-8	20	-
[29], 2013 ^s	CS Forward Body Bias	130	0.6	3.1–10.6	≤ -5	21 ^{\$}	≤ -10.6	1.0–3.9	+4.56 @ 6.0 GHz	4.1	-
[30], 2015 ^m	CS Forward Body Bias	130	1.0	3.0–10.0	≤ -11.4	12.1 ^{\$}	≤ 11.7	3.04–3.48	-6.6 @ 6.0 GHz	13.0	-
[17], 2015 ^s	Noise cancelling	130	1.3	2.3–9.37 ^a	≤ -8	10.3 ^{\$}	≤ -8	3.68–9.2	-4 @ 4.5 GHz	9.97	5.71
[27], 2013 ^m	CS Resistive Termination	180	1.0	3–5.6 ^a	≤ -9 @ 3–11 GHz	9 ^a	≤ -8 @ 3–7.5 GHz	4.6–5.3 ^a	+2 @ 5.3 GHz	9.0	-
[22], 2015 ^L	CS Forward Body Bias	180	1.5	3.1–10.6	< -10.6	14.4 ± 1.4	< -12.1	2.2–3.2	-6.0	9.0	-
[25], 2013 ^s	Common Gate	180	1.2	3.1–10.6	< -5.5	12.75 ± 0.83	< -7	2.5–3.7	-8.2 @ 5 GHz	12.14	12.58
[26], 2018 ^s	Noise cancelling	180	1.8	3–12	< -10	19.24–20.24	-	1.72–1.99		23.23	7.1
[31], 2008 ^s	Forward Body Bias	180	0.6	5	< -8	14.1	-	3.65	-17.1	1.68	-

^s Simulation results, ^m measurement results, ^L Layout data, ^a 3dB BW, * average value, ^{\$} max value, [#] minimum.

4. Conclusions

A low power UWB LNA was proposed in this paper for the UWB frequency range. The proposed LNA was designed and simulated using a 90nm CMOS process and implemented using common-gate cascade topology, with a feedback body biasing technique. Drain to body feedback was implemented using a resistor of 0.5 K Ω between the body terminal of M_1 and the drain of M_2 to alter the noise figure and power consumption. Detailed S_{11} , S_{22} and noise figure analysis was also provided to support the simulation results of the proposed LNA. The proposed LNA achieved a flat power gain (S_{21}) of 14.7 ± 0.5 dB for 4.5–13.0 GHz and noise figure of 3.0–4.0 dB. An output reflection coefficient of < -10.8 dB was achieved throughout the complete UWB range with a very small power consumption of 5.2 mW, including the output buffer stage and has a chip-layout area of 1.318 mm², which makes the proposed LNA design a good candidate for low power and low noise wireless applications.

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