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Analytical Performance of the Threshold Voltage and Subthreshold Swing of CSDG MOSFET

Uchechukwu A. Maduagwu * and Viranjay M. Srivastava *

Department of Electronic Engineering, Howard College, University of KwaZulu-Natal,
Durban 4041, South Africa
* Correspondence: maduagwuu@gmail.com (U.A.M.); viranjay@ieee.org (V.M.S.)

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Abstract: In this research work, the threshold voltage and subthreshold swing of cylindrical surrounding double-gate (CSDG) MOSFET have been analyzed. These analyses are based on the analytical solution of 2D Poisson equation using evanescent-mode analysis (EMA). This EMA provides the better approach in solving the 2D Poisson equation by considering the oxide and Silicon regions as a two-dimensional problem, to produce physically consistent results with device simulation for better device performance. Unlike other models such as polynomial exponential and parabolic potential approximation (PPA) which consider the oxide and silicon as one-dimensional problem. Using the EMA, the 2D Poisson equation is decoupled into 1D Poisson equation which represent the long channel potential and 2D Laplace equation describing the impacts of short channel effects (SCEs) in the channel potential. Furthermore, the derived channel potential close-form expression is extended to determine the threshold voltage and subthreshold behavior of the proposed CSDG MOSFET device. This model has been evaluated with various device parameters such as radii Silicon film thickness, gate oxide thickness, and the channel length to analyze the behavior of the short channel effects in the proposed CSDG MOSFET. The accuracy of the derived expressions have been validated with the mathematical and numerical simulation.

Keywords: CSDG MOSFET; short channel effects; channel engineering; DG MOSFET; subthreshold swing; microelectronics; nanotechnology; VLSI

1. Introduction

The downscale of the conventional MOSFETs devices to nanoscale regime has been the driving force of the semiconductor industry [1–3]. The main objective behind the transistor scaling is to enhance device performance, speed, low operating power, and packing density of the IC [4,5]. However, the downscaling of the device has led to problems of short channel effects (SCEs), such as threshold voltage roll-off, degradation of the subthreshold threshold swing, and subthreshold leakage current [6–9]. To overcome this problem several device structures has been proposed. Double gate structures [10–12] introduce the concept of volume inversion leading to higher current, better scalability, and increased conductance than conventional MOSFETs, but its use is limited based on the cost of production and process complexity.

In order to overcome these shortcomings of cost of production and process complexity, several novel geometric structures have been proposed. One of such structures is a three-dimensional cylindrical surrounding-gate (CSG) MOSFET [13–17]. The surrounding gate on the silicon pillar provides better coupling and its fabrication is less complex compared to DG MOSFET [18]. Additionally, CSG MOSFETs poses a better immunity to SCEs than conventional single gate MOSFETs and DG MOSFETs [19,20]. The most enhancing feature of the CSG MOSFET when compared to other novel structures, like single gate, pi gate, and double gate, is its geometric structure. This device structure

increases the packing density, and most importantly leads to better controllability of the gate over the channel [17,21]. The gate control results to enhancement of the subthreshold characteristics and greater immunity to SCEs. However, in terms of current drive the CSG MOSFETs have lesser current compared with the DG MOSFET, hence, its extensive use is limited for high performance application [22]. Thus, there is need to improve on the geometric structure of the CSG MOSFET to enhance the current drive, the gate control over the channel and further improve the SCEs immunity at the nanoscale regime.

A novel structure, the cylindrical surrounding double gate (CSDG) MOSFET, was proposed by Srivastava et al. [12]. The geometry is similar to that of the CSG MOSFET with an internal core gate. The core gate enhances the channel control and improves the SCEs immunity. Additionally, the device allows for higher packing density and higher volume inversion than DG MOSFETs and CSG MOSFETs [23,24]. The explicit charge model based on the unified charge model was carried out by Srivastava et al. [25,26]. The authors analyzed the channel current for the novel structure to be higher than the single, DG MOSFET, and CSG MOSFET. However, the authors did not consider the subthreshold regime. Verma et al. [27] worked on the subthreshold regime of the CSDG MOSFET in which only the threshold voltage was analyzed.

The proposed CSDG MOSFET is designed on a hollow concentric cylindrical structure in which a simple analytical channel potential model has been derived at subthreshold regime. The 2D Poisson equation is solved with the EMA as a boundary valued problem to obtain the minimum surface potential. The minimum surface potential is further extended in the derivation of the threshold voltage model, subthreshold current, and subthreshold swing of the device structure. Its performance is investigated with the device parameters. However, we neglected the quantum mechanical effect by assuming a minimum silicon body thickness of 5 nm [28]. This paper is organized as follows: The structure of CSDG MOSFET with the boundary conditions and modelling of the minimum surface potential with EMA is presented in Section 2. The threshold voltage model for the proposed CSDG MOSFET structure is derived using the minimum surface potential in Section 3. The subthreshold swing is derived in the Section 4. The results have been discussed in the Section 5. Finally, Section 6 concludes the work and recommends future aspects.

2. Structure of CSDG MOSFET and Potential Distribution Model using EMA Model

2.1. CSDG MOSFET Structure

The CSDG MOSFET is an extended version of DG MOSFET and CSG MOSFET in terms of form factor and current drive, respectively. The DG MOSFET has two gates (blue color), the oxides (yellow color), the drain/source (red color) and a silicon substrate (P, green color). When this DG MOSFET is rotated with respect to the reference point, the first gate (G_1) forms the internal radius ($r = a$) with a circular thin oxide to immune the effect of SCEs. The second gate (G_2) forms the external radius ($r = b$) with circular thin oxide, forming a hollow concentric cylinder [29]. Between the oxides is the silicon substrate, while the extension forms the source and drain part of the cylinder as shown in the Figure 1.

The internal and external gates of the CSDG MOSFET can be biased either separately or simultaneously to form separate inversion or volume inversion, respectively. However, the simultaneous biasing of the CSDG MOSFET is usually preferred due to higher current drive (volume inversion). Assuming the gate of an n-channel CSDG MOSFET are positively biased simultaneous. Below threshold voltage, the minority carrier electrons are attracted towards the oxide-silicon interface forming weak inversion. As the biasing voltage exceeds the threshold voltage, the onset of strong inversion occurs in CSDG MOSFET in similar manner with traditional MOSFET [30]. Both biasing gates voltage forms the internal and external channel of the device structure at subthreshold region. However, above threshold voltage the two channels contribute to higher current drive know as volume inversion.
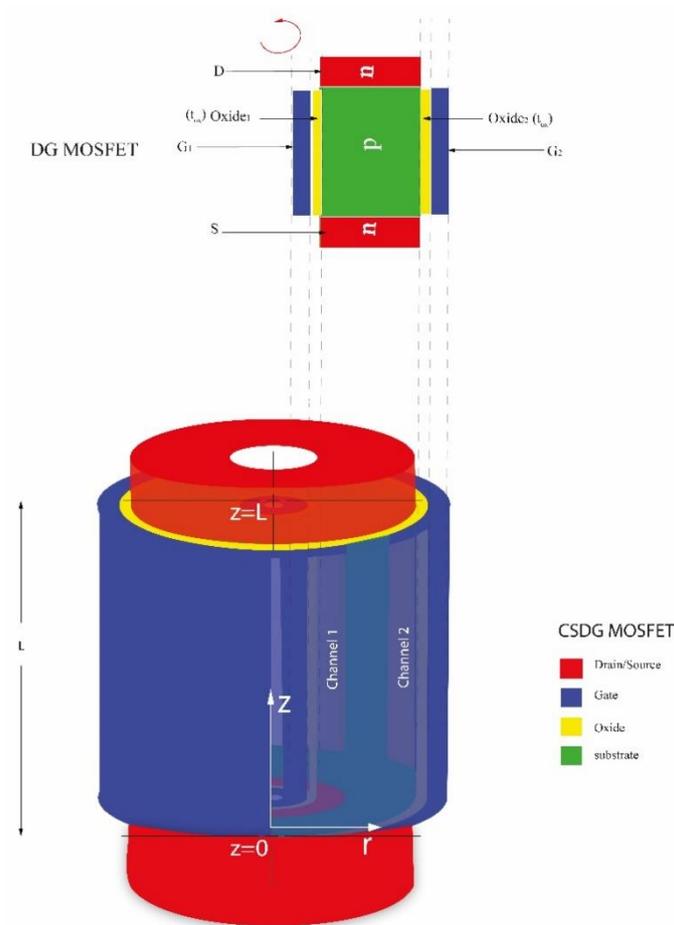
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Figure 1. 3D view of proposed CSDG MOSFET in cylindrical structure.

2.2. Potential Model Derivation with EMA Model

2.2.1. Evanescent Mode Analysis (EMA) Model

The evanescent mode analysis is a mathematical model for solving the 2D Poisson equation as a function of transverse confinement of the device structure with respect to its boundary condition [20].

The 2D Poisson solution yields the electrostatic potential distribution confinement of the CSDG MOSFET as shown in the flowchart of Figure 2. The SCEs on the CSDG MOSFETs are governed analytically by the electrostatic potential caused by biasing the inner and outer gate simultaneously. The derived potentials are extended in modelling the threshold voltage and subthreshold swing. Since, the threshold voltage roll-off are consequences of electrostatic charge sharing effect, it is typically considered as one major indicator of SCEs [31]. Another indicator of SCEs is the subthreshold swing degradation which results to higher off-state current.
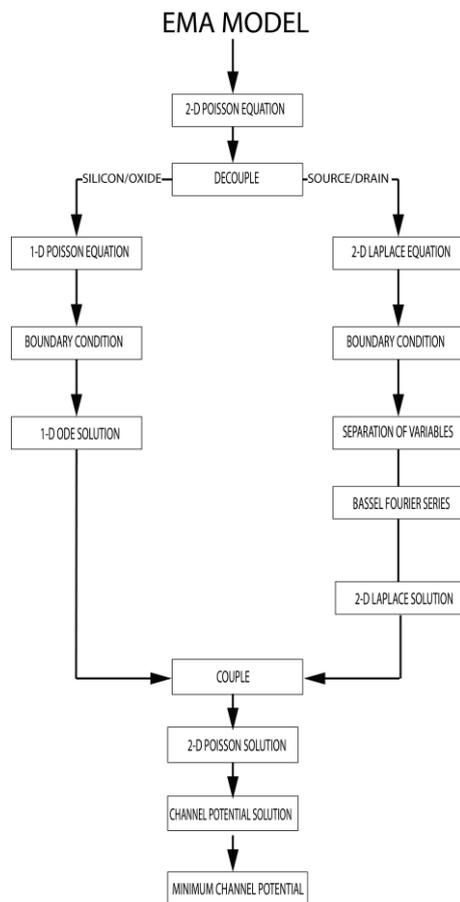
Figure 2. EMA model flow chart.

2.2.2. 2D Poisson Equation

In the subthreshold (weak inversion) regime, the 2D channel potential region, $\psi(r, z)$ is determined from cylindrical Poisson's equation in the cylindrical coordinate system. Assuming uniform channel doping and the independency of the channel potential on the angle θ as highlighted by [14], the 2D Poisson equation (in cylindrical coordinate) is expressed as [32]:

$$\frac{d^2\psi(r,z)}{dr^2} + \frac{1}{r}\frac{d^2\psi(r,z)}{dr^2} + \frac{d^2\psi(r,z)}{dz^2} = \frac{qN_A}{\varepsilon_{si}} \tag{1}$$

where $\psi(r, z)$, N_A, q, and ε_{si}, are the electrostatic potential distribution in the radii silicon film, doping concentration in radii silicon film, electric charge, and dielectric permittivity of the silicon, respectively.

The electrostatic potential, $\psi(r, z)$ can be modeled by decoupling the 2D Poisson equation into two-part as shown in Figure 2: (i) 1D in the silicon region through the oxide thickness, and (ii) 2D based on the source and drain impact on the channel using method of separation of variables [33], that is:

$$\psi(r, z) = \psi_{1D}(r) + \psi_{2D}(r, z) \tag{2}$$

where $\psi_{1D}(r)$ is the channel potential approximation which satisfies 1D Poisson's equation under depletion approximation, along the silicon thickness and it is given as [34]:

$$\frac{d^2\psi_{1D}(r)}{dr^2} + \frac{1}{r}\frac{d\psi_{1D}(r)}{dr} = \frac{qN_A}{\varepsilon_{si}} \tag{3a}$$

Additionally, ψ_{2D} (r, z) accommodates the 2D variation of the channel potential at the oxide-silicon interface with zero charges which satisfies the 2D Laplace equation [35]. The Laplace equation describes the impact of the source and drain on the channel potential. It is given as:

$$\frac{d^2\psi_{2D}(r,z)}{dr^2} + \frac{1}{r}\frac{d^2\psi_{2D}(r,z)}{dr^2} + \frac{d^2\psi_{2D}(r,z)}{dz^2} = 0 \tag{3b}$$

2.2.3. Boundary Condition for the CSDG MOSFET

The boundary conditions for the silicon body and gate oxide are used to solve the decoupled Poisson given Equations (3) and (4) with respect the structures in Figures 3 and 4.
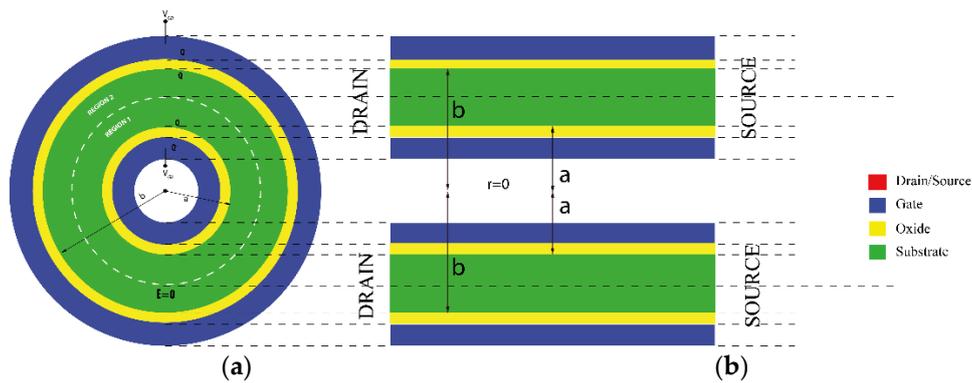

Figure 3. (**a**) CSDG MOSFET's circular cross-sectional view, and (**b**) its view in DG MOSFET.
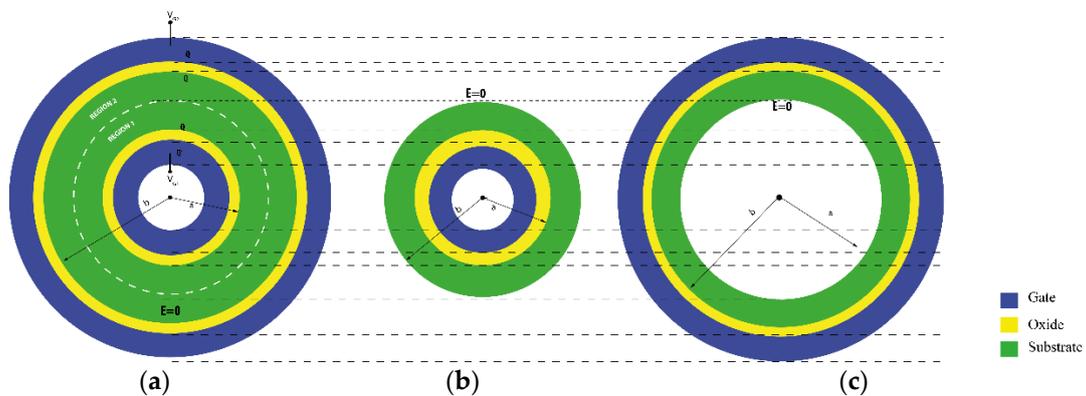

Figure 4. (**a**) CSDG MOSFET's cross section and its, (**b**) internal circular cross-sectional view, and (**c**) external circular cross-sectional view.

Based on Gauss' Law [36], zero electric field must exist within the center of the silicon subtract region indicated by the circular dash line known as the Gaussian surface in Figures 4a and 5a. The CSDG MOSFET is an advanced version of double-gate MOSFET as shown in Figures 1 and 3. It can also be treated as CSG MOSFET since the total electric field beyond $E = 0$ does not have effect on the enclosed surface within the circular dash line and likewise the electric field at the hollow center is zero assuming no charge exist in the center [37]. Hence, the internal and the external radius of CSDG MOSFET can be treated separately as two CSG MOSFET as shown in Figure 4.
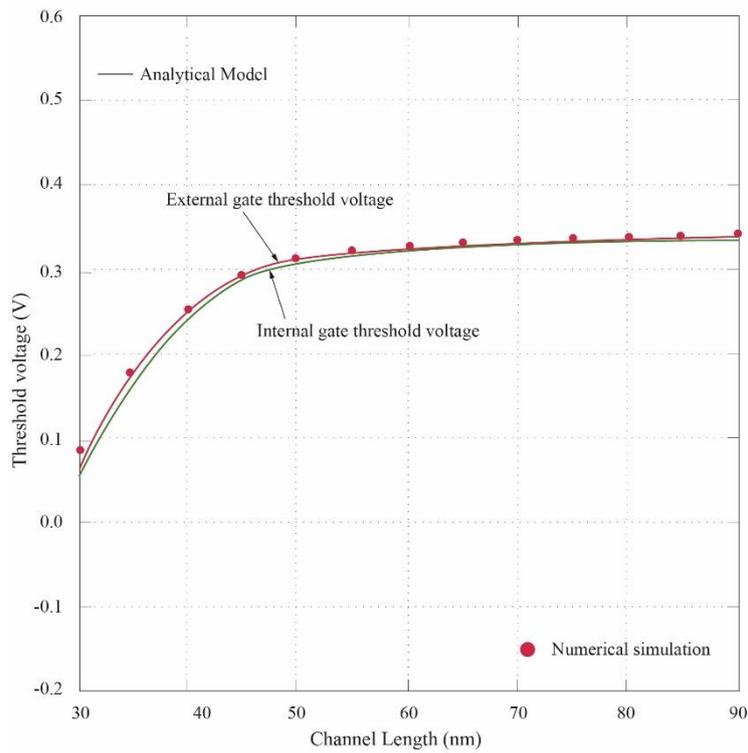
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Figure 5. Comparison of the internal and external gate threshold voltage with respect to channel length of CSDG MOSFET.

In order to obtain the boundary condition for the CSDG MOSFET, Figures 3 and 4 are considered as follows:

(I) The potential at the gate surface for internal and external gates respectively are obtained as:

$$\left.\begin{array}{l} \psi(r=a,z) = \psi_a(a) \\ \psi(r=b,z) = \psi_b(b) \end{array}\right\} \tag{4}$$

Potential at the center of silicon for the internal and external gates respectively with respect to the hollow structure:

$$\left.\begin{array}{l} \psi(r=0,z) = \psi(r=b,z)|_{r=b}\psi_{1D}(0) \\ \psi(r=0,z) = \psi(r=a,z)|_{r=a}\psi_{1D}(0) \end{array}\right\} \tag{5}$$

(II) The electric field at the channel center for internal and external potential, respectively:

$$\left.\begin{array}{l} \left.\frac{d\psi(r,z)}{dr}\right|_{r=0} = \left.\frac{d\psi(r,z)}{dr}\right|_{r=b} = 0 \\ \left.\frac{d\psi(r,z)}{dr}\right|_{r=0} = \left.\frac{d\psi(r,z)}{dr}\right|_{r=a} = 0 \end{array}\right\} \tag{6}$$

(III) The electric field at the silicon-oxide interface for internal and external potential, respectively:

$$\left.\begin{array}{l} C_{ox1}(V_{gs} - V_{FB} - \psi_{1D}(a,z)) = \left.\varepsilon_{si}\frac{d\psi(r,z)}{dr}\right|_{r=a} \\ C_{ox1}(V_{gs} - V_{FB} - \psi_{1D}(b,z)) = \left.\varepsilon_{si}\frac{d\psi(r,z)}{dr}\right|_{r=b} \end{array}\right\} \tag{7}$$

(IV)   The internal electrostatic field boundary condition based on 1D Poisson equation:

$$\left. \begin{array}{l} C_{ox1}(V_{gs} - V_{FB} - \psi_{1D}(a)) = \varepsilon_{si} \frac{d\psi_{1D}(r)}{dr} \Big|_{r=a} \\ C_{ox1}(V_{gs} - V_{FB} - \psi_{1D}(b)) = \varepsilon_{si} \frac{d\psi_{1D}(r)}{dr} \Big|_{r=0} = \varepsilon_{si} \frac{d\psi_{1D}(r)}{dr} \Big|_{r=b} = 0 \end{array} \right\} \tag{8}$$

where:

$$C_{ox1} = \frac{\varepsilon_{ox}}{\left[a In\left(1 + \frac{t_{ox}}{a}\right) \right]} \tag{9}$$

(V)   The external electrostatic field boundary condition based on 1D Poisson equation:

$$\left. \begin{array}{l} C_{ox2}(V_{gs} - V_{FB} - \psi_{1D}(b)) = -\varepsilon_{si} \frac{d\psi_{1D}(r)}{dr} \Big|_{r=b} \\ C_{ox2}(V_{gs} - V_{FB} - \psi_{1D}(a)) = -\varepsilon_{si} \frac{d\psi_{1D}(r)}{dr} \Big|_{r=0} = \varepsilon_{si} \frac{d\psi_{1D}(r)}{dr} \Big|_{r=a} = 0 \end{array} \right\} \tag{10}$$

where:

$$C_{ox2} = \frac{\varepsilon_{ox}}{\left[b In\left(1 + \frac{t_{ox}}{b}\right) \right]} \tag{11}$$

(VI)   The boundary condition along the Z-direction can be used to solve the 2D Laplace equation at the source and drain end. Therefore, the Potential at the source end where (Z = 0) is given as:

$$\psi(r, 0) = V_{bi} \tag{12a}$$

Potential at the drain end (Z = L) is given as:

$$\psi(r, L) = V_{bi} + V_{DS} \tag{12b}$$

$$\left. \begin{array}{l} C_{ox1}(V_{GS} - V_{FB} - \psi_{1D}(0)) = \varepsilon_{si} \frac{d\psi(r,z)}{dr} \Big|_{r=0} \\ \psi_{1D}(0) = \frac{(\psi_{1D}(a) + \psi_{1D}(b))}{2} \end{array} \right\} \tag{13}$$

By substituting Equation (13) into Equation (2), we obtained:

$$\left. \begin{array}{l} \psi(r, 0) = \psi_{1D}(r) + \psi_{2D}(r, 0) = V_{bi} \\ \Rightarrow \psi_{2D}(r, 0) = V_{bi} - \psi_{1D}(r) \\ \Rightarrow \psi_{2D}(r, L) = V_{bi} + V_{DS} - \psi_{1D}(r) \end{array} \right\} \tag{14}$$

where V_{bi}, V_{FB}, V_{GS}, and V_{DS}, are the built-in voltage, flat band voltage, gate to source voltage, and drain voltage, respectively. C_{ox1} and C_{ox2} are internal gate and external gate oxide capacitance, respectively, and ε_{si} and ε_{ox} are dielectric permittivity of silicon and the dielectric permittivity of the oxide. Additionally, *r* varies to *a* when considering the internal potential and to *b* when considering the external potential in Equations (9) and (11), respectively.

Using the boundary conditions Equations (4)–(14), the surface potential for the internal and external gate of the proposed CSDG structure is (Appendix A contains the detailed procedure):

$$\psi_S(z) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A a^2}{4\varepsilon_{si}} - \frac{qN_A t^2_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox-a}} \\ + \left(A_0 e^{(z\lambda_0)} + B_0 e^{(-z\lambda_0)} \right) J_0(a\lambda_0) \tag{15}$$

$$\psi_S(z) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t^2_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox-a}} \\ + \left(A_0 e^{(z\lambda_0)} + B_0 e^{(-z\lambda_0)} \right) J_0(b\lambda_{01}) \tag{16}$$

The surface potential obtained in Equations (15) and (16) is extended in the modelling of the threshold voltage and subthreshold swing of the proposed CSDG MOSFET which predicts the device characteristics and performance.

3. Threshold Voltage Model for the Proposed CSDG

The CSDG MOSFET as a switch requires an external source to be able to determine the *On-OFF* nature of the device. Since MOSFET are voltage-controlled device, a DC voltage is required to control the CSDG MOSFET. This DC voltage required for the *ON*—switching of the device when a reasonable drain current is achieved is known as the threshold voltage.

Threshold voltage can also be defined as the gate voltage at which the minimum surface potential is twice the Fermi potential, $2\phi_f$ [38]. Hence, Equations (2), (15), and (16) is simplified further by setting its first derivative at $z = 0$ along the z-axis to obtain the minimum surface potential position (z_{min}) which equates the Fermi potential level of the device structure. After mathematical transformation, the minimum surface potential in terms of z_{min} is given as:

$$\psi_{s_{\min}}(z_{\min}) = \psi_{1D}(r) + 2J_0(\lambda_0 r)\sqrt{A_m B_m} = 2\phi_f \tag{17}$$

where:

$$\phi_f = \frac{KT}{q} In\left(\frac{N_A}{n_i}\right)$$

where n_i is the intrinsic carrier concentration, $r = a$ for internal cylinder and $r = b$ for external cylinder, and $m = 0$ and $m = 1$ for the internal and external coefficient. K, T, q, N_A, and n_i are the Boltzmann's constant, Temperature (K), electronic charge, and doping concentration, respectively.

The threshold voltage for the proposed CSDG structure is given as:

$$V_{TH_{Si}\_CSDG} = V_{TH_L\_CSDG} - V_{TH_i\_CSDG} \tag{18}$$

where V_{THL_CSDG} are the threshold voltage for the long channel assuming the drain and source has no the effect on the channel, V_{THi_CSDG} are the threshold voltage roll-off due to drain and source effects with respect to internal or external gate, and V_{THsi_CSDG} is the short channel threshold voltage for the internal and external gate surface potential.

Considering the Long channel condition and assuming gradual channel approximation [39], the threshold voltage for the internal and external gates are given based on Equation (17) as:

$$\psi_{1D}(r) = \left.2\phi_f\right|_{V_{GS}=V_{TH\_L}} \Rightarrow$$
$$V_{TH\_L} = 2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A a^2}{4\varepsilon_{si}} + \frac{qN_A t_{si}^2}{16\varepsilon_{si}} + \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox1}} \tag{19}$$

$$V_{TH\_L} = 2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A b^2}{4\varepsilon_{si}} + \frac{qN_A t_{si}^2}{16\varepsilon_{si}} + \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox2}} \tag{20}$$

Considering the short channel condition, we included the drain and source effect in the model based on Equation (17) as given:

$$\psi_{1D}(r) + 2J_0(\lambda_{01}r)\sqrt{A_0 B_0} = 2\phi_f \tag{21}$$

(a)   Considering the internal gate *(r = a)* for the short channel model:

$$\psi_S(r = a, z_{\min})|_{V_{GS}=\psi_{1D}(a)=V_{th}} = \psi_{1D}(a)$$
$$+\left(A_0 e^{(z_{\min}\lambda_0)} + B_0 e^{(-z_{\min}\lambda_0)}\right)J_0(a\lambda_0) = 2\phi_f \tag{22}$$

From Equation (17) we obtain:

$$V_{TH_a\_CSDG} + 2J_0(a\lambda_0)\sqrt{A_0B_0} = 2\phi_f \tag{23}$$

This can be expressed in polynomial form of second order as given:

$$X_1 V_{TH_a\_CSDG}^2 + X_2 V_{TH_a\_CSDG} + X_3 \tag{24}$$

where:

$$\left. \begin{array}{l} X_1 = 4a_1 - a_2 - 2 \\ X_2 = (2V_{bi} + V_{DS})(2 - 4a_1) \\ X_3 = \left[4a_1[(V_{bi}(V_{bi} + V_{DS}))] - (V_{bi} + V_{DS})^2 - 4\phi_f^2 a_2 - V_{DS}^2 \right] \\ \left. \begin{array}{l} a_1 = 2J^2(a\lambda_0)\sinh(L\lambda_0) \\ a_2 = 4J^2(a\lambda_0)\sinh^2(L\lambda_0) \end{array} \right\} \end{array} \right\} \tag{25}$$

Therefore, the threshold voltage for the internal gate surface potential due to the short channel is given as:

$$V_{TH_a\_CSDG} = \frac{-X_2 + \sqrt{X_2^2 - 4X_1X_3}}{2X_1} \tag{26}$$

Hence the closed-form expression of the threshold voltage roll-off for the internal gate of CSDG MOSFET is given with the practical assumption of $\lambda_n L \gg 1$ [40]:

$$V_{TH_{Sa}\_CSDG} = \left(2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A a^2}{4\varepsilon_{si}} + \frac{qN_A t_{si}^2}{16\varepsilon_{si}} + \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox-a}} \right) - \left(\frac{-X_2 + \sqrt{X_2^2 - 4X_1X_3}}{2X_1} \right) \tag{27}$$

(b) Considering the External gate *(r = b)* for the short channel model:

$$V_{TH_b\_CSDG} + 2J_0(b\lambda_0)\sqrt{A_0B_0} = 2\phi_f \tag{28}$$

Similarly, this can be expressed as a quadratic equation as given:

$$Y_1 V_{TH_b\_CSDG}^2 + Y_2 V_{TH_{TH_b\_CSDG}} + Y_3 \tag{29}$$

where:

$$\left. \begin{array}{l} X_1 = 4a_1 - a_2 - 2 \\ X_2 = (2V_{bi} + V_{DS})(2 - 4a_1) \\ X_3 = \left[4a_1[(V_{bi}(V_{bi} + V_{DS}))] - (V_{bi} + V_{DS})^2 - 4\phi_f^2 a_2 - V_{DS}^2 \right] \\ \left. \begin{array}{l} a_1 = 2J^2(a\lambda_0)\sinh(L\lambda_0) \\ a_2 = 4J^2(a\lambda_0)\sinh^2(L\lambda_0) \end{array} \right\} \end{array} \right\} \tag{30}$$

Therefore, the threshold voltage for the short channel is:

$$V_{TH_b} = \frac{-Y_2 + \sqrt{Y_2^2 - 4Y_1Y_3}}{2Y_1} \tag{31}$$

Like the closed-form expression of the short channel threshold voltage for the external gate of CSDG MOSFET is given as:

$$V_{TH_{Sb}\_CSDG} = \left(2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A b^2}{4\varepsilon_{si}} + \frac{qN_A t_{si}^2}{16\varepsilon_{si}} + \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox-b}} \right) - \left(\frac{-Y_2 + \sqrt{Y_2^2 - 4Y_1Y_3}}{2Y_1} \right) \tag{32}$$

Therefore, the threshold voltage of the short channel can be determined either through the internal gate minimum surface potential or the external gate minimum surface potential of the CSDG MOSFET as given in Equations (27) and (32).

4. Subthreshold Current and Subthreshold Swing

This section presents the subthreshold current and the subthreshold swing close-form expression using the minimum surface potential derived from Equation (17). Subthreshold swing determines the device's behavior by showing the effect of the change in external gate voltage on the subthreshold current. In an ideal MOSFET, the subthreshold current is zero when the applied gate voltage is lesser than threshold voltage. However, in the practical aspect, such behavior is never obtainable. The ideal subthreshold swing value at room temperature is 60 mV/dec. Furthermore, the analyses are verified with the numerical simulation.

4.1. Subthreshold Current

The subthreshold current flows from source to drain along the channel length through diffusion mechanism. Hence, the subthreshold current is given by integration with respect to the circular area as given [41]:

$$\left. \begin{array}{l} I_{Sub} = q\pi t_{si} D_n \frac{n_m(r,z)}{L}\left[1 - e^{\frac{-V_{DS}}{V_T}}\right] \\ D_n = \mu V_T \end{array} \right\} \tag{33}$$

where n_m is the electron density at subthreshold regime in relation to classical Boltzmann's equation. it is given as:

$$n_m(r,z) = \frac{n_i^2}{N_A} e^{\left(\frac{\psi(r,z)}{V_T}\right)} \tag{34}$$

D_n, V_T, and n_i are the diffusion constant, thermal voltage, and intrinsic concentration respectively. Using the Equation (33), assuming the subthreshold current occurs at the virtual cathode ($z = zmin$), the subthreshold current of CSDG MOSFT ($I_{\_CSDG}$) is obtained by:

$$I_{CSDG\_sub} = I_a + I_b \tag{35a}$$

$$I_{CSDG} = \frac{q\pi t_{si} D_n n_m(r,z_{\min})\left[1 - e^{\frac{-V_{DS}}{V_T}}\right]}{\int\limits_0^l M^{-1}(z)dz} + \frac{q\pi t_{si} D_n n_m(r,z_{\min})\left[1 - e^{\frac{-V_{DS}}{V_T}}\right]}{\int\limits_0^l N^{-1}(z)dz} \tag{35b}$$

where:

$$\left. M(z) = \frac{qn_i^2}{N_A}\int\limits_{\frac{t_{si}}{2}}^{a} f_a(r)dr \;,\; N(z) = \frac{qn_i^2}{N_A}\int\limits_{a}^{b} f_b(r)dr, f(r) = e^{\frac{q\psi(r,z_{\min})}{KT}} \right\} \tag{36}$$

$M(z)$ and $N(z)$ can be obtained by integrating the indefinite $f_a(r)$ and $f_b(r)$ through the trapezoidal rule of numerical approach as given by [40]:

$$\left. \begin{array}{l} M = \frac{qn_i^2}{N_A}G_a\left[\left(e^{\frac{q\psi_{\min}}{kT}}\right) + \left(\sum\limits_{k=1}^{n-1}\left(e^{\frac{\psi(G_ak,z_{\min})}{KT}}\right) + e^{\frac{q\psi(0,z_{\min})}{KT}}\right)\right] \\ G_a = \frac{a}{2n} \end{array} \right\} \tag{37a}$$

$$\left. \begin{array}{l} N = \frac{qn_i^2}{N_A}G_b\left[\left(e^{\frac{q\psi_{\min}}{kT}}\right) + \left(\sum\limits_{k=1}^{n-1}\left(e^{\frac{\psi(G_bk,z_{0\min})}{KT}}\right) + e^{\frac{q\psi(0,z_{0\min})}{KT}}\right)\right] \\ G_b = \frac{b}{2n} \end{array} \right\} \tag{37b}$$

By equating the partition number to one ($n = 1$) in Equations (37a) and (37b), the subthreshold current for CSDG MOSFET can be obtained in Equation (35b).

4.2. Subthreshold Swing

Subthreshold swing (SS) is defined as the change in gate bias voltage required for a change of one decade of subthreshold drain current [42]. Since, subthreshold swing is an important device parameter to represents the switching characteristics of MOS device, Hence, its evaluation is a necessity and it is given as [43]:

$$SS = \left[\frac{d \log I_{CSDG\_sub}}{dV_{GS}} \right]^{-1} \tag{38}$$

By substituting Equation (35b) into Equation (38), the subthreshold swing can be calculated, since the $\psi\,(r, z_{min})$ is a function of change in voltage (dv) from Equation (38) and dV is a function of gate voltage. However, the subthreshold swing is very difficult to obtain using the subthreshold current due to its complicated dependency of the minimum radius (r_{min}) on the gate voltage and the numerical integration involved. In a simpler approach, the subthreshold current can be related to the minimum surface potential, $\psi_{s\_min}(r, z_{min})$ through the electron concentration at the virtual cathode [44]. This is because at subthreshold operation, the subthreshold current is dominated by a diffusion process. This leads to a probability of mobile electron surmounting the source end of the energy barrier. Thus, it can be assumed that the subthreshold current is proportional to the carrier concentration at the virtual cathode $n_{min}\,(r, z_{min})$, given as [42]:

$$I_{sub} \cdot \alpha \cdot n_{min}(r, z_{min}) \alpha \cdot e^{\left(\frac{\psi_{min}}{V_T} \right)} \tag{39}$$

Since the electron density follows Boltzmann distribution according [45] we can express the SS by substituting Equation (39) in Equation (38) as given:

$$SS_{CSDG} = \frac{V_T In10}{\left(\frac{d\psi_{s_{min}}(r, z_{min})}{dV_{GS}} \right)} \tag{40}$$

where $V_T = \frac{KT}{q}$.

From Equation (39) minimum surface potential can be obtained as:

$$\psi(r, z_{min}) = \psi(r) + \psi(r, z_{min}) = \psi(r) + 2J_0(r\lambda)\sqrt{A_1 B_1} \tag{41}$$

$$\begin{aligned} \psi_{s_{min}}(r_{min}) = (V_{GS} - V_{FB}) + \frac{qN_A r^2}{4\varepsilon_{si}} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox-a}} \\ + \left(A_0 e^{(z_{min}\lambda_0)} + B_0 e^{(-z_{min}\lambda_0)} \right) J_0(r\lambda_0) \end{aligned} \tag{42}$$

$$\frac{d\psi_{s_{min}}(r, z_{min})}{dV_{GS}} = \frac{d\psi(r)}{dV_{GS}} + \frac{d\psi(r, z_{min})}{dV_{GS}} \tag{43}$$

Therefore, the subthreshold swing can be obtained using Equations (40), (42), and (43). The simulation results of the close form expression obtained and the numerical results are explained in the further sections.

5. Results and Discussions

In this section, the theoretical and numerical simulation results are presented using Equations (27), (32), (35), and (40). The list of parameters used for the CSDG MOSFETs are given in Table 1.

The threshold voltage of the internal and external gate CSDG MOSFET with variation of channel length is shown in Figure 5. It has been observed that the decrease in channel length, causes a corresponding rapid decrease in the threshold voltage. The phenomenon is called the threshold roll-off which can be determined with either the internal gate or external gate model. Although, the threshold

voltage between the internal and external gate are almost the same. However, the external gate has lightly higher threshold voltage than the internal gate due to higher minimum surface potential as shown in Figure 5. The external gate is in perfect match with the numerical simulation.

Table 1. The device parameters for simulation.

Parameters	Values
t_{ox1}, t_{ox2}	2–5 nm (each)
L	9–90 nm
a	3–6 nm
b	13 nm
$t_{si} = (b - a)$	10 nm
N_A	10^{17} cm^{-3}
Φ_{MS1}, Φ_{MS2}	4.8 eV
V_{DS}	0.1 V

The thin gate oxide of the internal and external structure of the CSDG MOSFET enables the dominance of the vertical electrical fields over the lateral electric field resulting from the drain and source ends. This enables the two gates to have better control of the channels created within the structure. Furthermore, the dominance of the vertical electric field will result to less leakage of current when the device is turned off. The variation of threshold voltage with channel length at different oxide thickness is shown in Figure 6. It is clearly observed that the decrease in channel length, results to the decrease in threshold voltage which affects the device performance. Additionally, the lower the threshold voltage, the more unpredictable the device switching performance. This degrades the switching characteristics of the device during the *turn-OFF* stage. However, higher threshold voltage enhances stability and accurate switching of the device. We optimized the threshold voltage with different oxide thickness. The threshold voltage increases with decrease in gate oxide, hence, thin gate oxide tends to provide better gate controllability than the thicker oxide. Additionally, thin gate oxide reduces SCEs in CSDG MOSFETs. The result is in good agreement with the numerical simulation of the proposed structure.

Furthermore, the thinner radii silicon film difference of the CSDG MOSFET structure enhances the internal and external gate controls of the channel carriers over the drain and source ends. The reduction in radii difference further reduces the drain and source sizes, and their impact on the channel is significantly reduced. Hence, the gates have better control of the channel carriers. The variation of threshold voltage with channel length at different radii silicon film thickness is shown in Figure 7. It is observed that as the silicon film thickness decreases, the threshold voltage of CSDG MOSFET increases because the drain ends losses control of the channel. As a result, the thin silicon film provides better gate controllability leading to low threshold voltage degradation and better suppression of SCEs. The result matches the numerical simulation of the proposed structure.

The CSDG MOSFETs provides higher drain current due to the coupled internal and external gates. These gates increase the average electric field of the structure. This enables rapid acceleration of carriers at the interface towards the drain terminal, resulting to the enhancement of the carrier transportation efficiency for the proposed structure. However, an increase in the drain current causes slight increase in the subthreshold leakage current, which needs to be minimized at less than 30 nm gate length. The subthreshold current versus the gate voltage with different variation in channel length is shown in Figure 8. The channel length is varied from 60 nm to 20 nm. It is clearly observed that the subthreshold current increases as the channel length decreases with an upward shift as clearly observed. This implies lesser control of the gate over the channel at lower channel length resulting to more leakage current. It is should be noted that the model is considered at the subthreshold regime. The slight deviation of the numerical simulation from model towards 0.5 V of the gate voltage shows the inversion onset phase. The model matches with the numerical simulation for the proposed structure within the subthreshold regime.
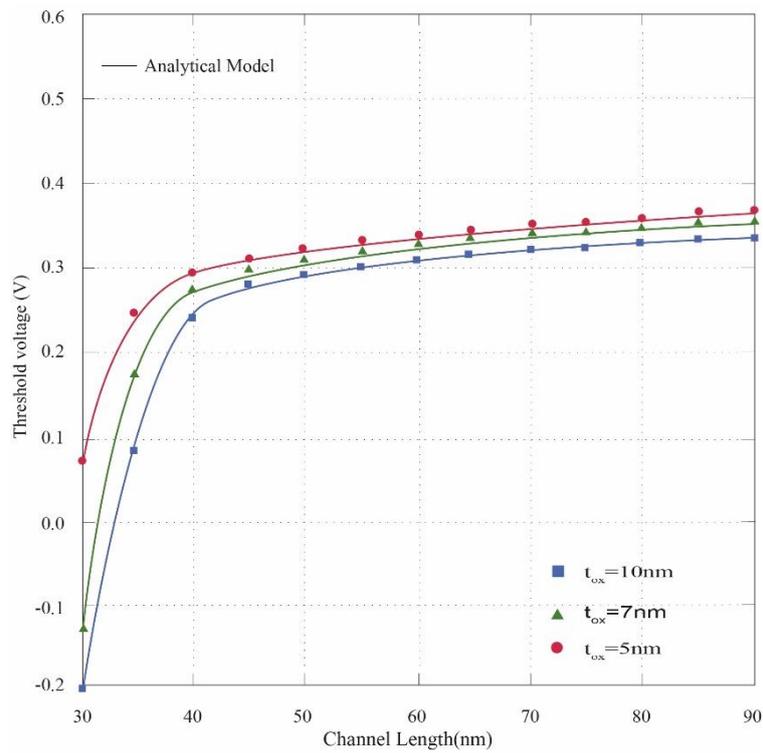
Figure 6. Threshold voltage of the external gate of CSDG MOSFET versus channel length by numerical simulation and model with different gate oxide thickness.
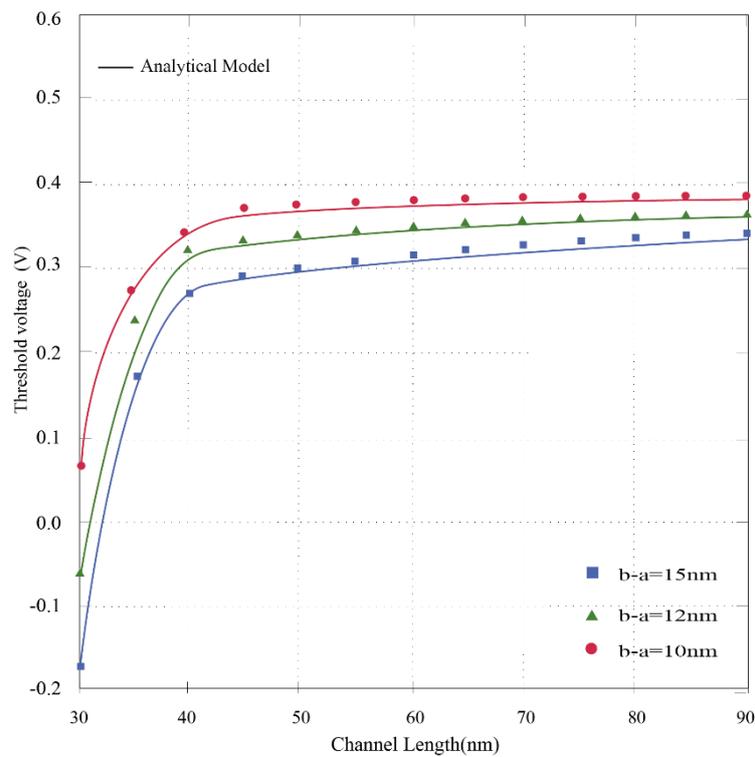

Figure 7. Threshold voltage of the external gate of CSDG MOSFET versus channel length by numerical simulation and model with different radii difference (silicon) thickness.
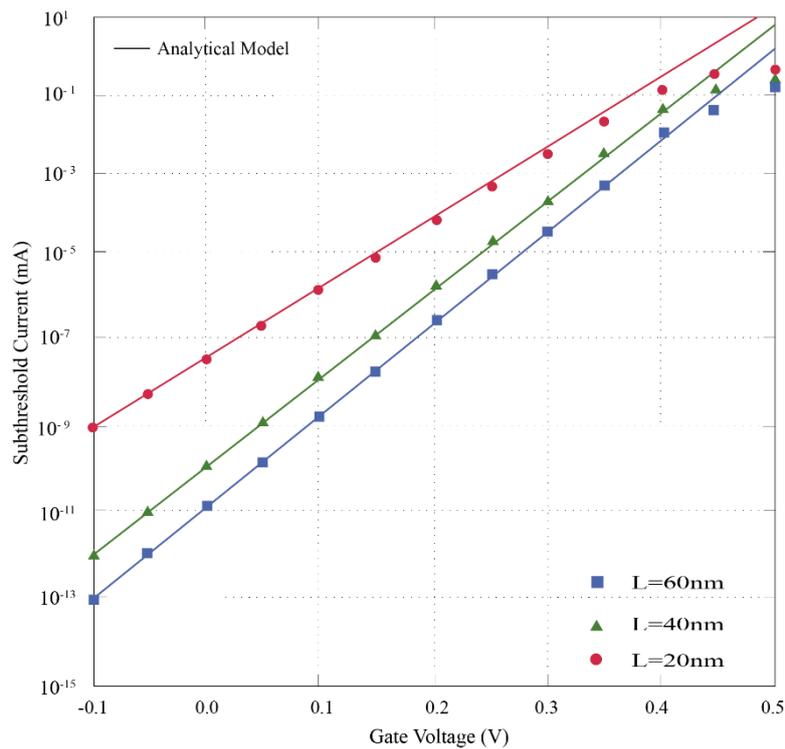
Figure 8. Subthreshold current of CSDG MOSFET versus the gate voltage by numerical simulation and model with different channel length.

Furthermore, the presence of the thin gate oxide on the proposed CSDG MOSFET reduces the subthreshold leakage current by enabling greater gate control over the channel and minimal lateral Electric Field effects. The subthreshold current versus the gate voltage with respect to different variation of the gate oxide thickness is shown in Figure 9. It is observed that the as the gate-oxide thickness increases, the subthreshold current leakage also increases. The increased gate oxide reduces the gate control over the channel and the leakage due to impacts from the drain is added to the channel. Hence, the thin oxide is preferred over thicker oxide. However, a balance must be maintained to prevent gate-tunneling. The deviation of the numerical simulation toward 0.5 V shows the onset of the strong inversion. The numerical simulation is in good agreement with the model within the subthreshold regime.

Additionally, the internal and external gates voltage describes the exponential behavior of the current in the CSDG MOSFET at subthreshold. This exponential behavior known as the subthreshold swing which increases at shorter gate lengths is minimized in CSDG MOSFET with thin oxide thickness. The smaller subthreshold swing enables better channel control by the gates at micro power application. The subthreshold swing versus channel length for different oxide thickness is presented in Figure 10. Subthreshold swing decreases significantly as the oxide thickness decreases because the gates enhances effective channel control. Hence, a thin oxide thickness provides excellent immunity over SCEs. Furthermore, the model matches the numerical simulation of the proposed structure.
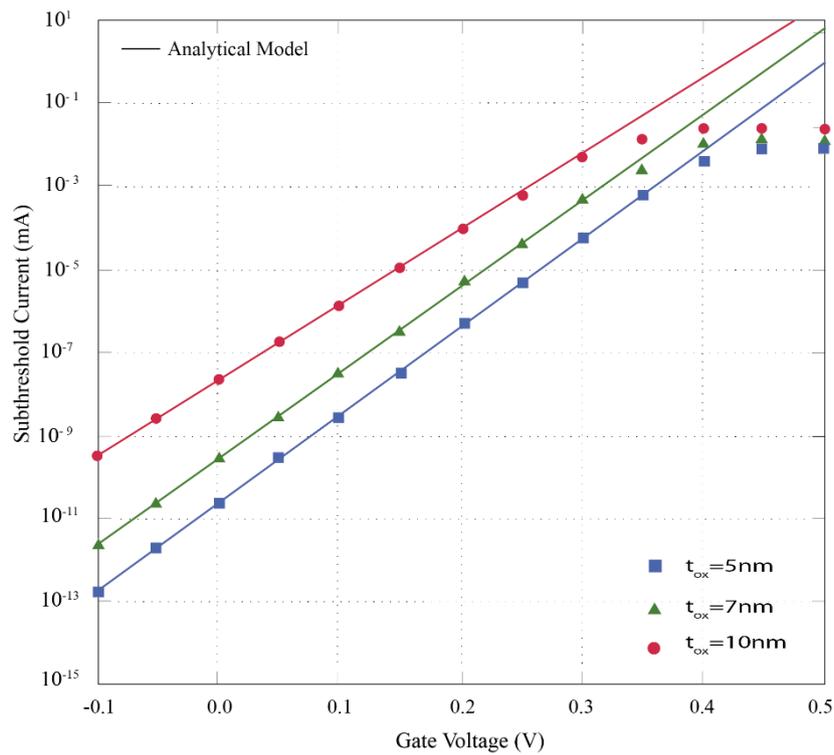
Figure 9. Subthreshold current of CSDG MOSFET versus the gate voltage by numerical simulation and model with different gate oxide.
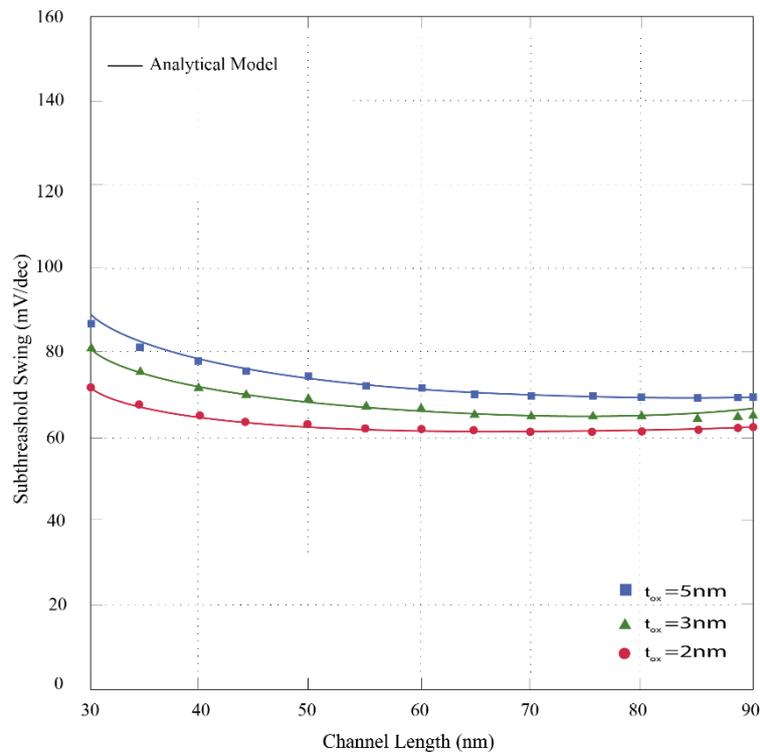

Figure 10. Subthreshold swing of CSDG MOSFET versus channel length by device simulator and model with different oxide thickness.

Furthermore, the reduction in radii Silicon film difference of the CSDG MOSFET enhances the device performance. The subthreshold swing has been minimized by thin radii silicon film. The

internal and external gate control over the channel minimizes the lateral field effects from drain end. This results to increase in the threshold voltage. Since the subthreshold swing depends on the gate voltage, increasing the threshold voltage leads to gradual reduction in the subthreshold swing. The subthreshold swing versus channel length at various silicon film thickness is shown in Figure 11. It is obviously seen that as the channel length decrease, the subthreshold swing increases which is a major problem in scaling at nanometer. This affects the switching characteristics of the of device structure. However, as the radii silicon film thickness decreases, the subthreshold swing decreases. At 10 nm radii silicon film thickness, the subthreshold swing decreases below 80 mV/dec., enabling faster switching characteristics of the device structure. Hence, thin radii silicon film thickness helps in SCEs suppression at reduced channel length. The numerical simulation matches perfectly with the proposed device model.
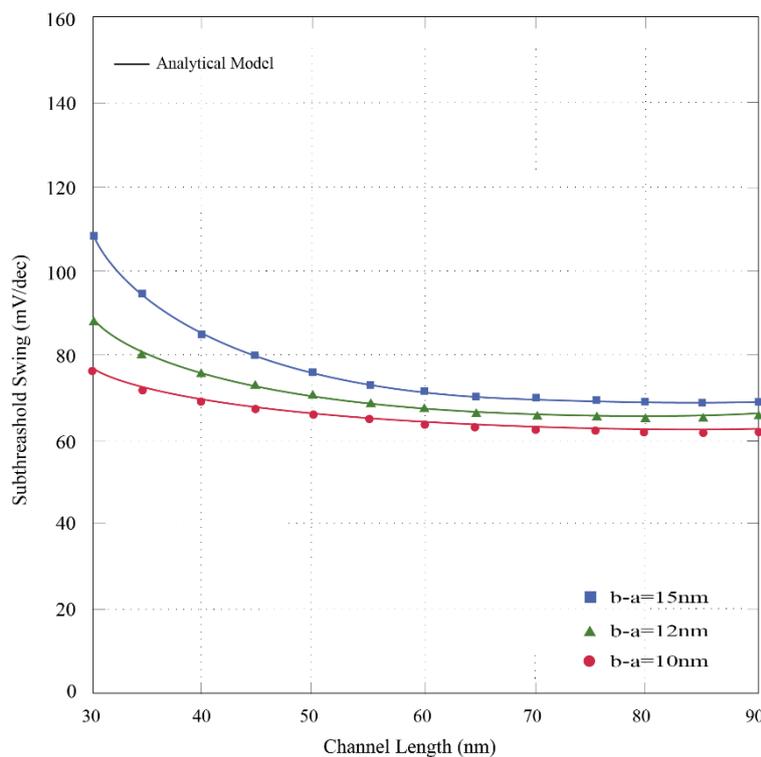

Figure 11. Subthreshold swing of CSDG MOSFET versus channel length by the device simulator and model with different radii silicon film thickness.

6. Conclusions and Recommendations

In this research work, the close form expression for the threshold voltage, subthreshold current, and the subthreshold swing has been derived using evanescent-mode analysis to demonstrate the performance of the CSDG MOSFET. The behavior of the SCEs with various device parameters like radii silicon film thickness, gate-oxide thickness, and the channel length has been considered to predict the device performance. Results shows that the threshold voltage decreases with decrease in channel length. This results to threshold voltage roll-off which is due to 2D field effect that originated from the source and drain region because of their proximity to the channel at nanoscale length. However, this is optimized by decreasing the oxide thickness and radii silicon film difference of the CSDG MOSFET to increase the stability of the threshold voltage and better control of the turn-OFF current. This shows that the CSDG MOSFET improves immunity to SCEs, making it a promising device for the future nanometer MOSFET applications.

Although, the subthreshold swing increases above 60 mV/dec at room temperature as the channel length decreases. However, it decreases with proportional decrease in radii silicon film thickness or

gate-oxide thickness which enhances the switching performance of the device for CMOS technology application. Additionally, it is observed that the decrease in the device channel length increases the subthreshold current leakage. However, the coupling of the internal and external gate control over the channel limits the leakage. Hence, making CSDG MOSFET, a suitable device for nanoscale switching operation.

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Appendix A

(a)   Solution to the 1-D Poisson Equation ($\psi_{1D}(r)$) which satisfies the long channel potential distribution of the device structure.

The 1D equation can easily been solved with this approximation with the boundary conditions as given [13]:

$$\psi_{1D}(a) = \frac{V_0}{4}\left[\frac{a^2}{t^2_{si}} - \frac{1}{4} - \frac{1}{M}\right], V_0 = \frac{qN_A t^2_{si}}{\varepsilon_{si}}, M = \frac{C_{si}}{C_{ox1}}, C_{si} = \frac{\varepsilon_{si}}{t_{si}}\right\} \tag{A1}$$

(I)   Internal Gate potential distribution can be derived by substituting Equations (8) and (13) into Equation (A1) as given:

$$\psi_{1D}(a) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A a^2}{4\varepsilon_{si}} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox1}} \tag{A2}$$

(II)   External Gate potential distribution can be derived by substituting Equations (10) and (11) into Equation (A1) as given:

$$\psi_{1D}(b) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t_{si}^2}{16\varepsilon_{si}} - \frac{qN_A t_{si}^2 C_{si}}{4\varepsilon_{si} C_{ox2}} \tag{A3}$$

(b)   Solution to the 2D Laplace equation ($\psi_{2D}(r,z)$) satisfies the impact of the drain and the source on the channel at nanometer length.

Authors have solved 2D Laplace equation (Equation (3b)) using the method of separation of variables as given [33]:

$$\psi_{2D}(r,z) = G(r)H(z) \tag{A4}$$

Considering the internal gate where ($0 \leq r \leq a$), and substituting (A4) into (3b) results to the separation of the 2D Laplace equation into two independent variables as given:

$$\frac{1}{G(r)}\left(\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}G(r)\right)\right) + \frac{1}{H(z)}\left(\frac{dH(z)}{dz^2}\right) = 0 \tag{A5}$$

Rearranging by using a separation constant, λ known as the eigenvalue, (A5) can be separated into two parts as:

$$\frac{1}{H(z)}\left(\frac{dH(z)}{dz^2}\right) = \lambda^2 \tag{A6}$$

and:

$$\frac{1}{G(r)}\left(\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}G(r)\right)\right) = -\lambda^2 \tag{A7}$$

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Equations (A6) and (A7) have a general Bessel solution function as given [20,46]:

$$\psi_{2D}(r,z) = G(r)H(z) = \sum_{n=0}^{\infty}\left(\left[A_n e^{(z\lambda_n)} + B_n e^{(-z\lambda_n)}\right]J_0(r\lambda_n)\right) \tag{A8}$$

Since the lowest value ($n = 0$) dominates the whole series due to rapid decay of higher value [47], (A8) is reduced to:

$$\psi_{2D}(r,z) = G(r)H(z) = \left(\left[A_0 e^{(z\lambda_0)} + B_0 e^{(-z\lambda_0)}\right]J_0(r\lambda_0)\right) \tag{A9}$$

A_0 and B_0 are obtained using the boundary condition in Equations (12) and (13) as given:

$$\begin{aligned}A_0 &= \left(\frac{(V_{bi}+V_{DS}-\psi_{1D}(a))-(V_{bi}-\psi_{1D}(a))e^{-L\lambda_0}}{J_0(a\lambda_0)(e^{L\lambda_0}-e^{-L\lambda_0})}\right)\\ B_0 &= \left(\frac{(V_{bi}-\psi_{1D}(a))e^{L\lambda_0}-(V_{bi}+V_{DS}-\psi_{1D}(a))}{J_0(a\lambda_0)(e^{L\lambda_0}-e^{-L\lambda_0})}\right)\end{aligned} \tag{A10}$$

where the eigenvalue, λ which is the scaling length parameter must verify the Poison equation at the silicon-insulator interfaces for continuity as given [48]:

$$\lambda_0 = \left.\frac{C_{ox1}J_0\left(\lambda_0\frac{b-a}{2}\right)}{\varepsilon_{si}J_1\left(\lambda_0\frac{b-a}{2}\right)}\right\} \tag{A11}$$

Using Equations (2), (A2), (A9), and (A10), the solution for the surface channel potential in Equation (15) is derived. Using similar approach, Equation (16) is obtained.

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