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LTPS TFTs with an Amorphous Silicon Buffer Layer and Source/Drain Extension

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Abstract: A low leakage poly-Si thin film transistor (TFT) is proposed featuring hydrogenated amorphous silicon (a-Si:H) buffer layer and source/drain extension (SDE) by using technology computer aided design (TCAD) simulation. This architecture reduces off-current effectively by suppressing two leakage current generation mechanisms with little on-current loss. The amorphous silicon buffer layer having large bandgap energy (E_g) suppresses both thermal generation and minimum leakage current, which leads to higher on/off current ratio. In addition, the formation of lightly doped region near the drain alleviates the field-enhanced generation in the off-state by reducing electric field. TCAD simulation results show that the proposed TFT shows more than three orders of magnitude lower off-current than low-temperature polycrystalline silicon (LTPS) TFTs, while maintaining on-current.

Keywords: LTPS TFT; off-state current; on/off current ratio; source/drain extension; hydrogenated amorphous silicon (a-Si:H) buffer layer

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1. Introduction

A low-temperature polycrystalline silicon thin-film transistor (LTPS TFT) fabricated on a glass substrate has been considered as one of the most attractive options for active-matrix organic light emitting diode (AMOLED) display applications because it has higher electron mobility and driving current than an amorphous-silicon (a-Si) TFT and oxide TFT [1–7]. However, there are critical disadvantages of LTPS TFTs: low on/off current ratio and high leakage current [8–17]. For the improvement of display quality, the leakage current of TFTs which act as pixel switches should be minimized [1–6]. The main leakage mechanism of LTPS TFTs is the generation-recombination (G-R) occurring at the drain-side depletion region [6–9]. The G-R is classified into the two sub-mechanisms [9–13]. One is the thermal generation depending on trap density, energy bandgap, and temperature while being independent of gate voltage (V_G). It is dominant under the low electric field condition, especially near the flat band voltage. Thus, it determines minimum leakage current. The other is the field-enhanced generation including field-enhanced thermal emission (Poole–Frenkel), phonon-assisted tunneling, trap-assisted tunneling, and band-to-band tunneling (BTBT). It strongly depends on V_G and trap density because the tunneling barrier narrows with increasing V_G and trap density. Under the high electric field condition, the field-enhanced generation makes the leakage current independent of temperature and exponentially dependent on V_G [1,11].

Several methods have already been proposed for lower leakage current and higher performance [18–30] including field-induced drain (FID) [28,29] and current and electric field split (CES) design TFTs [30]. However, both FID and CES design TFTs suffer from complex fabrication process and large parasitic capacitance because they need one more field plate.

In this paper, we propose the LTPS TFTs using an amorphous silicon buffer layer and source/drain extension (SDE) which lowers leakage current by suppressing both thermal generation and field-enhanced generation in the off-state. The hydrogenated a-Si (a-Si:H) layer whose bandgap energy (E_g) is 1.8 eV is located between the active layer and gate insulator to suppress thermal generation. The SDE reduces the electric field at the channel/drain junction, which alleviates field-enhanced generation. It should be noted that the introduction of an amorphous silicon buffer layer and SDE causes only little on-state current loss. It is because the amorphous silicon layer is very thin (<4 nm) [25–27], because the defects and crystallinity of the amorphous silicon layer can be optimized by controlling the silane (SiH_4) and hydrogen (H_2) gas flow rates [26] and because the current is spread to the entire SDE region [14–16]. Thus, without serious on-current loss, the on/off current ratio becomes $>10^3 \times$ higher in high V_D. Additionally, in terms of process flow, sidewall spacer and implant-to-silicide (ITS) techniques can be introduced [31,32].

2. Proposed Process Flow

Figure 1 shows the key fabrication steps of our proposed LTPS TFT. First, a 45 nm thick a-Si layer is deposited and then crystallized by excimer laser annealing (ELA) to convert a-Si into poly-Si. On the poly-Si layer, a 4 nm thick amorphous silicon buffer layer is deposited controlling the ratio of silane (SiH_4) to hydrogen (H_2) [26]. In addition, to make 4 nm amorphous silicon, it is necessary to keep the temperature and radio frequency (RF) power low to prevent crystallization for plasma enhanced chemical vapor deposition (PECVD) [25,26]. Then, SiO_2 and a-Si layers are deposited. The a-Si layer is patterned to form the gate electrode layer. Subsequently, an oxide layer is deposited and anisotropically etched to form a sidewall spacer around the gate. The most important process step is Ni silicide formation. For self-aligned silicidation to form the silicided S/D, the deposition of a thin Ni layer is followed by the low temperature annealing (500 °C, 40 s) process [31,32]. Next, the unreacted Ni layer is removed and the ITS process is performed to form S/D. Implanted dopants are diffused out of silicide at the channel–S/D interface.

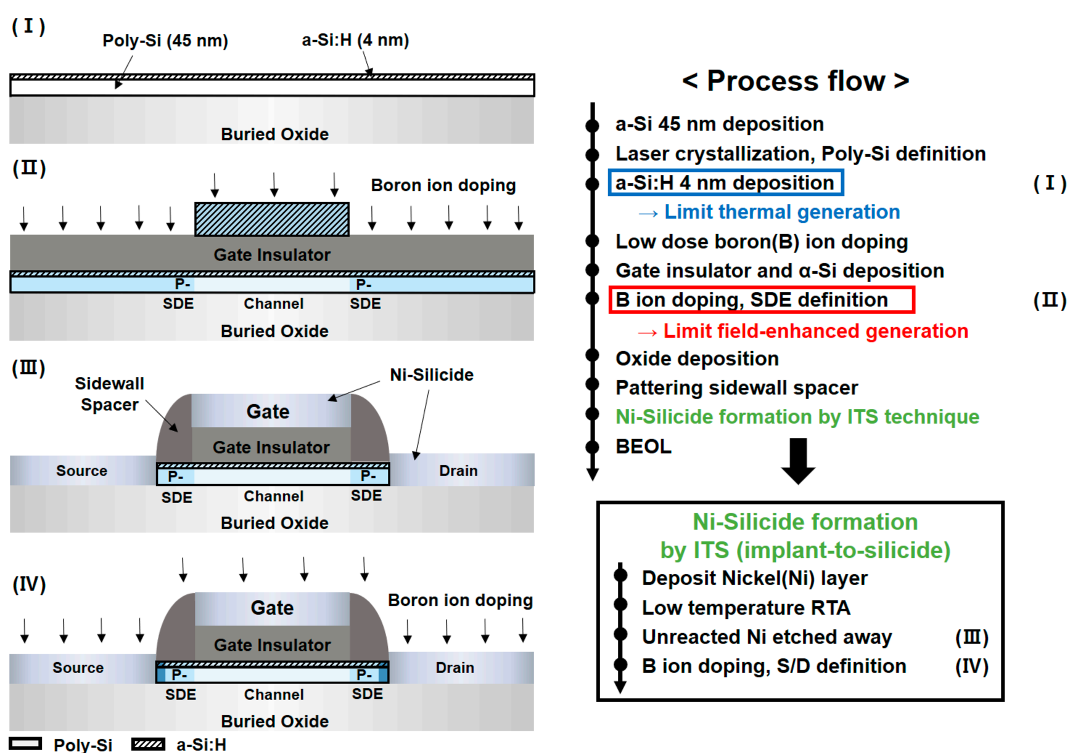

Figure 1. Process flow information and the key process figure of the proposed LTPS TFTs with an amorphous silicon buffer layer and source/drain extension.

3. Device Structure and Simulation Methodology

To investigate the proposed device, a two-carrier and two-dimensional device simulation was performed by using a technology computer-aided design (TCAD) simulator [33]. The Poisson equation, continuity equation, and physics models including charge transports were used to calculate electrostatic potential, carrier flow, and G-R. The Shockley–Read–Hall (SRH) recombination and Hurkx BTBT model considering trap-assisted tunneling, phonon-assisted tunneling, and BTBT were also used.

Figure 2 shows the device structure of the proposed p-type LTPS TFT with a 0.75 µm long SDE and 4 nm thick amorphous silicon buffer layer. Uniform doping profiles are assumed in the poly-Si and amorphous silicon layer. Boron doping concentration at the channel, source/drain, and SDE are 12.3 × 10^{16} cm^{-3}, 1.64 × 10^{19} cm^{-3}, and 4.6 × 10^{17} cm^{-3}, respectively. The thicknesses of the active layer (t_{act}) and the gate insulator (t_{GI}) are 0.045 and 0.12 µm, respectively. The channel width (W) and length (L) are 3.5 and 4 µm, respectively. Device dimensions and doping profiles refer to the literature [15,21]. In addition, 10 nm long highly-doped regions are located between the SDE and silicide region considering dopant segregation whose doping concentration is the same as that of the source/drain region of conventional LTPS TFTs [34]. Detailed device parameters are summarized in Table 1.

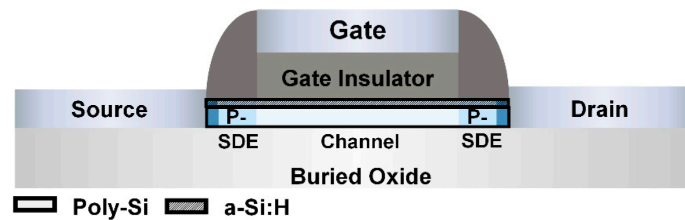

Figure 2. Schematic of the proposed p-type LTPS TFT with an amorphous silicon and source/drain extension.

Table 1. Summarized simulated device parameters.

Material and Device Properties	Symbol	Value	Unit
Thickness of polycrystalline silicon	t_{act}	45	nm
Thickness of amorphous silicon	t_{buf}	4	nm
Bandgap of Poly-Si/a-Si	E_g	1.1/1.8	eV
Thickness of gate insulator	t_{GI}	120	nm
Channel Width/Length	W/L	3.5/4	µm
Length of source/drain extension	L_{SDE}	0.75	µm
Source/Drain doping density	N_{SD}	Boron, 1.64 × 10^{19}	cm^{-3}
SDE doping density	N_{SDE}	Boron, 4.6 × 10^{17}	cm^{-3}
Channel doping density	N_{Ch}	Boron, 2.3 × 10^{16}	cm^{-3}

The subgap density of states (DOSs) of LTPS and amorphous silicon are assumed to be uniformly distributed throughout the poly-Si and amorphous silicon [35–37]. Additionally, the capture cross section for traps is assumed to be 10^{-12} cm^2 in the simulation. The detailed subgap DOS N (E) equation is derived by using the superposition of the exponential tail-level and Gaussian deep-level states as:

$$N(E) = N_{TD} \exp\left(\frac{E_V - E}{W_{TD}}\right) + N_{GD} \exp\left(-\left(\frac{E - E_{GD}}{W_{GD}}\right)^2\right) + N_{TA} \exp\left(\frac{E - E_C}{W_{TA}}\right) + N_{GA} \exp\left(-\left(\frac{E_{GA} - E}{W_{GA}}\right)^2\right), \quad (1)$$

where the N (E) is DOS, E is energy level, E_C is the conduction band minimum, E_V is the valence band maximum, W is the width of the energy distribution, and E_G is the energy of the center of the trap distribution. The subscript A and D mean the acceptor-like and the donor-like DOS, respectively. The subscript T and G mean the tail and the Gaussian

distribution, respectively. The detailed DOS parameters of poly-Si and amorphous silicon are summarized in Table 2.

Table 2. Density of states (DOS) parameters of poly-Si and amorphous silicon (a-Si) [37].

Definition	Symbol	Poly-Si	a-Si	Unit
Density of donor-like tail states	N_{TD}	1×10^{20}	2×10^{21}	cm^{-3}
Density of acceptor-like tail states	N_{TA}	1×10^{20}	2×10^{21}	
Density of donor-like Gaussian states	N_{GD}	4.5×10^{14}	5×10^{18}	
Density of acceptor-like Gaussian states	N_{GA}	1×10^{15}	5×10^{18}	
Slop of donor-like tail states	W_{TD}	0.015	0.021	eV^{-1}
Slop of acceptor -like tail states	W_{TA}	0.012	0.021	
Width of donor-like Gaussian states	W_{GD}	0.15	0.086	
Width of acceptor-like Gaussian states	W_{GA}	0.1	0.086	
Peak energy position of donor-like Gaussian states	E_{GD}	0.6	0.1	eV
Peak energy position of acceptor-like Gaussian states	E_{GA}	0.2	1.7	

4. Simulation Results and Discussion

Figure 3 shows the two simulated structures of the LTPS TFTs with and without 4 nm thick amorphous silicon buffer layer and 0.75 µm long SDE: conventional and our proposed LTPS TFTs. Figure 4 shows the transfer curves of the structures. Our proposed LTPS TFT shows dramatical reduction of off-current with the help of the SDE and amorphous silicon buffer layer. According to the literature [18–21], SDE suppresses field-enhanced generation current under the high electric field condition while wide bandgap materials located between the gate insulator and channel reduces thermal generation current under the low electric field condition. Our proposed LTPS TFT not only reduces leakage current under the high electric field condition, but also lowers the minimum leakage current under low electric field condition with <7% on-current loss. Because both thermal and field-enhanced generation depend on temperature and electric field, they can be investigated separately.

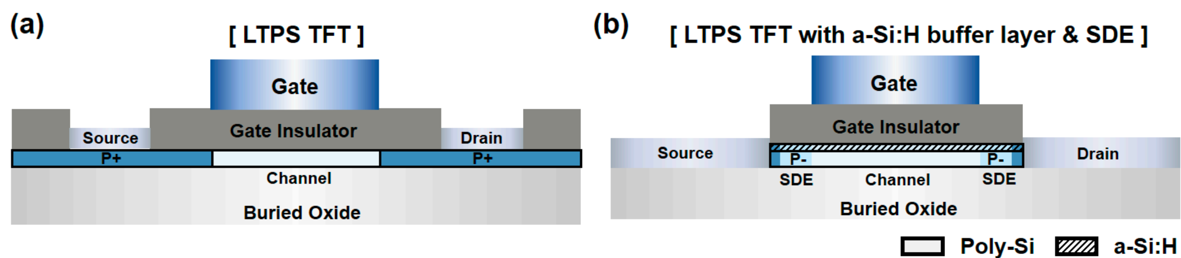

Figure 3. Schematic view of the (**a**) p-type LTPS TFTs and (**b**) proposed p-type LTPS TFTs with an amorphous silicon buffer layer and SDE for TCAD simulation.

The field effect mobility (μ) was calculated by the $g_{m.max}$ method and the threshold voltage (V_{th}) was observed at $I_D = 10^{-7}$ A by constant current method. The μ of TFTs is 73.9 $cm^2/V{\cdot}S$ (LTPS TFT) and 63.82 $cm^2/V{\cdot}S$ for proposed TFT, respectively. In addition, V_{th} is −0.48 V for LTPS TFT and −0.42 V for proposed TFT, respectively. It is observed that conventional LTPS TFT shows higher on-current than the rest of TFTs and that the LTPS TFTs with SDE show the same on-current as our proposed LTPS TFTs. Thus, on-current loss is originated from the SDE rather than an amorphous silicon layer. On the contrary, in the off-state, our proposed LTPS TFTs show the lowest leakage current because thermal generation is suppressed by the amorphous silicon layer. However, as V_G increases, our proposed LTPS TFTs show almost the same leakage current as the LTPS TFTs with SDE because field-enhanced generation is dominant under the high electric field condition.

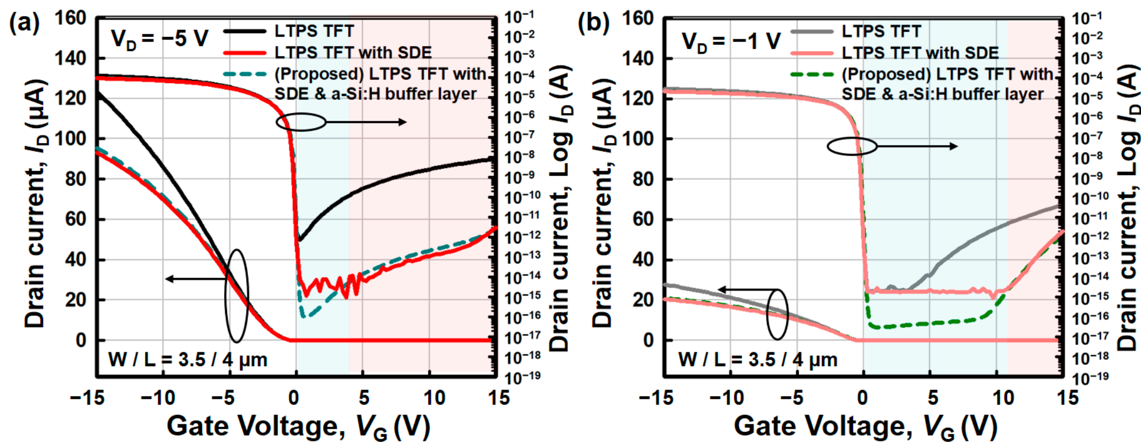

Figure 4. Linear scale (left *Y*-axis) and log scale (right *Y*-axis) transfer (I_D-V_G) curves of a conventional LTPS TFT, LTPS TFT with SDE, and the proposed LTPS TFT with SDE and amorphous silicon buffer layer: (**a**) at $V_D = -5$ V; and (**b**) at $V_D = -1$ V. The blue (red) background are the areas where the thermal (field-enhanced) generation mechanism is dominant.

The main off-current component of LTPS TFTs tunneling is through traps at the near-drain grain boundaries [10–13] which becomes dominant when the electric field exceeds 0.7 MV/cm [11]. Figure 5 compares the electric field distribution of the three kinds of LTPS TFTs along the channel surface. V_G varies from 0 to 15 V while drain voltage (V_D) is fixed at −5 V. It is observed that the LTPS TFTs with SDE have analogous electric field distribution near the gate edge of the gate and that conventional LTPS TFTs show higher electric field peak than the rest of LTPS TFTs. The maximum electric field is ~1.2 MV/cm in the case of conventional LTPS TFTs and 0.5 MV/cm in the case of the rest of LTPS TFTs. From Figures 4 and 5, it can be concluded that the SDE suppresses the field-enhanced tunneling current effectively.

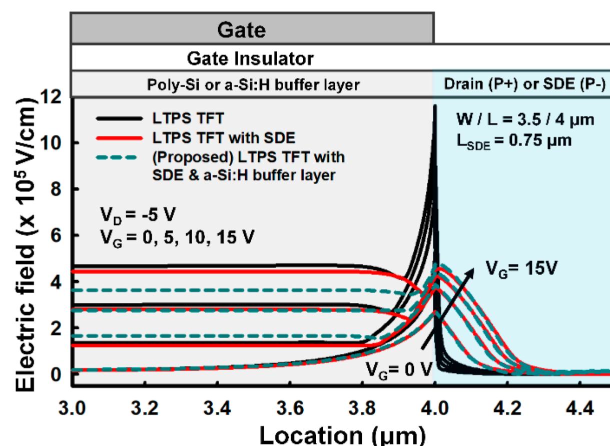

Figure 5. Electric field distributions along the channel interface of a conventional LTPS TFT, LTPS with SDE, and our proposed LTPS TFT in the TCAD simulation. The peak electric fields are distributed between the channel and drain or SDE.

Figure 6 shows the BTBT generation rate including tunneling through traps at $V_D = -5$ V and $V_D = -1$ V. It is observed that drain current (I_D) shows similar behavior to the BTBT generation rate as V_G increases. It means that the major leakage current mechanism under the high electric field condition is the field-enhanced tunneling. In addition, it should be noted that conventional LTPS TFTs show a higher BTBT rate than the rest of LTPS TFTs and that our proposed LTPS TFTs show almost the same BTBT rate as the LTPS TFTs with SDE.

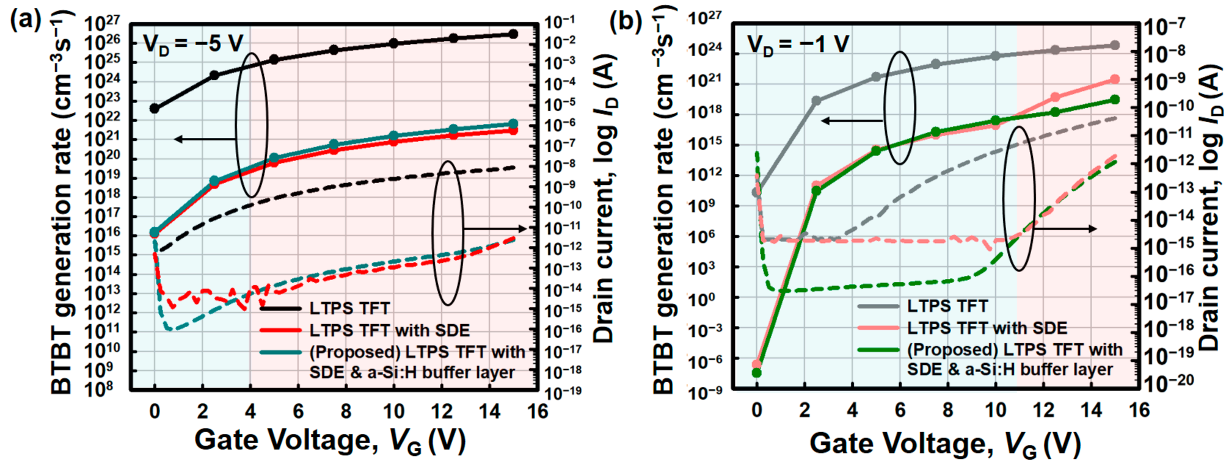

Figure 6. BTBT generation rate (left *Y*-axis) and off-state I_D (right *Y*-axis) of a conventional LTPS TFT, LTPS TFT with SDE, and our proposed LTPS TFT: (**a**) at V_D = −5 V; and (**b**) at V_D = −1 V.

From the above shown simulation results, it can be concluded that under the high voltage condition, the SDE reduces the electric field and tunneling rate while an amorphous silicon layer rarely affects leakage current. It is clearly shown that the role of the SDE is the electric field and tunneling suppression under the high electric field condition. Even if the BTBT rate is lowered by the SDE, it is difficult to lower the minimum leakage current below 10^{-15} A. The LTPS TFTs with and without the SDE have no difference in minimum leakage under the low electric field condition, which means that the dominant mechanism at a low electric field is independent of electric field. The minimum leakage of the LTPS TFTs with SDE is almost the same as that of conventional ones at low V_D. On the contrary, our proposed LTPS TFTs show lower minimum leakage current and higher on/off current ratio than the rest of LTPS TFTs. Thus, it can be concluded that minimum leakage current reduction is originated from the wide bandgap of the amorphous silicon layer.

Off-current is a function of temperature and electrostatic potential barrier height. As V_D and V_G increase, the potential barrier felt by the carriers in traps decreases and trap levels approach the valence and conduction band. Thus, the field-enhanced generation becomes dominant under the high field condition. At low voltage, on the contrary, carriers in the midgap are expected to overcome ~$E_g/2$. Thus, thermal generation becomes more dominant than field-enhanced generation:

Activation energy (E_a) indicates the potential barrier height as shown below:

$$I_D = I_0 \exp\left(\frac{-E_a}{kT}\right), \tag{2}$$

where k is Boltzmann constant and T is absolute temperature. The E_a is extracted as follows:

$$\ln(I_{D2}) - \ln(I_{D1}) = \frac{-E_a}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right). \tag{3}$$

Figure 7 shows the Arrhenius plots of conventional and our proposed LTPS TFTs. It is observed that drain leakage current strongly depends on E_a as a function of V_G. The E_as extracted from Figure 7 are shown as a function of V_G in Figure 8 [13]. E_a depends strongly on V_G and V_D. At V_D = −1 V, the maximum value of activation energy is ~0.55 eV in the case of conventional LTPS TFTs, which corresponds to the potential barrier height required for trap emission. Because E_a is ~$E_g/2$, thermal generation is a dominant leakage mechanism. In addition, in the case of our proposed LTPS TFTs, the E_a is ~0.8 eV at V_G = 0.375 V, which is a typical value of amorphous silicon. Additionally, the proposed LTPS TFTs suppress thermal generation effectively by controlling E_g.

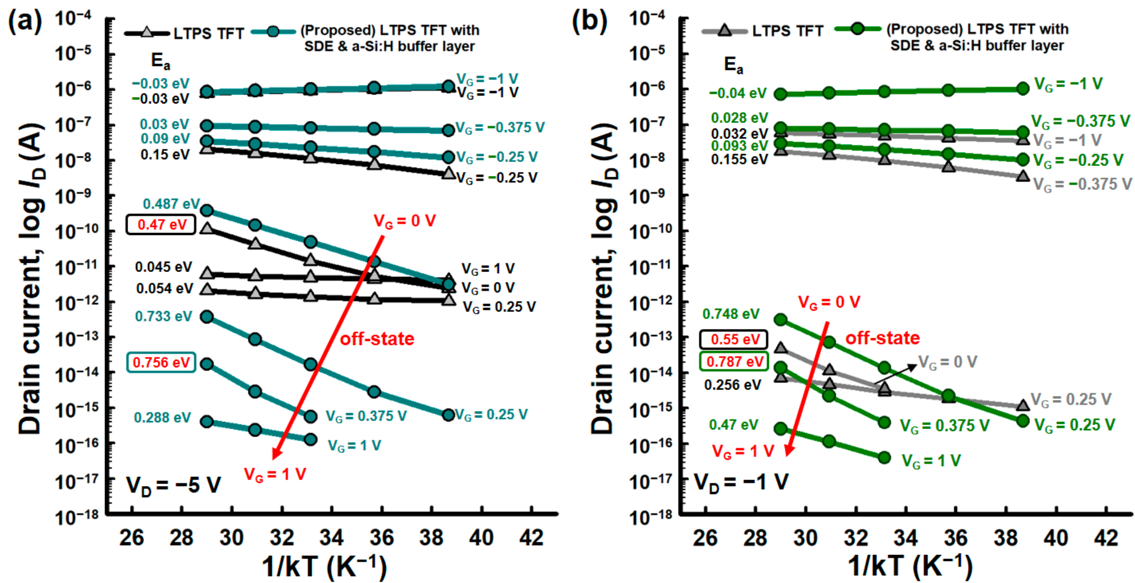

Figure 7. Arrhenius plots (I_D-1/kT) as a function of V_G for T (300, 325, 350, 375, 400 K): (**a**) at V_D = −5 V; and (**b**) at V_D = −1 V. The slopes of each line indicate E_a's.

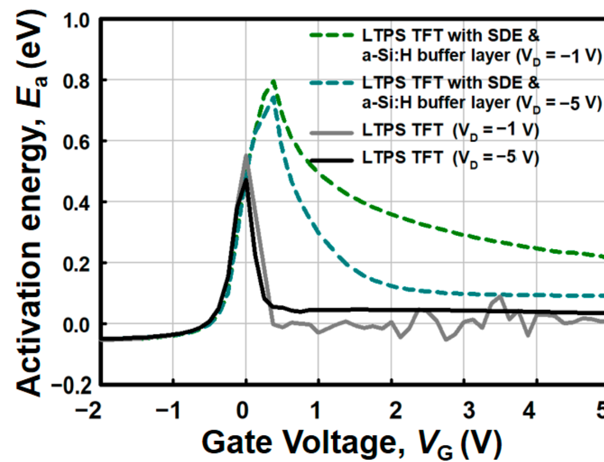

Figure 8. E_a versus V_G of conventional and our proposed LTPS TFTs at V_D = −1 V and V_D = −5 V.

5. Conclusions

A novel LTPS TFT is proposed to reduce the off-state current by suppressing thermal generation and field-enhanced generation with the help of an amorphous silicon buffer layer and SDE. The deposition of the thin amorphous silicon buffer layer on the poly-Si active layer limits thermal generation and reduces the off-state minimum current by three orders of magnitude in high V_D thanks to the increased E_a originated from the large E_g of amorphous silicon. In addition, the lightly doped region near the drain reduces the field-enhanced generation and provides sufficient separation gap between the channel and drain silicide.

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