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Review

Categorization and SEU Fault Simulations of Radiation-Hardened-by-Design Flip-Flops

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Abstract: In the previous three decades, many Radiation-Hardened-by-Design (RHBD) Flip-Flops (FFs) have been designed and improved to be immune to Single Event Upsets (SEUs). Their specifications are enhanced regarding soft error tolerance, area overhead, power consumption, and delay. In this review, previously presented RHBD FFs are classified into three categories with an overview of each category. Six well-known RHBD FFs architectures are simulated using a 180 nm CMOS process to show a fair comparison between them while the conventional Transmission Gate Flip-Flop (TGFF) is used as a reference design for this comparison. The results of the comparison are analyzed to give some important highlights about each design.

Keywords: dual interlocked storage cell (DICE); flip-flop (FF); linear energy transfer (LET); radiation-hardened-by-design (RHBD); single event transient (SET); single event upset (SEU); spatial redundancy; temporal redundancy; triple modular redundancy (TMR)

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1. Introduction

When an energetic particle hits a logic circuit, it can introduce a temporary voltage disturbance due to charge depositing that can upset sensitive circuit nodes and propagate to the successive blocks [1]. Electron-hole pairs are generated corresponding to the strike of an ionizing particle with the transistor nodes, resulting in a generated charge that depends on the Linear Energy Transfer (LET) of the striking particle. At a certain threshold, this charge becomes critical and causes a soft error that flips the logic output [2]. These events are known as Single Event Transients (SETs), and they can be latched by registers causing an error in the stored bits, which is called Single Event Upsets (SEUs) [1,2]. Mitigating SEU is crucial in space and nuclear applications due to the existence of higher energetic particles such as heavy ions and protons [1,3]. Recently, SEU has become a terrestrial problem in modern nanoscale CMOS technology since a small amount of charge can upset the data stored in the Flip-Flops (FFs) [4].

Two techniques can be implemented in the device level of the FF to increase its immunity to SEU that are Radiation-Hardened-by-Process (RHBP) and Radiation-Hardened-by-Design (RHBD) [5]. The first technique is executed at the fabrication process of the CMOS transistors by modifying their geometrical parameters. The other technique concerns the FF architecture such as redundancy and filtering. It is independent of the technology size but results in some overhead in area, power, delay, or cost.

RHBD FFs, in this review, are classified into three different categories; they are spatial redundancy FF that makes different copies of the same FF in space [1,6–9], temporal redundancy FF that compares the signal at different times by adding some delay [10–14], and node hardening FF that strengthens the internal nodes of the FFs and protects them from flipping by soft errors [4,15–22]. Additionally, some FFs can be categorized into multiple categories such as spatial–temporal redundancy FF [7,23–26] or node hardening FF with spatial/temporal redundancy [27,28].

This review focuses on RHBD FFs. First, it introduces the Conventional Transmission Gate FF (TGFF) in Section 2, showing its structure and how it is affected by soft errors. Section 3 classifies the different topologies of RHBD FFs into three main categories. Section 4 presents the simulation results of some selected well-known RHBD FFs regarding their radiation resilience using a 180 nm CMOS process. Finally, Section 5 concludes this review.

2. Conventional Transmission Gate Flip-Flop (TGFF)

Conventional TGFF is a well-known FF topology that is used in many earlier microprocessors and it is a modified version of the popular FF used in the PowerPC 603 processor (NXP Semiconductors, Eindhoven, Netherlands) [29–31]. Figure 1a shows the circuit diagram of TGFF, which consists of a master latch that captures the input D signal when the CLK is low and keeps it when the CLK is high; and a slave latch that operates on the opposite CLK levels as the signal is passed from master latch to slave latch while the CLK is high, and it is kept as long as the CLK is low. Accordingly, the signal has to pass through the master latch during the CLK = 0 and pass through the slave latch during the CLK = 1, which means that the input signal D is only transferred to the output Q when the CLK changes from 0 to 1 (Positive edge of the CLK) as illustrated in Figure 1b.

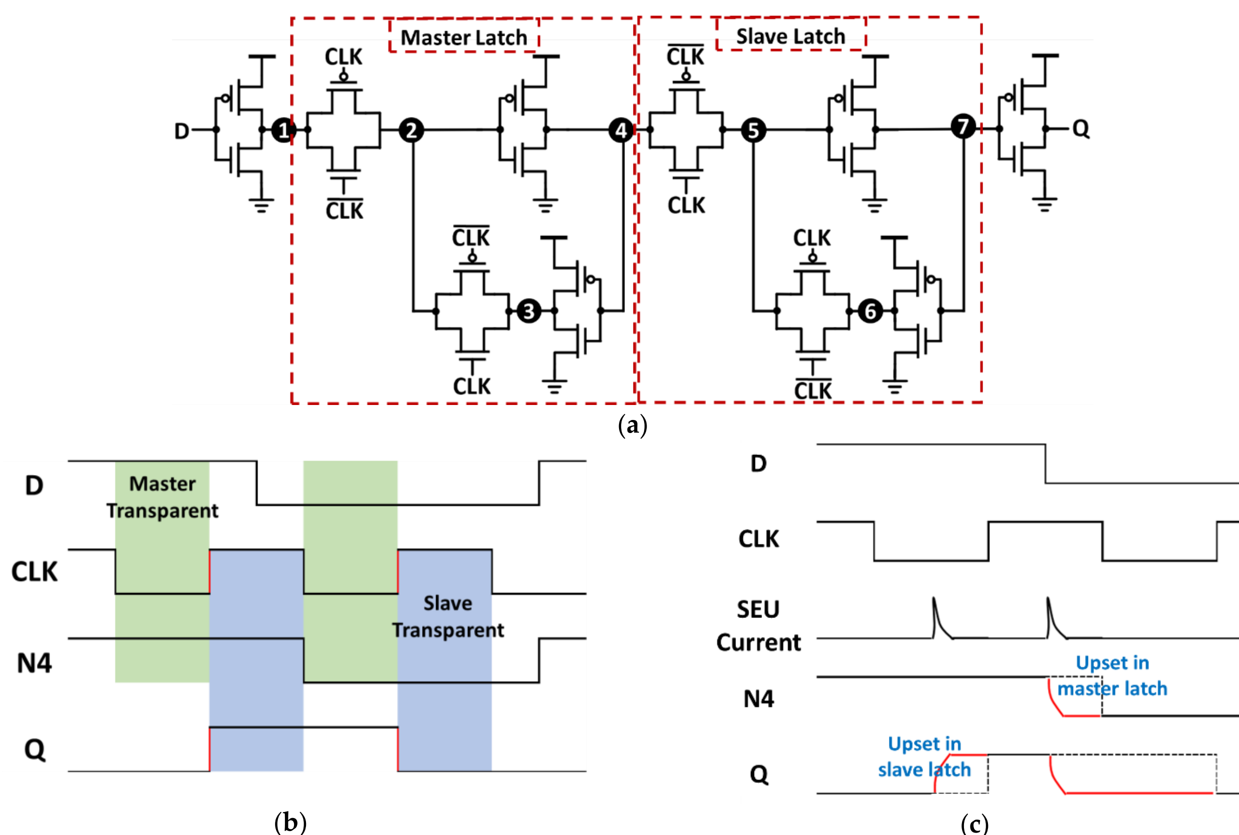


Figure 1. Conventional Transmission Gate Flip-Flop (TGFF): (**a**) TGFF circuit diagram consisting of master and slave latches; (**b**) Waveforms showing the operation of TGFF; (**c**) Effect of Single Event Upset (SEU) on TGFF on both master and slave latches.

Conventional TGFF has a relatively small area and is one of the most power-efficient topologies compared to other master–slave latch-pairs [31], which makes it a good candidate to be used as a benchmark to compare other FFs. However, TGFF is weaker against soft errors by order of ~2× or ~3× than other RHBD FF [32]. The master latch of TGFF can be easily upset by the soft errors that happen when the CLK is high (in the hold state of the master latch) while the slave latch can be upset when the CLK is low (in the hold state of

the slave latch) as shown in Figure 1c. Additionally, soft errors can affect TGFF during the transparent state if this error is propagated and latched by the next latch [6].

3. Radiation-Hardened-by-Design Flip-Flops (RHBD FF)

There are numerous designs for RHBD FF. In this review, we divide them into three main categories, which are spatial redundancy, temporal redundancy, and nodes hardened.

3.1. Spatial Redundancy FF

SEU is collected by a single node at a certain time. Spatial redundancy FF designs make replicas of each logic and check their outputs to detect the error or correct it [6]. XOR gate can be used to compare the output of two redundant FFs and produces an error signal if they do not match. To determine the correct output, a third FF is required, and a majority voter circuit is connected to the output of the three FFs. This design is considered one of the most popular RHBD FFs, which is well-known as Triple Modular Redundancy (TMR) FF, and it is illustrated in Figure 2a [1,7]. TMR FF is very immune to soft errors, but it requires a 3× larger area than the conventional TGFF, and thus exhibiting 3× power consumption overhead.

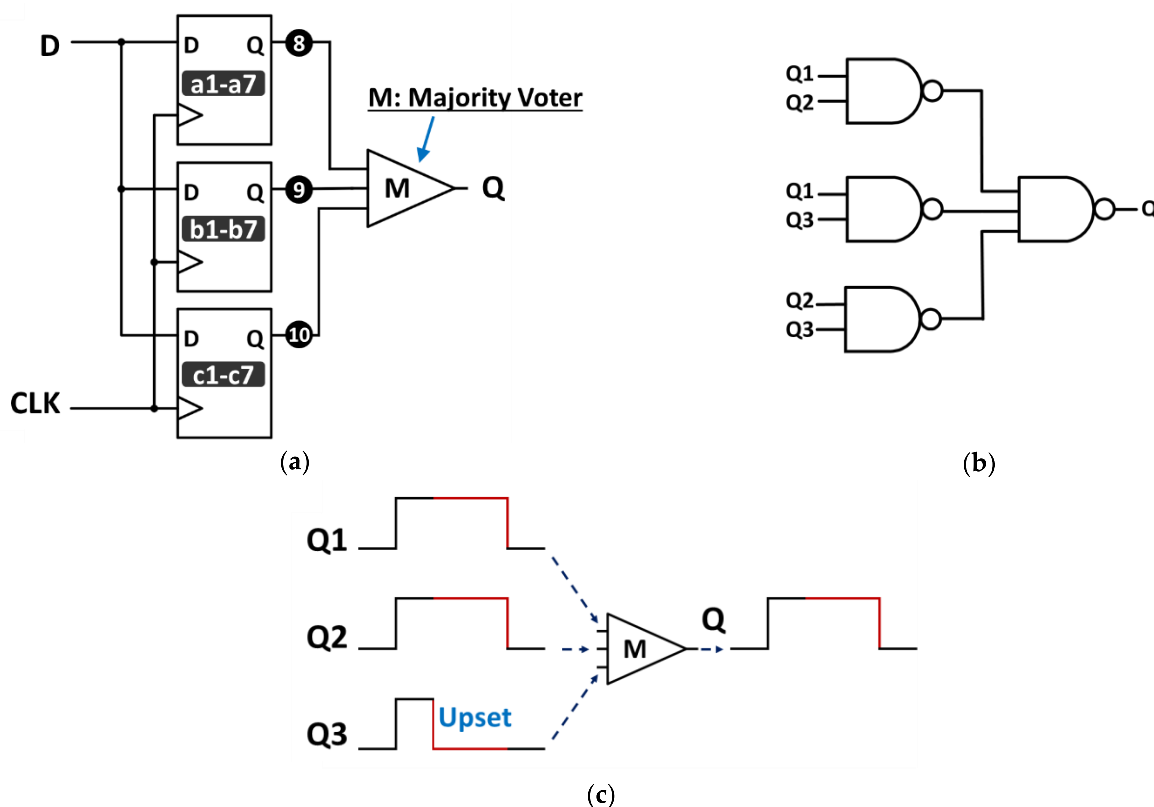


Figure 2. Triple modular redundancy Flip-Flop (TMR FF) votes between three copies of FFs with the same data: (**a**) Circuit diagram of TMR; (**b**) Majority voter circuit; (**c**) The outputs of the three copies are voted to give the final correct output.

TMR stills can fail to SEU in advanced nanoscale technologies due to charge sharing accompanied by the decreased distance between transistors [6]. However, the charge sharing effect can be reduced by proper layout techniques.

The majority voter circuit, shown in Figure 2b, simply consists of two-level NAND gates that generate an output that agrees with any two consistent inputs. If only one FF is upset, the majority voter ignores it and keeps the correct output relying on the other two correct FFs as demonstrated in Figure 2c. Since the voter is connected to the output of the three replicas, if the particle hits the voter circuit with enough charge, it can flip the final output [6]. However, this fault is instantaneous and it is not latched.

3.2. Temporal Redundancy FF

Another technique that can help in countering soft errors is to make delayed replicas at different times of the same signal and vote between them as shown in Figure 3a. This makes the FF resists the SEU effect as long as the delay time is larger than the SEU current period. Figure 3b. shows how the delay time can affect the resilience of the FF to the soft error [10]. On the left side of the figure, the soft error time is less than the delay time which makes the disturbance takes effect at a different time, and at any certain moment, the majority voter circuit sees at least two correct inputs. Accordingly, the FF can tolerate the error by voting between three signals easily. On the other hand, if the soft error time exceeds the delay time, two signals would suffer from disturbance at the same time resulting in a fault at the final output. One major disadvantage of the added delay elements is reducing the maximum allowable frequency that the temporal redundancy FF can operate at. This is because the signal path with the longest delay elements would significantly increase the CLK to Q delay of the FF, which makes it unsuitable for high-speed applications.

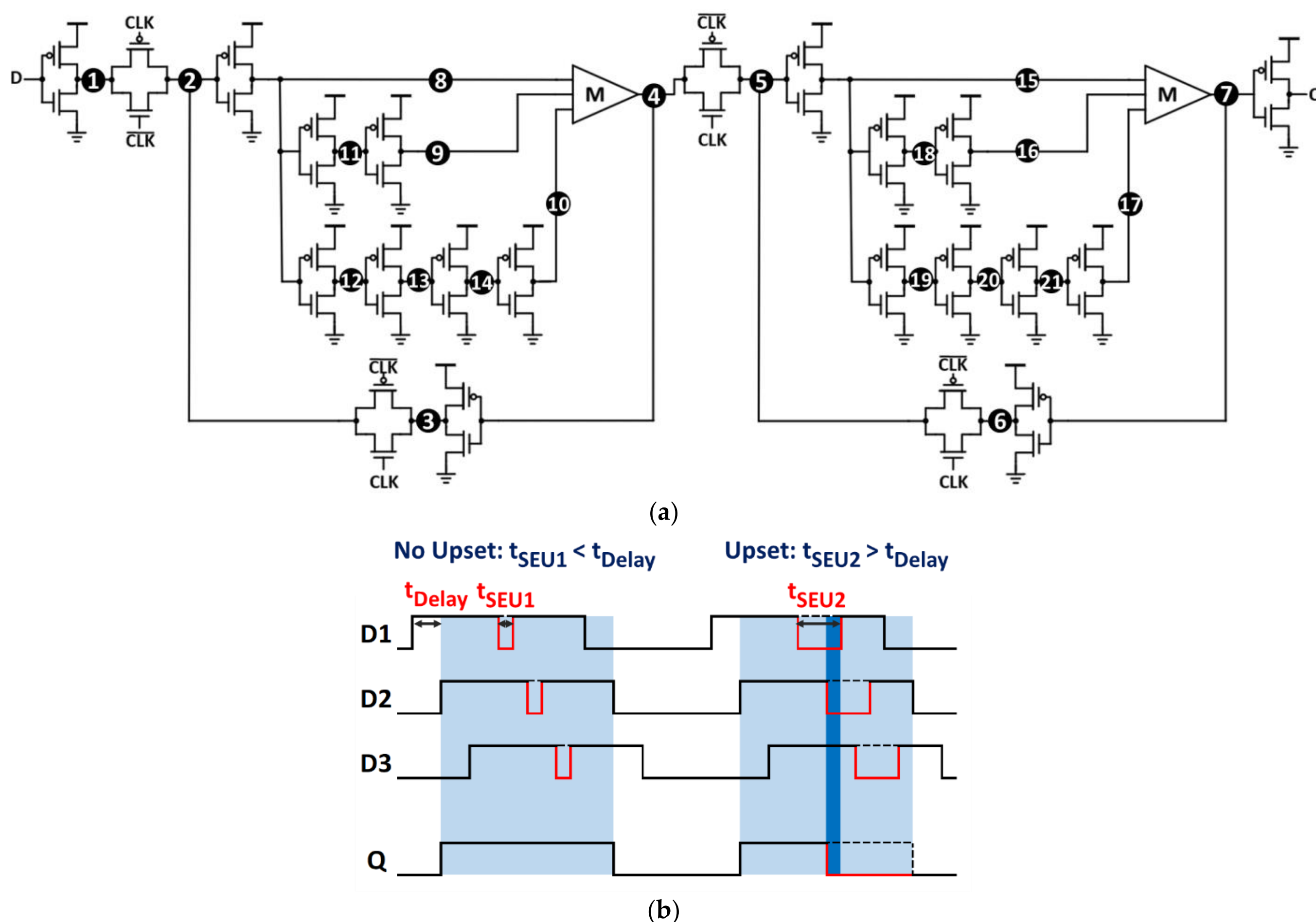


Figure 3. Temporal redundancy FF uses delay elements to get the signal at different times: (**a**) Circuit diagram of a simple temporal redundancy FF; (**b**) The output signal shows how the delay time can tolerate the soft error.

3.3. Node Hardened FF

This category comprises any design technique that relies on protecting or hardening the internal nodes of the FF and makes them difficult to flip by soft errors. Dual Interlocked storage Cell (DICE) FF, shown in Figure 4, is one of the most common techniques in this category.

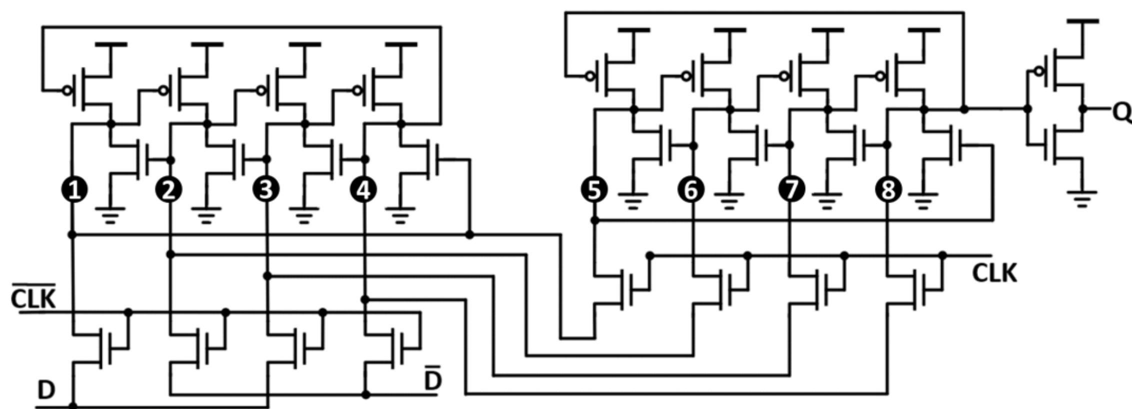


Figure 4. Circuit diagram Dual Interlocked storage Cell (DICE) FF. Two nodes 1 and 3 (or 2 and 4) have to be flipped simultaneously to overwrite the FF stored value.

The logic states of any node in the DICE latch are controlled by two adjacent nodes, so the DICE latch requires two simultaneous nodes with the same logic to be flipped to change its state, while the soft error that hits only one node at a time will be tolerated [15]. DICE is classified here as a node hardened FF; however, it can also be classified as a spatial redundancy FF [4]. There is another node hardened latch that has four storage nodes as a DICE latch, Quatro latch [17].

Node hardening can also be obtained by using stacked inverters instead of standard inverters as it is stronger to soft errors [18]. This method is immune to soft errors when it is used with Silicon on Thin Box (SOTB) process, which prevents the charge sharing effect because a BOX layer isolates transistor channels. Accordingly, the output of the stacked inverters flips only when both of its nMOS transistors are hit by energetic particles at the same time [19]. One drawback of this method is the increased delay because of the duplicated gate capacitance and output resistance compared to conventional FF. In [19,20] other FF designs using stacked transistors are implemented based on the adaptive coupling to reduce the power consumption and delay. A comparison between a stacked transmission-gate FF and a stacked tristate-inverter FF is presented in [22] shows a similar strength to soft errors of both FFs, while stacked tristate-inverter FF has less delay by 21% with a larger area by 9% than the stacked transmission-gate FF.

The fourth structure for node hardening [21] uses an RC filtering structure with an adaptive SEU detecting circuit to control the functions of the switches that automatically control the involved RC filtering structure in the sensitive nodes. This adaptivity makes the system able to select between higher speed or higher SEU immunity based on the detected values of the critical nodes.

3.4. Hybrid Hardened FF

The above three topologies can be combined to construct a hybrid topology. Figure 5a shows a combination of spatial–temporal redundancy FF that consists of TMR FF with delay elements [7]. This temporal-TMR FF can possess a higher soft error immunity even with the charge sharing effect. On the other hand, it suffers from the same size problem of the TMR FF and the speed problem of temporal redundancy FF. Another spatial–temporal redundancy FF is known as Dual Modular Redundancy (DMR) FF, shown in Figure 5b. It depends on two replicas of the conventional FF instead of three replicas as TMR [23]. The outputs of the two copies are connected to a C-element. The truth table of the C-element is shown in Table 1. The C-element delays the change in the final output until both copies of the FF agree together. Accordingly, even if one copy is upset, the final output keeps its previous state. A third spatial–temporal redundancy FF, radiation-hardened scan FF (RH-SFF) [24], corrects soft errors in the sequential element and its preceding combinational logic.

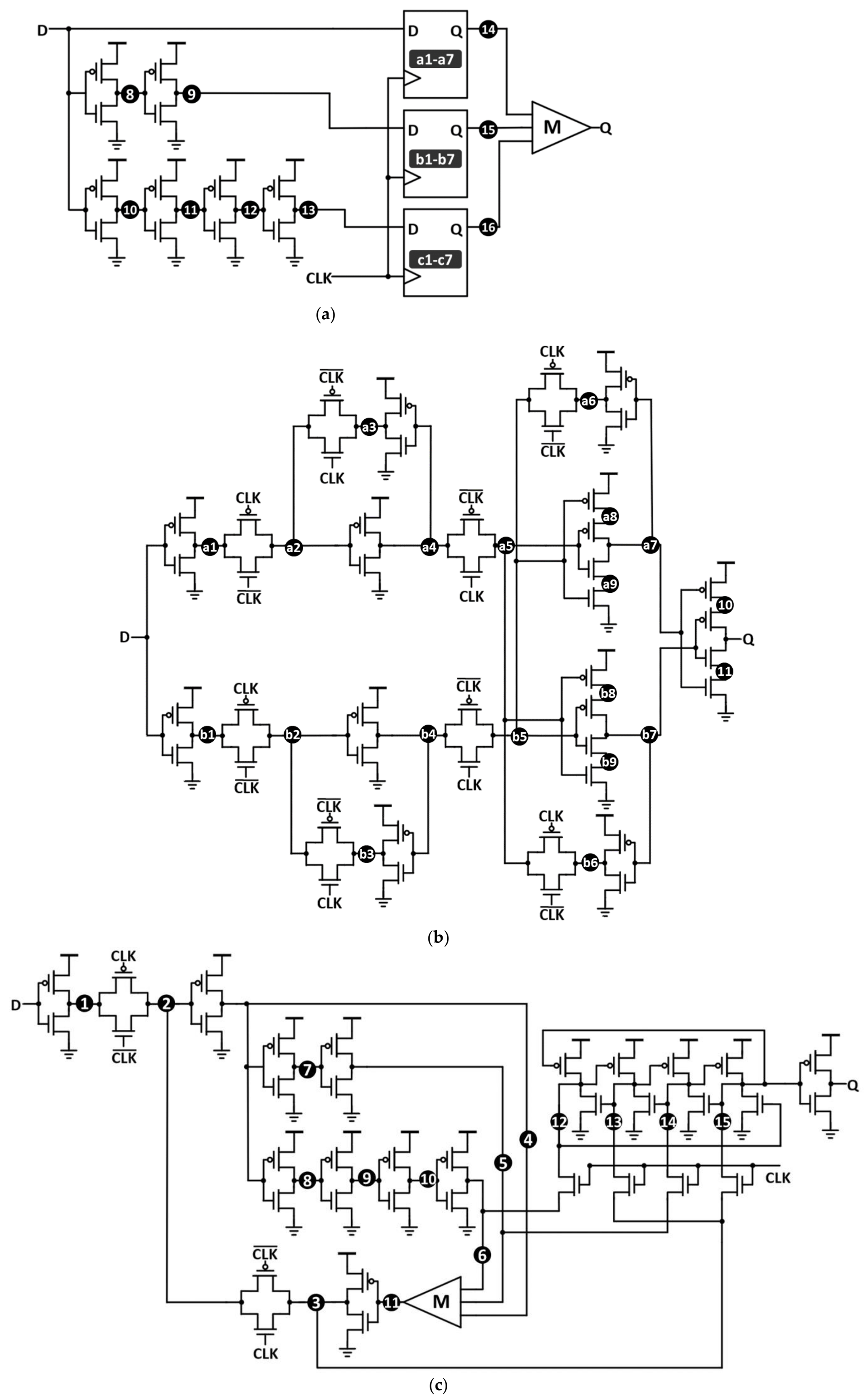


Figure 5. Hybrid FF topologies: (**a**) Circuit diagram of temporal-Triple modular redundancy (TMR) FF; (**b**) Circuit diagram of Dual Modular Redundancy (DMR) FF based on C-element; (**c**) Circuit diagram of temporal-DICE FF.

Table 1. Truth table of the C-element.

A	B	Out
0	0	0
0	1	Float
1	0	Float
1	1	1

One more hybrid topology is shown in Figure 5c, which consists of a temporal master latch and a DICE slave latch [27]. Similar to temporal-TMR FF, the temporal-DICE FF can get the hardening advantages of both DICE and temporal redundancy, but it also suffers from the disadvantages of speed limitations due to delay elements.

4. Results and Measurements

This section shows the simulation results of previously presented seven FF topologies using a 180 nm process to compare their performance and soft error resilience. The use of a large process results in better radiation hardening because of the larger capacitance accompanied by their transistors, which requires a large amount of charge to upset it. This also can help us to compare different topologies without taking into consideration the charge sharing effect that can depend on different layouts. The simulated FFs are TGFF, TMR FF, temporal FF, DICE FF, temporal-TMR FF, DMR FF, and temporal-DICE FF.

4.1. The SEU Testbench

To judge the radiation resilience of the selected FFs, a double-exponential current source in (1) is generated using Verilog-A code to emulate the SEU effect [33]. It is injected at every node in each FF. The tested nodes are shown by numbered circles in Figures 1–5.

$$I_{SEU} = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) \quad (1)$$

here, Q_{coll} is the charge deposited upon the strike of the particle, τ_α and τ_β are the collection and falling time constants, and they are selected to be 200 ps and 50 ps respectively [34,35]. Figure 6a shows the SEU current testbench that is created to test the selected FF while injecting the SEU current at the following cases:

1. Both positive and negative SEU spikes are tested, by changing both Sp and Sn switches simultaneously in Figure 6a.
2. SEU current is injected at the two cases of input D; high input (D = 1) and low input (D = 0) as shown in Figure 6b.
3. For each input case, SEU current is timed at the positive edge of the clock and when the clock level is stable as shown in Figure 6b by the yellow thunder symbols.
4. A wide range of clock frequencies is applied (100 MHz, 250 MHz, 500 MHz, 1 GHz, 2 GHz).
5. An extended range of the deposited charge (Q_{coll}) is used (1 fC to 2.16 pC).

Q_{coll} of 2.16 pC is equivalent to the highest LET of particles that can be found in space (~100 MeV/cm^2/mg) according to (2), while L is the collection depth of ~2 µm [10,34]. It is exceedingly rare to get particles with LET values above ~30 MeV/cm^2/mg [36], which is equivalent to ~650 fC. While many previous works [10,34,35] are reported for Q_{coll} = 100 fC and 150 fC only.

$$dQ\ (fC) = 10.8\ *\ L\ (\mu m) - LET\ \left(MeV/cm^2/mg\right) \quad (2)$$

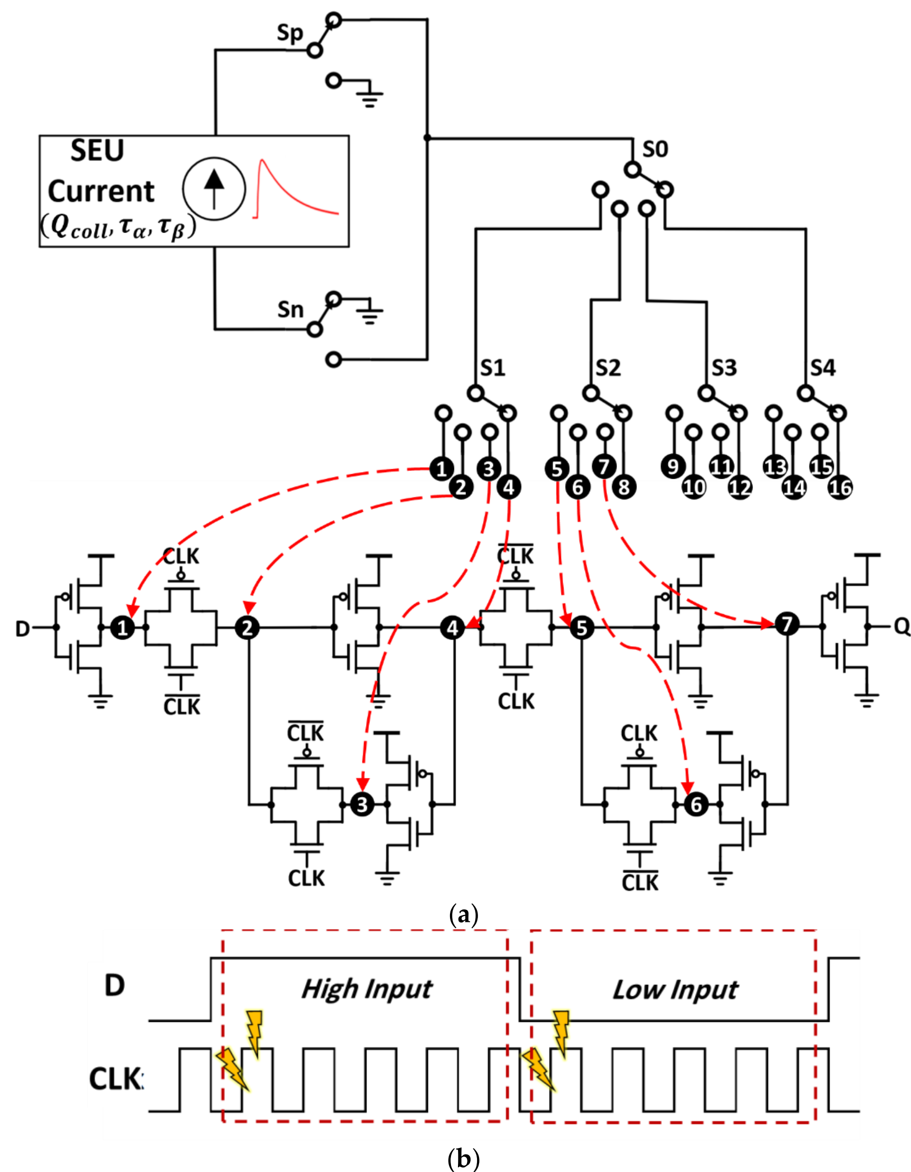


Figure 6. Single Event Upset (SEU) testbench: (**a**) SEU testbench for injecting current at different nodes with both positive and negative polarities; (**b**) Injection time at both high and low D input and edge and level CLK.

4.2. Transistors Sizing and Area

The transistors sizing used in the simulations are illustrated in Table 2; Most nMOS transistors are selected to have a width (W) of 220 nm and length (L) of 200 nm, except for the delay inverters that are set to a width of 4W (=880 nm) and length of 4L (= 800 nm) or 6L (= 1.2 µm). Another sizing is used to enhance the DICE FF by strengthening its pass-transistors using a width of 23 W (= 5.06 µm). All pMOS transistors used the same length as the nMOS transistor but with a 2× larger width. The number of transistors with their width and length for each FF gives a rough estimation of the FF area. It is clear that developing an RHDB FF brings a huge area overhead that sometimes can be 1.5×–2× larger than TGFF, but mostly it becomes higher than 3× than TGFF. Hybrid topologies, especially temporal-TMR FF, suffer from a massive area overhead (>4× larger than TGFF), due to the spatial redundancy in addition to the delay elements. Some RHBD FFs are more area efficient than others. DIEC FF (1) is considered the smallest size RHBD FF between the presented designs. Using DICE FF (1) can save about 64% of the area used by TMR FF.

Table 2. Transistors sizing for the selected Flip-Flops (FFs).

Flip-Flop		TGFF	TMR FF	Temporal FF (1)	Temporal FF (2)	DICE FF (1)	DICE FF (2)	Temporal TMR FF	DMR FF	Temporal DICE FF (1)	Temporal DICE FF (2) [3]
# Transistors	**All**	20	78	80		28		90	44	54	74
	W[1], L[2]	20	78	56		28	20	78	44	42	58
	4W, 4L	-	-	24	-	-	-	12	-	12	-
	4W, 6L	-	-	-	24	-	-	-	-	-	12
	23W, L	-	-	-	-	-	8	-	-	-	4

[1] W of nMOS = 220 nm, W of pMOS = 440 nm. [2] L = 200 nm. [3] Implemented using two majority voters.

4.3. The Simulation Results

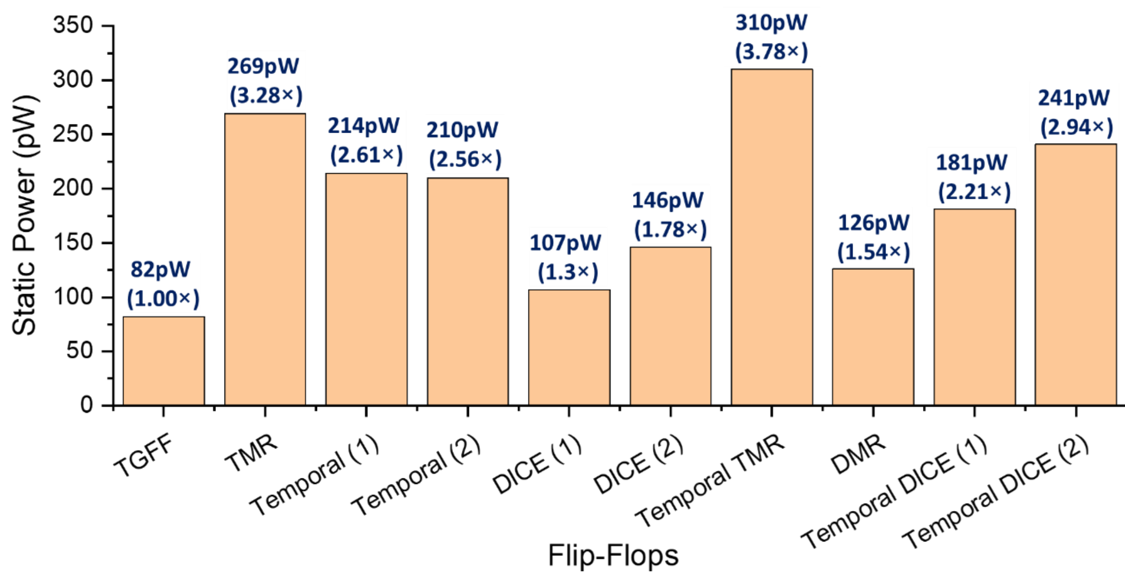
The simulation results of the SEU resilience are summarized in Table 3. TMR FFs always show the highest SEU tolerance at all frequencies. Even if one FF is upset, the other two would stay correctly functioning, and the majority voter circuit would always give the final correct output. On the other hand, TMR FF requires a large number of transistors which leads to a larger chip area. Accordingly, TMR FF and temporal-TMR FF have the highest static power consumption among all the tested FFs, which are 3.28× and 3.78× larger than the static power of TGFF, as shown in Figure 7a. Moreover, they have two of the highest dynamic powers that are 3.03× and 5.28× the dynamic power of TGFF as revealed in Figure 7b.

Table 3. The simulation results of the selected FF for soft error immunity.

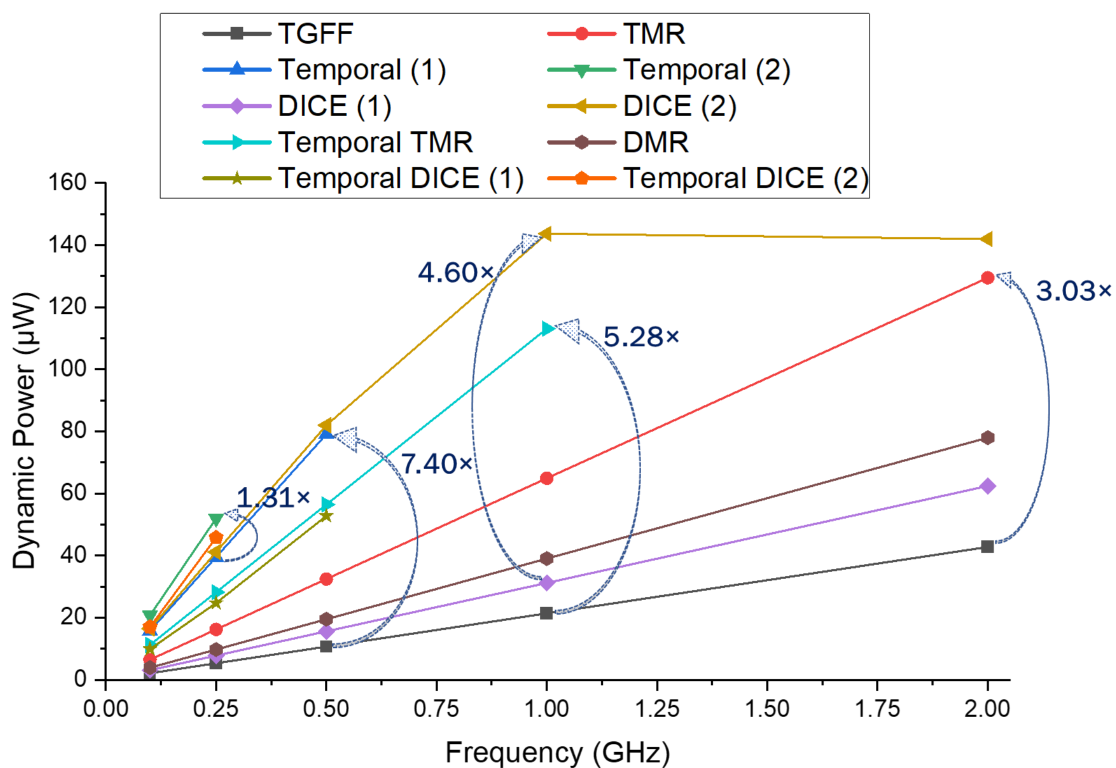
Flip-Flop		TGFF	TMR FF	Temporal FF (1)	Temporal FF (2)	DICE FF (1)	DICE FF (2)	Temporal TMR FF	DMR FF	Temporal DICE FF (1)	Temporal DICE FF (2)
Nodes tested		7	24	21		8		30	20	15	
Critical node		2	-	5		All	8	9	2	2, 5	
$Q_{critical}$ (fC)	**100 MHz**	18	FI [1]	91	171	5 [2]	FI [1]	FI [1]	16 [2]	58	234
	250 MHz	18		60	51	5 [2]			16 [2]	58	40
	500 MHz	18		32	NF [3]	5 [2]			16 [2]	31	NF [3]
	1 GHz	18		NF [3]		5	175	13	16	NF [3]	
	2 GHz	18				5	39	NF [3]	16		

[1] FI = Fully Immune to SEU. [2] Fully immune at the CLK level only. [3] NF = Not Functioning.

Any FF that implements temporal redundancy (temporal FF, temporal-TMR FF, or temporal-DICE FF) has a limitation in functionality (Not functioning) at high CLK frequencies since adding delay elements to the FF increases its propagation delay (CLK-to-Q) delay as shown in Figure 8a, as well as the setup time as shown in Figure 8b. The propagation delay of the temporal FF reaches 7.15× and 11.31× of that of TGFF, depending on the delay elements used, while the setup time is between 6.83× and 10.59× of the TGFF. From Table 2 and Figure 8b, the setup time is directly related to the maximum allowable CLK frequency. The temporal FF (2) and temporal-DICE FF (2), which are using 6L length delay elements, have the highest setup time that exceeds 1ns, and accordingly, they do not operate at 500 MHz or higher frequencies. Furthermore, temporal redundancy FF requires a large area to implement delay elements, and it also suffers from high dynamic power dissipation that is >7.4× of TGFF. In addition, increasing the delay elements makes temporal FF more power-hungry, as shown in Figure 7b, using 6L delay elements increased the dynamic power by 1.31× than the temporal FF with 4L delay elements. However, it is important to notice that increasing the delay time of the delay elements provides higher immunity to SEU. This ensures that the delay times between different data samples are larger than the SEU width, referring to Figure 3b. As shown in Tables 2 and 3, by increasing the length of the delay elements from 4L to 6L, which results in a 1.58× longer propagation delay, the immunity of temporal FF to SEU at 100 MHz increases from 5× to 9.5× times the TGFF.



(**a**)



(**b**)

Figure 7. Power consumption of each selected FF using 2 V supply voltage: (**a**) Static power; (**b**) Dynamic power.

DMR FF and DICE FF show a good performance among other RHBD FFs, regarding their power consumption and propagation delay (1.61× and 0.97× of TGFF) and setup and hold time. Both DMR FF and DICE FF can introduce an excellent SEU tolerance when the spikes hit at a steady-state (at the level of the CLK), but they fail with even week low-charge spikes that hit at the time of the CLK edge. However, the proper sizing of the pass transistors of the DICE FF makes it immune to SEU spikes at both the CLK level and edge especially for frequencies below 1 GHz. On the other hand, increasing the width of pass transistors increased the dynamic power of the DICE FF by 4.6×.

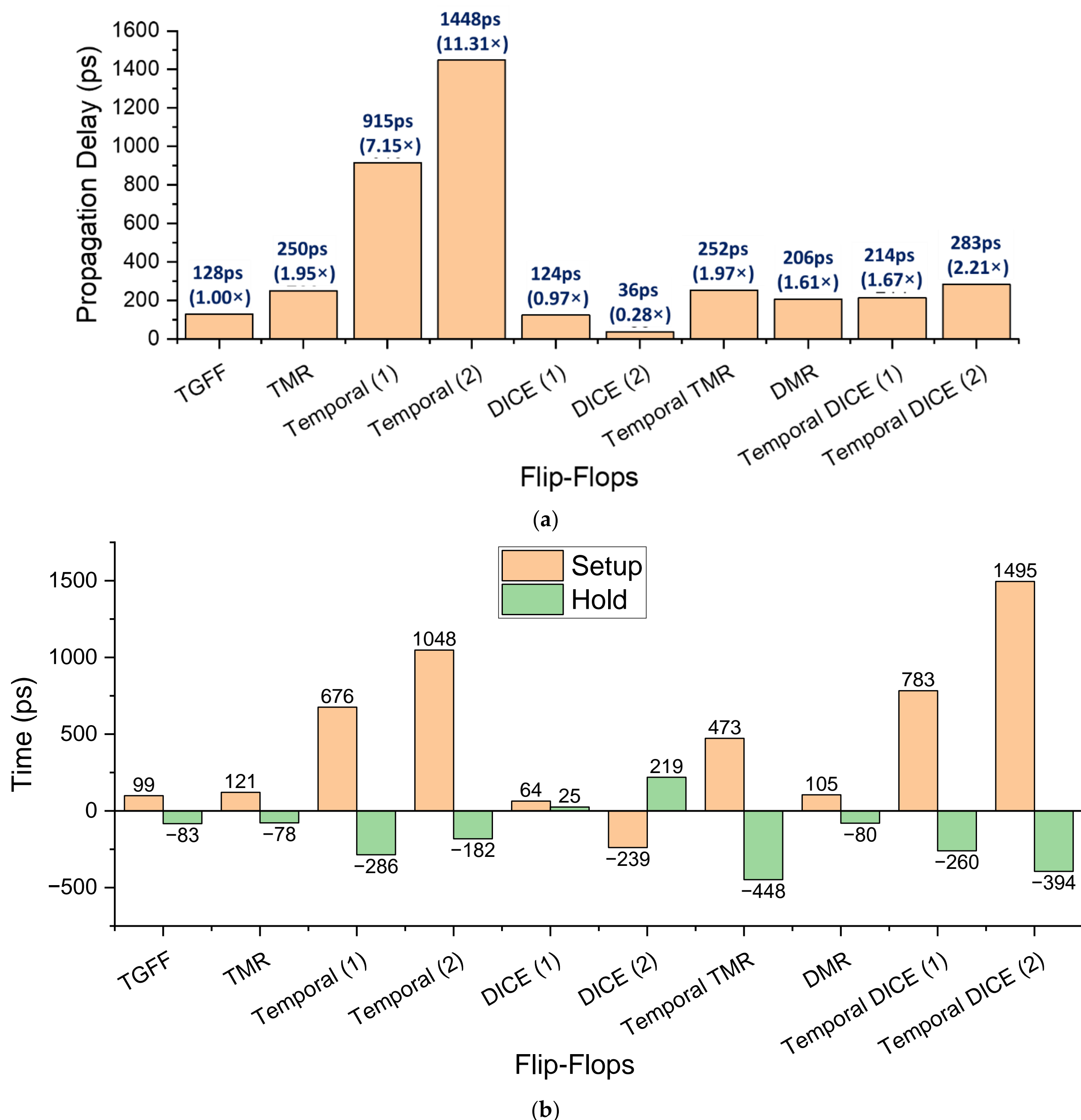


Figure 8. Timing of each the selected FF: (**a**) Propagation delay; (**b**) Setup and hold times.

4.4. Critical Nodes

Another important observation is recorded in Table 3 that is the critical node for each FF. The critical node is selected to be the most frequent node that makes the FF upset with the least charge ($Q_{critical}$). For TGFF, DMR FF, and Temporal DICE FF, it is the 2nd node in the master latch. The pass transistors do not recover the signal coming from node 1 or 3, and thus making node 2 is the easiest node to be upset. For temporal FF, the same problem happens with nodes 2 and 5. Node 5 in the temporal FF comes out from the majority voter circuit, shown in Figure 2b, which has a three-input NAND gate that requires four stacked transistors with additional overdrive voltage. This makes the signal delivered to node 5 is weaker, and thus it is easier to be disturbed and upset the FF. Additionally, node 5 voltage is distributed to the delay paths of the slave latch, which makes it still not protected by the temporal redundancy.

For DICE FF without strengthening the pass transistors, all nodes are sensitive to any small charge. After proper sizing of the pass transistors, node 8 (the last node before the Q output) becomes the critical node at high CLK frequencies (e.g., 1 GHz). For temporal-TMR FF, node 9 appears to be the critical node at 1 GHz CLK frequency. Since node 9 locates at the beginning of the middle delay chain, it can be voted with the first chain before the update of the third chain path happens, which leads to wrong output, and a similar concept is applied to node 5 in temporal-DICE FF. The awareness of the critical nodes of each FF can further help in enhancing their resilience to radiation by utilizing different transistors sizing or enhanced layout techniques.

4.5. Process Corners Simulations

This subsection represents the same simulation results introduced in Section 4.3, but for all process corners (slow–slow (SS), slow–fast (SF), typical–typical (TT), and fast–slow (FS), and fast–fast (FF)). Table 4 shows the critical charge that is required to upset each FF at different frequencies for all corners. SS corner always shows the lowest critical charge while FF corner shows the highest one, however, the difference between them is not very significant, except for DICE that can have about 100fC difference between SS and FF corners. From this table, it can be concluded that the SEU tolerance of the presented RHBD FFs is not process-dependent.

Table 4. The simulation results of the selected FF for soft error immunity showing all process corners (SS, Sf, TT, FS, FF).

<table>
<tr><th colspan="2" rowspan="2">Flip-Flop</th><th rowspan="2">TGFF</th><th rowspan="2">TMR FF</th><th colspan="2">Temporal FF</th><th colspan="2">DICE FF</th><th rowspan="2">Temporal TMR FF</th><th rowspan="2">DMR FF</th><th colspan="2">Temporal DICE FF</th></tr>
<tr><th>(1)</th><th>(2)</th><th>(1)</th><th>(2)</th><th>(1)</th><th>(2)</th></tr>
<tr><td rowspan="5">$Q_{critical}$ (fC) 100 MHz</td><td>SS</td><td>16</td><td rowspan="25">FI [1]</td><td>83</td><td>159</td><td>4 [2]</td><td rowspan="15">FI [1]</td><td rowspan="15">FI [1]</td><td>14 [2]</td><td>55</td><td>197</td></tr>
<tr><td>SF</td><td>18</td><td>78</td><td>177</td><td>4 [2]</td><td>16 [2]</td><td>57</td><td>234</td></tr>
<tr><td>TT</td><td>18</td><td>91</td><td>171</td><td>5 [2]</td><td>16 [2]</td><td>58</td><td>234</td></tr>
<tr><td>FS</td><td>18</td><td>106</td><td>166</td><td>5 [2]</td><td>16 [2]</td><td>65</td><td>233</td></tr>
<tr><td>FF</td><td>21</td><td>97</td><td>186</td><td>5 [2]</td><td>19 [2]</td><td>61</td><td>294</td></tr>
<tr><td rowspan="5">$Q_{critical}$ (fC) 250 MHz</td><td>SS</td><td>16</td><td>47</td><td>41</td><td>4 [2]</td><td>14 [2]</td><td>55</td><td>38</td></tr>
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<tr><td>FS</td><td>18</td><td>63</td><td>51</td><td>5 [2]</td><td>16 [2]</td><td>65</td><td>38</td></tr>
<tr><td>FF</td><td>21</td><td>80</td><td>62</td><td>5 [2]</td><td>19 [2]</td><td>61</td><td>44</td></tr>
<tr><td rowspan="5">$Q_{critical}$ (fC) 500 MHz</td><td>SS</td><td>16</td><td>22</td><td rowspan="15">NF [3]</td><td>4 [2]</td><td>14 [2]</td><td>24</td><td rowspan="15">NF [3]</td></tr>
<tr><td>SF</td><td>18</td><td>33</td><td>4 [2]</td><td>16 [2]</td><td>30</td></tr>
<tr><td>TT</td><td>18</td><td>32</td><td>5 [2]</td><td>16 [2]</td><td>31</td></tr>
<tr><td>FS</td><td>18</td><td>31</td><td>5 [2]</td><td>16 [2]</td><td>31</td></tr>
<tr><td>FF</td><td>21</td><td>43</td><td>5 [2]</td><td>19 [2]</td><td>32</td></tr>
<tr><td rowspan="5">$Q_{critical}$ (fC) 1 GHz</td><td>SS</td><td>16</td><td rowspan="10">NF [3]</td><td>4</td><td>135</td><td>7</td><td>14</td><td rowspan="10">NF [3]</td></tr>
<tr><td>SF</td><td>18</td><td>4</td><td>188</td><td>13</td><td>16</td></tr>
<tr><td>TT</td><td>18</td><td>5</td><td>175</td><td>13</td><td>16</td></tr>
<tr><td>FS</td><td>18</td><td>5</td><td>162</td><td>13</td><td>16</td></tr>
<tr><td>FF</td><td>21</td><td>5</td><td>233</td><td>17</td><td>19</td></tr>
<tr><td rowspan="5">$Q_{critical}$ (fC) 2 GHz</td><td>SS</td><td>15</td><td>4</td><td>26</td><td rowspan="5">NF [3]</td><td>13</td></tr>
<tr><td>SF</td><td>18</td><td>4</td><td>55</td><td>16</td></tr>
<tr><td>TT</td><td>18</td><td>5</td><td>39</td><td>16</td></tr>
<tr><td>FS</td><td>18</td><td>5</td><td>35</td><td>16</td></tr>
<tr><td>FF</td><td>21</td><td>5</td><td>61</td><td>19</td></tr>
</table>

[1] FI = Fully Immune to SEU. [2] Fully immune at the CLK level only. [3] NF = Not Functioning.

The static power has a significant difference between FF and SS corners for all flip-flops, as shown in Figure 9a, however, the dynamic power has less variance, as shown in Figure 9b. Since the dynamic power is in µWs while the static power is in pWs, this makes the dynamic power is dominant and the total power is not affected a lot by the process variations.

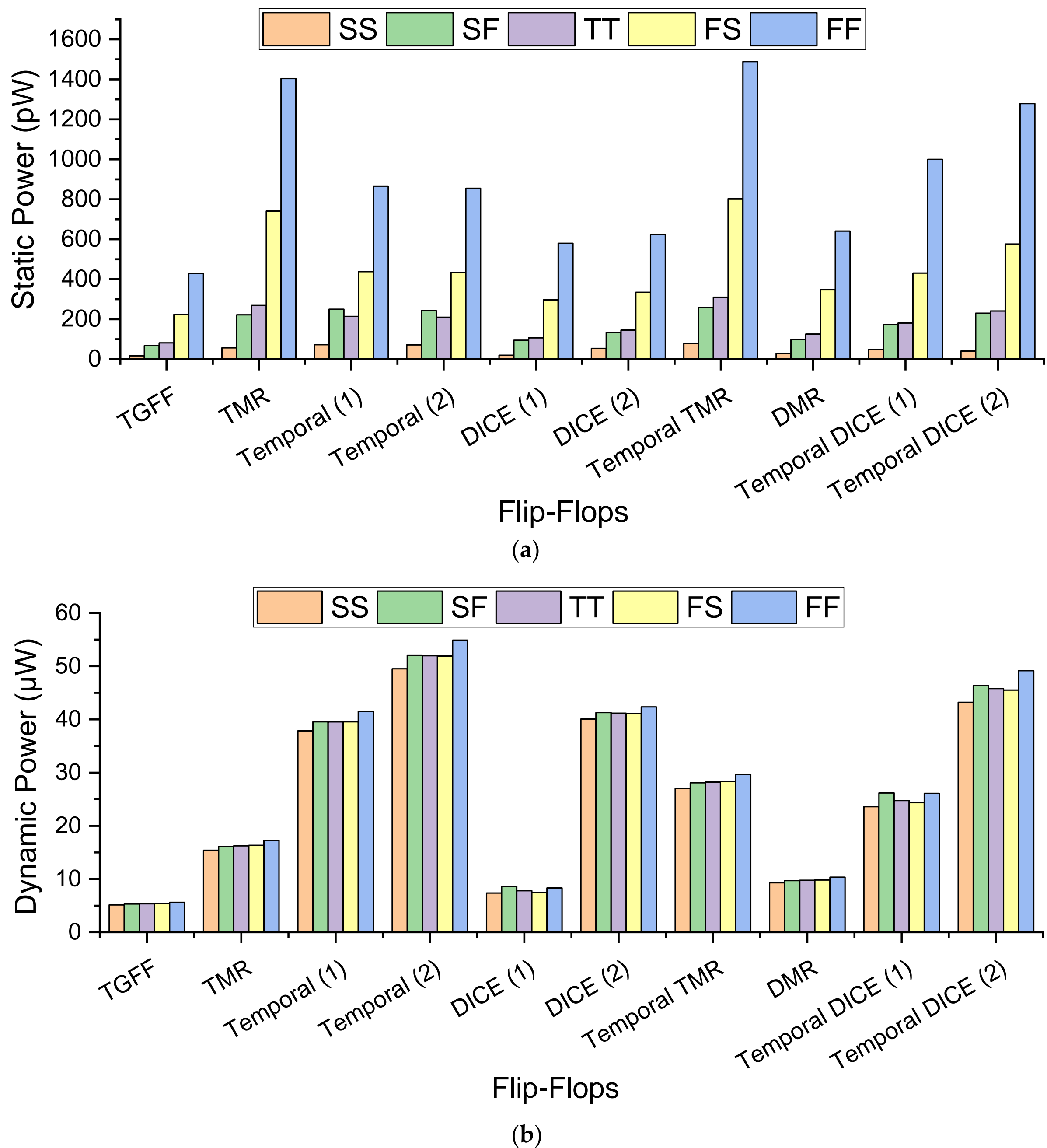

Figure 9. Power consumption of each selected FF showing all process corners: (**a**) Static power; (**b**) Dynamic power.

Finally, Figure 10 shows propagation delay, setup time, and hold time for all corners. The most variance presents in flip-flops that have temporal hardening, especially temporal flip-flop (2). In Figure 10a, temporal flip-flop (2) has the highest propagation delay difference between its two edge corners (496 ps between SS and FF corners).

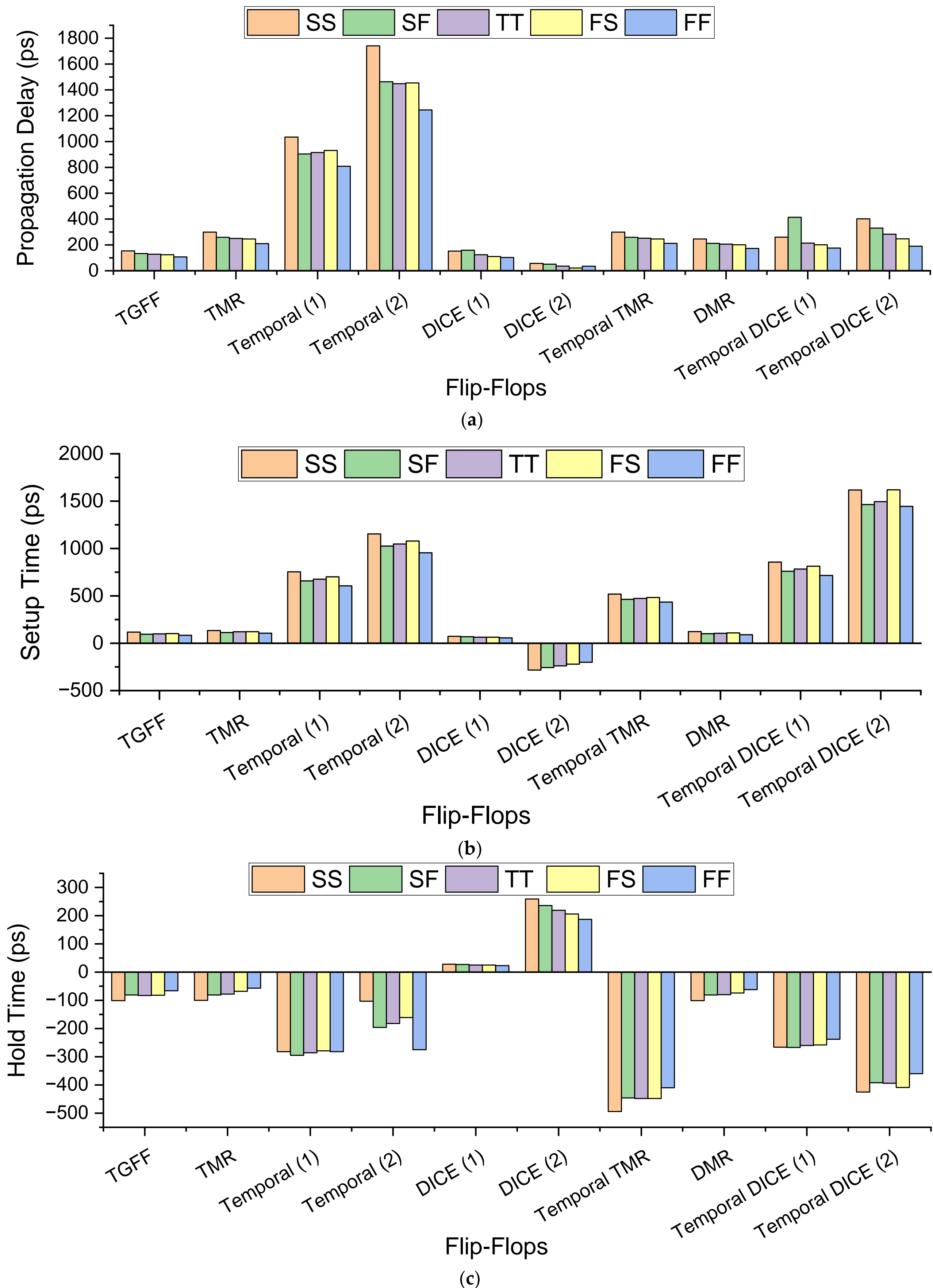

Figure 10. Timing of each the selected FF for all process corners: (**a**) Propagation delay; (**b**) Setup time; (**c**) Hold time.

4.6. Asynchronous Preset/Clear

To examine the timing related to the asynchronous preset/clear in the RHBD FFs, some adjustments are made on TGFF, TMR FF, temporal FF, and DICE FF to add preset/clear inputs. For the first three FFs, which were shown before in Figures 1a, 2a and 3a, four inverters whose inputs are connected to nodes 2, 4, 5, and 7 are swapped by NAND gates that have another input connected to Set (S) signal for asynchronous preset function or Rest (R) signal for asynchronous clear function. This is illustrated in Figure 11a for a modified TGFF.

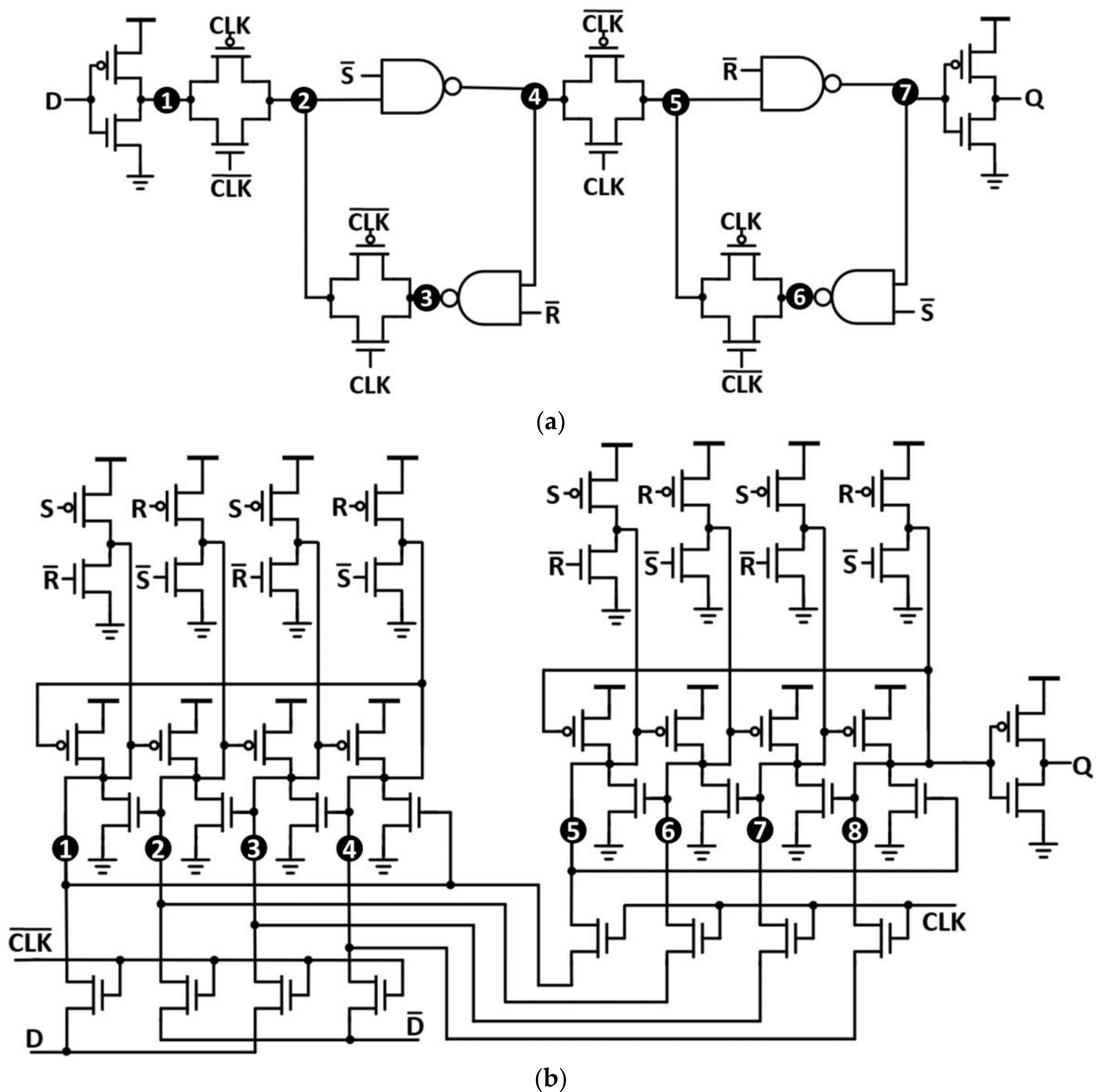

Figure 11. Implementing asynchronous preset/clear inputs in: (**a**) Transmission Gate Flip-Flop (TGFF); (**b**) DICE FF.

A different adjustment is implemented on DICE FF in Figure 11b. In order to preset DICE FF to high, four pMOS transistors are added to force the odd nodes 1, 3, 5, and 7 to the supply voltage, while another four nMOS transistors are added to force the even nodes 2, 4, 6, and 8 to the GND. Similarly, the clear function is implemented by adding additional 8 transistors (4 nMOS and 4 pMOS) in contrarily order.

Figure 12 confirms that temporal FF has longer preset, clear, recovery, and removal times than other FFs, while other FFs have relatively short preset/clear times. The preset and clear times of the temporal FF are at least 5.59× of the TGFF, while the recovery time and the removal times are 28.58× and 12.88× respectively. Moreover, the recovery and removal times change a lot between DICE FF (1) and DICE FF (2) because of the effect of the larger width of the pass transistors in DICE FF (2) on delaying the original CLK signal. However, the period between the recovery and removal time is still relatively small at about 41 ps in DICE FF (2).

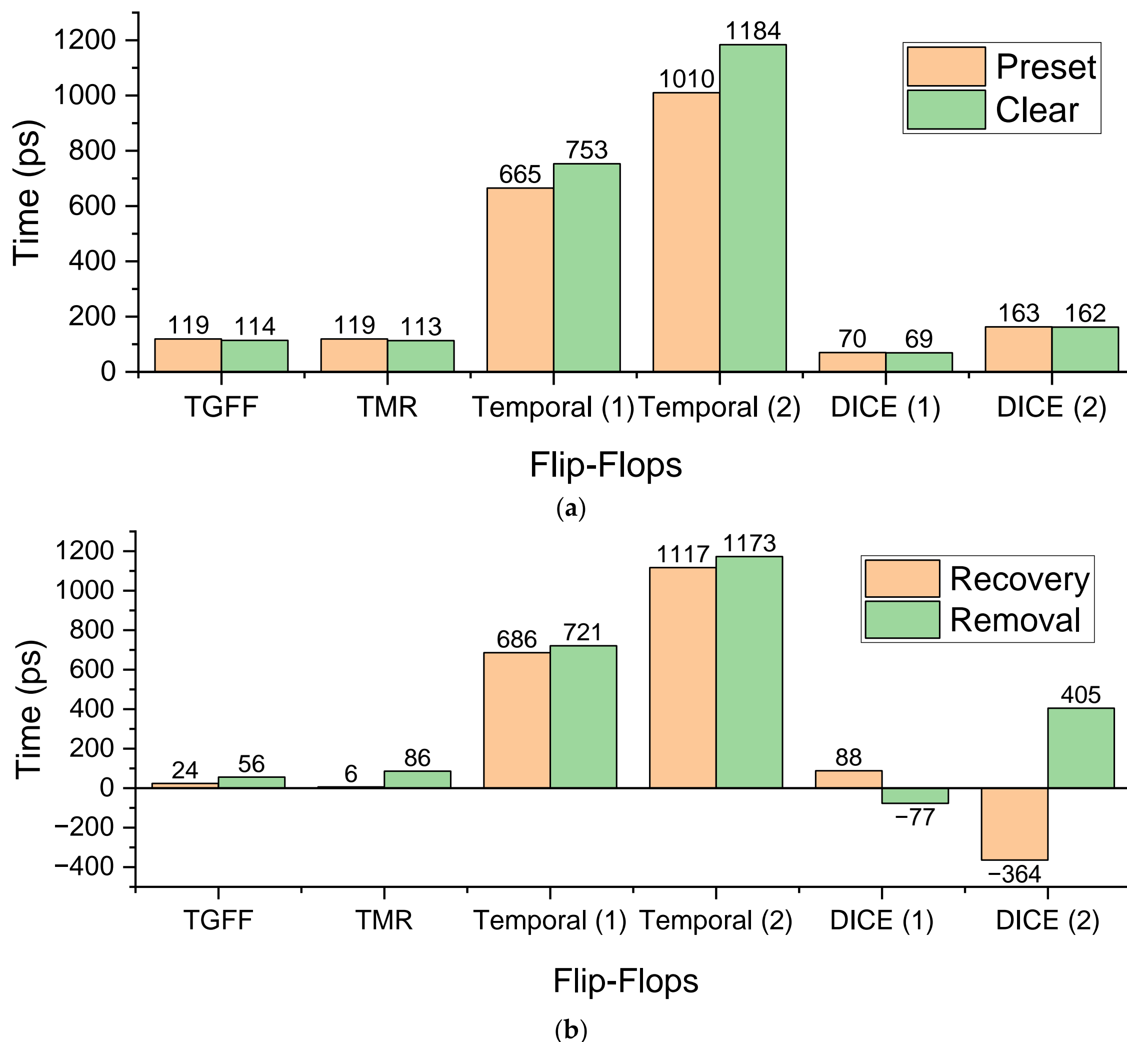

Figure 12. Timing for asynchronous inputs: (**a**) Preset and clear times; (**b**) Recovery and removal times.

4.7. Design for Testability

The RHBD FFs require to be tested after fabrication in a radiation environment, which brings the need to design FFs for testability. Design-For-Testability (DFT) has major importance in chip manufacturing to reduce the testing cost and time. The most popular DFT method for sequential circuits is the fully scanned design [37]. The basic structure of the scan is using the flip-flop with a 2 × 1 multiplexer. This multiplexer selects between the normal mode of operation and the test mode. In the test mode, all FFs in the system are connected in series to form a shift register with serial input and serial output, as shown in Figure 13. This full-scan DFT is easy to be implemented for any of the proposed RHBD FF.

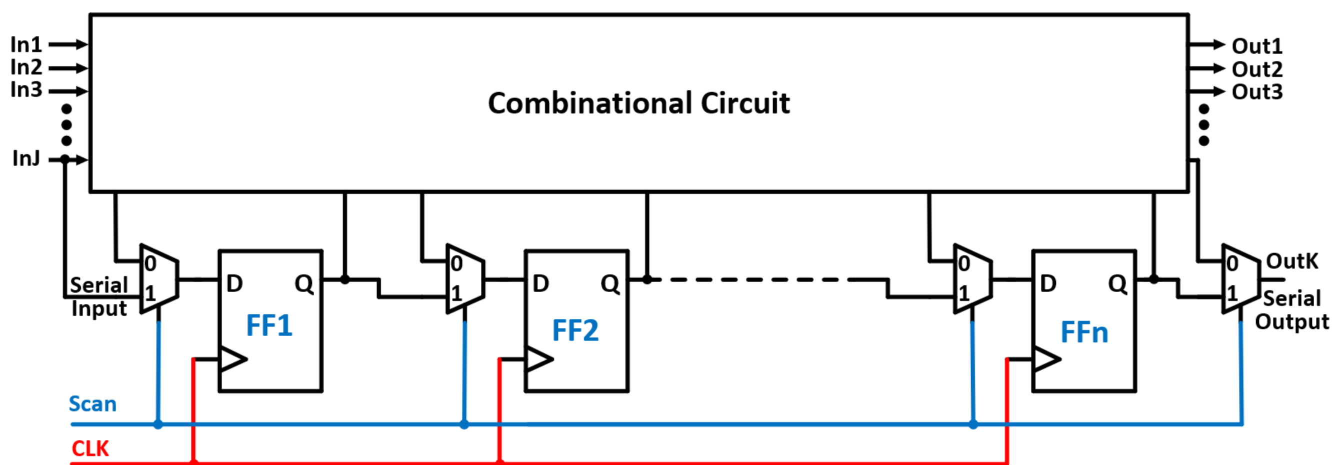

Figure 13. Fully scan design for testability.

5. Conclusions

This review introduces three RHBD FF categories with a basic example of each class and discusses its pros and cons. It also introduces a hybrid category combining any two of the basic three categories with some examples. Six selected RHBD FFs are presented in these categories and are simulated using a 180 nm CMOS process. The comparison shows that spatial redundancy presents the highest soft error tolerance without further sizing, but it exhibits a large overhead area and high power consumption. Temporal redundancy FF suffers from speed limitations due to added delay elements and it has to fulfill the specific delay conditions to become immune to SEU current. DICE FF gives a good balance between soft error tolerance, area, and power but it requires specific sizing for its pass transistors to work properly. A study of the critical node of each FF is also presented showing that nodes coming after tristate gates and nodes at the middle delay chains can be the most critical nodes in each design and should be carefully treated. Some RHBD FFs are adjusted to implement asynchronous preset/clear inputs and their results show that the temporal FF is the only one that suffers from the longest required preset/clear times.

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