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A Dual-Mode InGaP/GaAs HBT Power Amplifier Using a Low-Loss Parallel Power-Combining Transformer with IMD3 Cancellation Method

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Abstract: A dual mode InGaP/GaAs heterojunction bipolar transistor (HBT) power amplifier (PA) using a parallel power-combining transformer (PCT) is presented herein. A low loss transformer is implemented on a printed circuit board (PCB) to improve the passive efficiency of a PCT. Dual-mode operation is applied to reduce the current consumption at a low power level. In the low-power (LP) mode, one of the individual amplifiers is turned off to reduce the current consumption. Additionally, a third-order intermodulation distortion (IMD3) cancellation method using a PCT combiner is proposed to improve linearity performance. Nonlinear IMD3 components from each amplifier cancel each other out through magnetic coupling in the secondary winding of the PCT. The implemented PA achieves a saturated output power of 33.8 dBm and a peak power-added efficiency (PAE) of 54.5% at 0.91 GHz with a 5-V power supply. An average output power of 25.2 dBm with an adjacent channel leakage ratio (ACLR) of −42 dBc is delivered when the PA is tested with an orthogonal frequency division multiplexing (OFDM) 64-quadrature amplitude modulated (64-QAM) signal with a bandwidth of 10 MHz and peak-to-average power ratio (PAPR) of 7.8 dB. When compared with the high-power (HP) mode operation, the LP mode operation could save 48% of the current consumption at an average output power of 10.4 dBm.

Keywords: dual mode; power amplifier; power-combining transformer; IMD3 cancellation

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1. Introduction

With the exponential growth of modern wireless communications, current wireless systems are built with the aim of achieving high-speed data rates. Signals with high-order quadrature amplitude modulations (QAMs) are typically required to achieve these high data rates. These signals have high peak-to-average power ratios (PAPRs) and require highly linear operations of power amplifiers (PAs) in transmitters. Power-combining methods have been widely used to combine the output power from individual amplifiers so as to increase the output power of the PA. Among the power-combining passive networks, transformer-based power-combining methods are the preferred solution, because transformers can enable impedance transformation in addition to balun operation. Series power-combining transformers (SCTs) are the most popular configurations in power-combining transformers [1–9]. In SCTs, multiple primary windings are connected to individual amplifiers, and the output power from each primary winding is magnetically coupled with a secondary winding in series. In Reference [9], the SCT was implemented on a printed circuit board (PCB) to improve the passive loss. Another popular power-combining transformer is the parallel power-combining transformer (PCT) [10–13]. Herein, the output power from each primary winding is magnetically coupled with a secondary winding in a parallel configuration. A PCT configuration can be implemented in an area

smaller than that for an SCT configuration. Hence, in this work, to minimize the loss of the output-combining transformer with a relatively smaller area, a parallel power-combing transformer is implemented on a PCB, providing a thicker *Cu* layer with a flame retardant 4 (FR4) substrate. Compared with the PA design using an on-chip transformer in [14], the PA design using the transformer on a PCB improves output power and efficiency performances owing to the improvement of the transformer efficiency. The output power level of the PA design using a PCT is much higher than that of [14] by adding the output power from multiple primary windings of the transformer. In addition, a dual-mode operation using a PCT is applied in a high-Q PCB transformer to reduce the current consumption at a lower power level.

Although many studies on PAs using CMOS technology have focused on replacing heterojunction bipolar transistor (HBT)-based PAs, the achievement of comparable circuit performances using CMOS technology continues to be challenging. Thus, HBT-based PAs are widely used in current handset products. Power amplifiers in femto-cell base-station applications require highly linear operations compared with typical PAs in handset applications [15]. A third-order intermodulation distortion (IMD3) cancellation method using parallel-combined transistors was proposed with an inductor-capacitor (LC) output matching in [16] to improve the linearity performance using HBT technology. It can also be applied using power-combining transformers. An SCT-based output combiner was used to cancel the IMD3 components in [8]. In this work, an IMD3 cancellation technique using a PCT combiner is proposed wherein the nonlinear components from each primary winding cancel each other out at the secondary winding of the PCT.

The remainder of this paper is organized as follows. Section 2 describes the analysis of the PCT with a high-Q output combiner and the dual-mode operations. In Section 3, the analyses of the proposed IMD3 cancellation mechanism using a PCT combiner are described. Section 4 discusses the measurement results of this work. Finally, Section 5 concludes the paper.

2. Low-Loss Dual-Mode Parallel Power-Combining Transformer

Figure 1 shows the equivalent non-ideal circuit model of a parallel power-combining transformer. L_{p1} and R_{p1} represent the net resistance and self-inductance, respectively, of the primary winding connected to PA1.

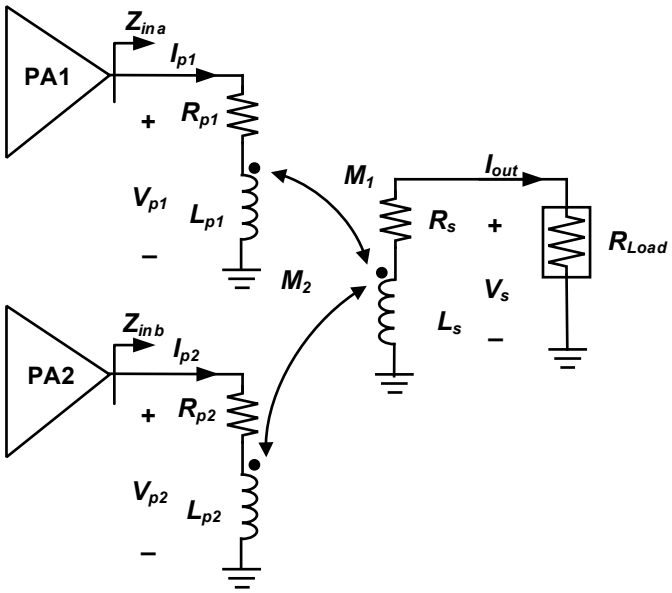


Figure 1. Equivalent non-ideal circuit model of a parallel power-combining transformer.

Similarly, L_{p2} and R_{p2} represent those of the primary winding connected to PA2. L_S and R_S are used to model the secondary winding. The voltages of the primary and secondary windings (V_{p1}, V_{p2}, and V_s) can be expressed as

$$\begin{bmatrix} V_{p1} \\ V_{p2} \\ V_s \end{bmatrix} = \begin{bmatrix} R_{p1}+j\omega L_{p1} & 0 & -j\omega M_1 \\ 0 & R_{p2}+j\omega L_{p2} & -j\omega M_2 \\ j\omega M_1 & j\omega M_2 & -(R_s+j\omega L_s) \end{bmatrix} \cdot \begin{bmatrix} I_{p1} \\ I_{p2} \\ I_{out} \end{bmatrix} \quad (1)$$

$$V_{p1} = \left(R_{p1}+j\omega L_{p1}\right)\cdot I_{p1} - j\omega M_1 \cdot I_{out} \quad (2)$$

$$V_{p2} = \left(R_{p2}+j\omega L_{p2}\right)\cdot I_{p2} - j\omega M_2 \cdot I_{out} \quad (3)$$

$$V_s = j\omega M_1 \cdot I_{p1} + j\omega M_2 \cdot I_{p2} - (R_s+j\omega L_s)\cdot I_{out} = R_{Load}\cdot I_{out} \quad (4)$$

where

$$I_{out} = \frac{j\omega M_1 \cdot I_{p1} + j\omega M_2 \cdot I_{p2}}{R_s + R_{Load} + j\omega L_s}$$

R_{Load} is the load impedance and is typically 50 Ω. The input impedances looking into the transformer of PA1 and PA2 (Z_{ina} and Z_{inb}) are as follows:

$$Z_{ina} = \frac{V_{p1}}{I_{p1}} \equiv R_{ina} + jX_{ina} = \frac{\left(R_{p1}+j\omega L_{p1}\right)\cdot(R_s+R_{Load}+j\omega L_s) + \omega^2\cdot {M_1}^2 + \omega^2 \cdot M_1 M_2 \cdot \frac{I_{p2}}{I_{p1}}}{R_s+R_{Load}+j\omega L_s} \quad (5)$$

$$Z_{inb} = \frac{V_{p2}}{I_{p2}} \equiv R_{inb} + jX_{inb} = \frac{\left(R_{p2}+j\omega L_{p2}\right)\cdot(R_s+R_{Load}+j\omega L_s) + \omega^2\cdot {M_2}^2 + \omega^2 \cdot M_1 M_2 \cdot \frac{I_{p1}}{I_{p2}}}{R_s+R_{Load}+j\omega L_s} \quad (6)$$

where R_{in} and X_{in} are the real and imaginary parts, respectively, of Z_{in}. R_{ina} and R_{inb} are expressed as

$$R_{ina} = R_{p1} + \frac{(R_s+R_{Load})\cdot\omega^2\cdot\left({M_1}^2 + M_1 M_2 \cdot \frac{I_{p2}}{I_{p1}}\right)}{(R_s+R_{Load})^2 + (\omega L_s)^2} \quad (7)$$

$$R_{inb} = R_{p2} + \frac{(R_s+R_{Load})\cdot\omega^2\cdot\left({M_2}^2 + M_1 M_2 \cdot \frac{I_{p1}}{I_{p2}}\right)}{(R_s+R_{Load})^2 + (\omega L_s)^2} \quad (8)$$

The efficiency of the parallel power-combining transformer can be expressed as

$$\eta_{PCT} \equiv \frac{|I_{out}|^2\cdot R_{Load}}{|I_{p1}|^2\cdot R_{ina} + |I_{p2}|^2\cdot R_{inb}} = \frac{\left\{\omega M_1\cdot|I_{p1}| + \omega M_2\cdot|I_{p2}|\right\}^2\cdot R_{Load}}{\left\{(R_s+R_{Load})^2+(\omega L_s)^2\right\}\cdot\left\{R_{p1}\cdot|I_{p1}|^2 + R_{p2}\cdot|I_{p2}|^2\right\} + \omega^2\cdot(R_s+R_{Load})\cdot\left\{M_1\cdot|I_{p1}| + M_2\cdot|I_{p2}|\right\}^2} \quad (9)$$

A linear PA is typically modeled as a current source. Because both PA1 and PA2 are turned on in the HP mode, both of the current sources (I_{p1} and I_{p2}) are excited into the transformer. Thus, the transformer efficiency for the high-power (HP) mode (i.e., $I_{p1} = I_{p2}$), when $L_{p1} = L_{p2} = L_p$, $R_{p1} = R_{p2} = R_p$, and $M_1 = M_2 = M$, can be expressed as follows:

$$\eta_{PCT}\left(I_{p1} = I_{p2}\right) = \frac{(2\omega M)^2\cdot R_{Load}}{\left\{(R_s+R_{Load})^2 + (\omega L_s)^2\right\}\cdot 2R_p + \omega^2\cdot(R_s+R_{Load})\cdot(2M)^2} \quad (10)$$

In addition, because PA1 is turned on while PA2 is turned off in the low-power (LP) mode, only the current source I_{p1} is excited into the transformer. Thus, the transformer efficiency for the LP mode (i.e., $I_{p2} = 0$) when $L_{p1} = L_{p2} = L_p$, $R_{p1} = R_{p2} = R_p$, and $M_1 = M_2 = M$ can be expressed as follows:

$$\eta_{PCT}\left(I_{p2} = 0\right) = \frac{(\omega M)^2\cdot R_{Load}}{\left\{(R_s+R_{Load})^2 + (\omega L_s)^2\right\}\cdot R_p + \omega^2\cdot(R_s+R_{Load})\cdot M^2} \quad (11)$$

Figure 2 depicts the plot of the calculated transformer efficiencies in the HP and LP modes for the PCT. All the transformer design parameters are determined by considering

the values extracted from the physical layout geometries of a PCB. The mutual inductances are selected as $M = k\sqrt{L_p \cdot L_s}$ (k = 0.57). The inductances and resistances of the primary and secondary windings are set as L_p = 4.9 nH, L_s = 10.8 nH, $R_p = \omega L_p/Q_p$, and $R_s = \omega L_s/Q_s$ (quality factor $Q_p = Q_s = 40$). The calculated efficiencies for both the HP and LP modes are higher than 80% at 0.91 GHz. The calculated efficiencies for the two modes for different Q values are plotted in Figure 3. The efficiency of the PCT can be increased with an increase in the Q value, in both the HP and LP modes. As can be seen in (10) and (11), the transformer efficiency is inversely proportional to R_p and R_s. With the selected design parameters of L_p and L_s, the increase in Q_p and Q_s values decrease R_p and R_s, resulting in the increase in the transformer efficiency. Thus, a low-loss power combing transformer can be obtained using a high-Q PCB.

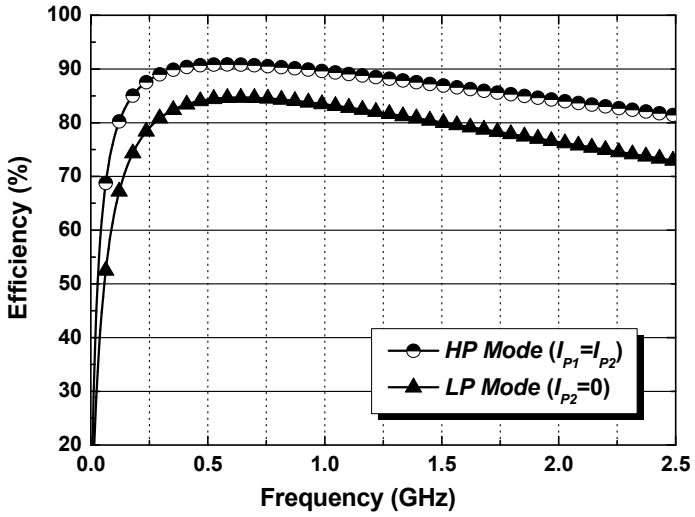


Figure 2. Calculated transformer efficiencies for HP and LP modes for the PCT.

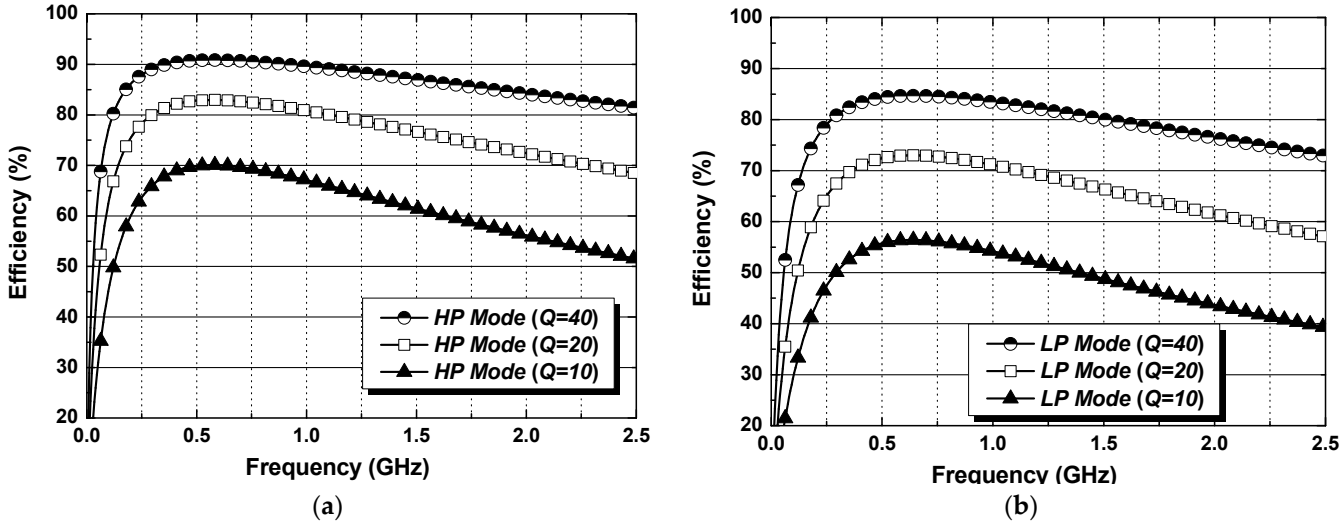


Figure 3. Transformer efficiencies of the PCT calculated for different Q values (**a**) HP mode (**b**) LP mode.

Figure 4 shows a 3D view of the proposed PCT using a four-layer FR4 PCB. The size of the PCT is 2.2 mm × 2.2 mm.

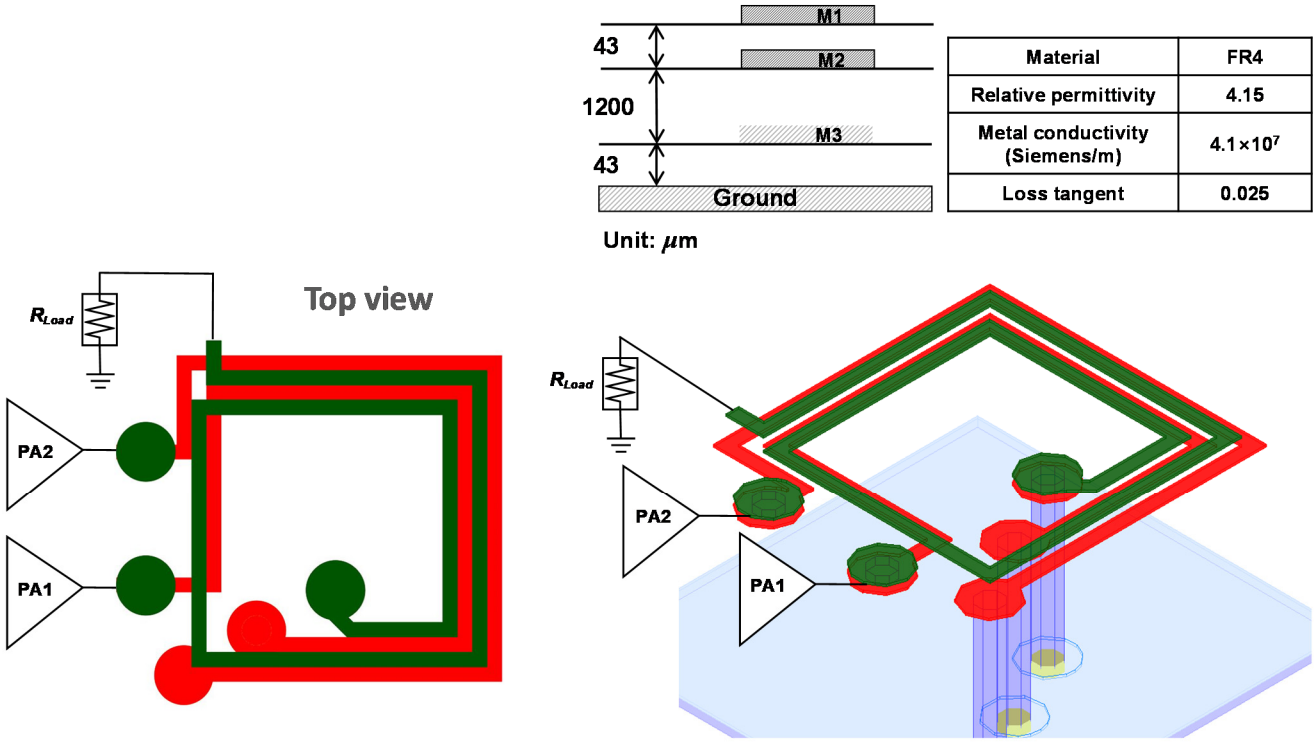


Figure 4. Layout of the PCT structure and layout information of the PCB.

Two primary windings with a width of 100 μm are designed using an M2 metal layer. The spacing between the two primary windings is 100 μm. For the interconnection, PA1 and PA2 are connected to the primary windings through an M1–M2 via. The M1 top metal layer is used for the construction of the two-turn secondary winding with a width of 100 μm. The electromagnetic (EM) simulated insertion losses in the HP and LP modes are plotted in Figure 5. The insertion loss, which is the inverse of the maximum available gain, has been used to evaluate the transformer efficiency [17]. The EM simulated insertion losses in the HP and LP modes are 0.27 dB and 0.45 dB, respectively.

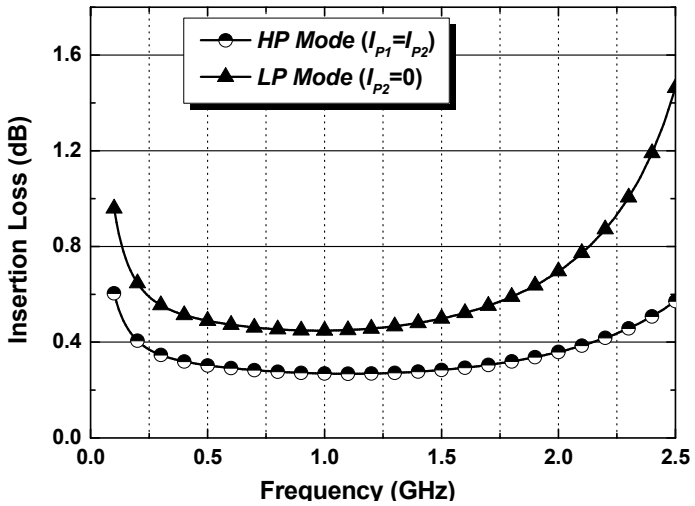


Figure 5. EM simulated insertion loss in HP and LP modes for the PCT.

3. IMD3 Cancellation with Parallel Power-Combining Transformer

Transmitters in femto-cell base-station applications require highly linear PAs to satisfy their stringent ACLR specification. An IMD3 cancellation using a PCT combiner is proposed to satisfy the stringent ACLR requirement, as shown in Figure 6.

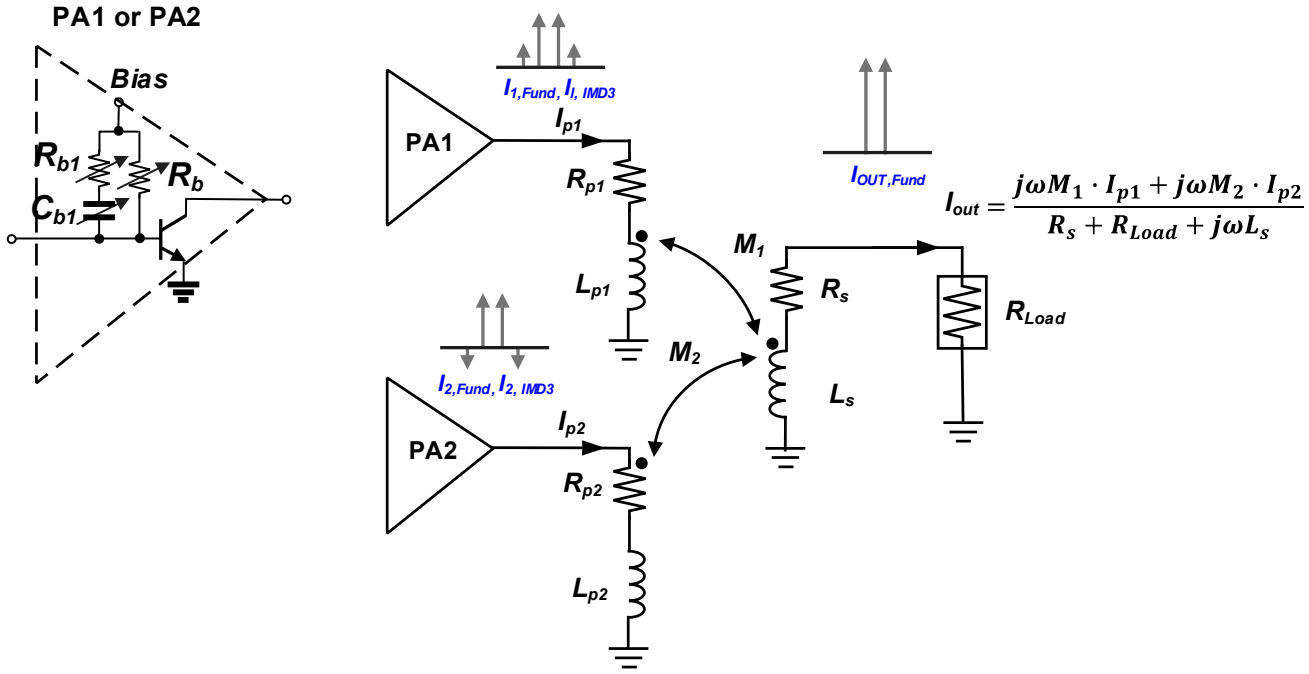


Figure 6. Proposed IMD3 cancellation method using a parallel power-combining transformer.

As described in Equation (4), the currents from each primary winding are added at the output secondary winding through the magnetic couplings of the PCT. With the appropriate selection of R_b, R_{b1}, and C_{b1} in PA1 and PA2, the phase difference between the fundamental components of the currents from PA1 and PA2 is approximately 0° [16]. The phase difference between the IMD3 components of the currents from PA1 and PA2 is approximately 180° [16]. Thus, the fundamental components of the currents from PA1 and PA2 are added up at the output load. The nonlinear IMD3 components of the currents from PA1 and PA2 cancel each other out at the output. For the configuration of each unit cell in PA1 and PA2, a ballast resistor R_b is inserted to prevent thermal runaway of the HBT transistors. In addition, resistors R_{b1} and C_{b1} are incorporated to form bypass circuits and compensate for the decrease in the base voltage of the HBT transistor [18].

Figure 7 shows the total schematic of the proposed HBT PA with a parallel power-combining transformer. With the appropriate value of $R_{b,PA1}$, $R_{b1,PA1}$, and $C_{b1,PA1}$ in PA1 and $R_{b,PA2}$, $R_{b1,PA2}$, and $C_{b1,PA2}$ in PA2, the phase difference of the IMD3 currents from PA1 and PA2 can be approximately 180°. Thus, the IMD3 currents will cancel each other out at the output. In contrast, the phase difference of the fundamental currents from PA1 and PA2 will be approximately 0° and the fundamental currents will be summed up at the output. For the bias circuit, an active bias circuit topology is applied to compensate for the distortion [18–20]. An on-chip *LC* input matching and inter-stage matching are indicated with shaded boxes in Figure 7. A driver stage is included to provide sufficient gain of the total PA. Because the changes in R_b, R_{b1}, and C_{b1} also change the bias currents of PA1 and PA2, different sizes of HBT transistors are selected for PA1 and PA2. Thus, additional matching components (off-chip inductor and capacitor) are added to PA2. The phase change owing to the additional matching circuits is also included in the circuit simulation (see Figure 7). The two-tone simulation with a signal having a tone spacing of 10 MHz has been performed at 0.91 GHz. As shown in Figure 8, the phase difference in the fundamental currents between PA1 and PA2 is less than 30° for an output power of up to

27.3 dBm. Thus, the fundamental currents from PA1 and PA2 can be added to the secondary winding at the PCT. Figure 9 shows the simulated phase of the IMD3 current components.

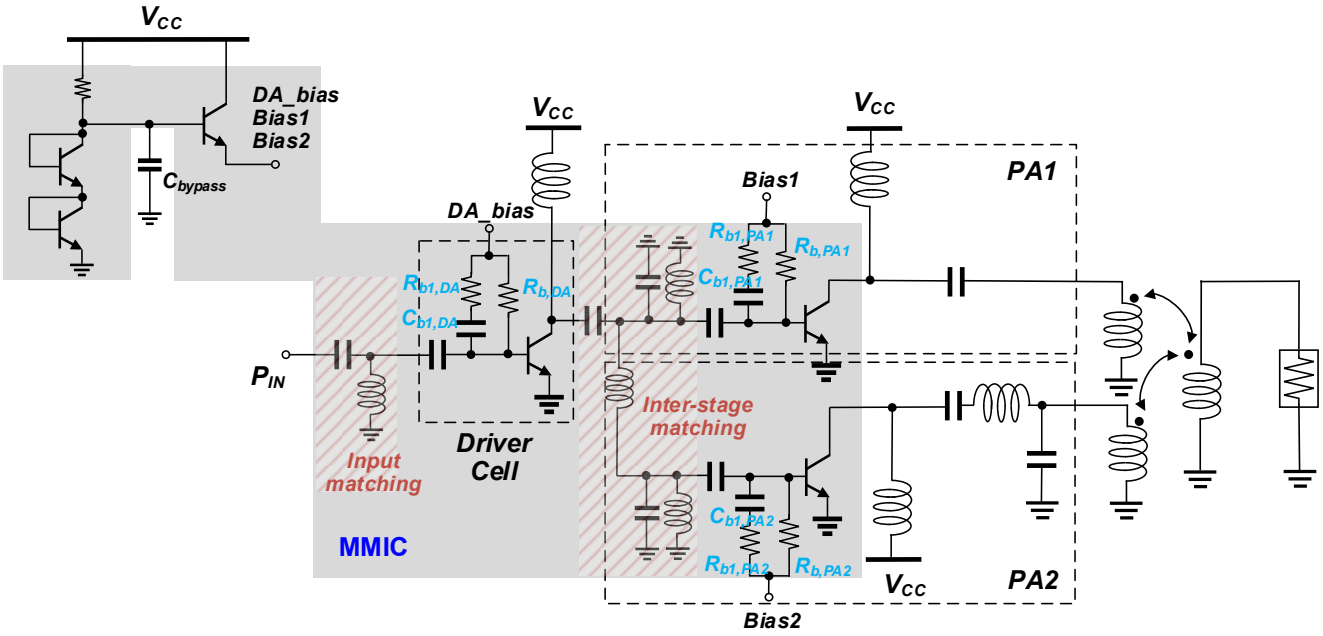


Figure 7. Schematic of the proposed HBT PA with a parallel power-combining transformer.

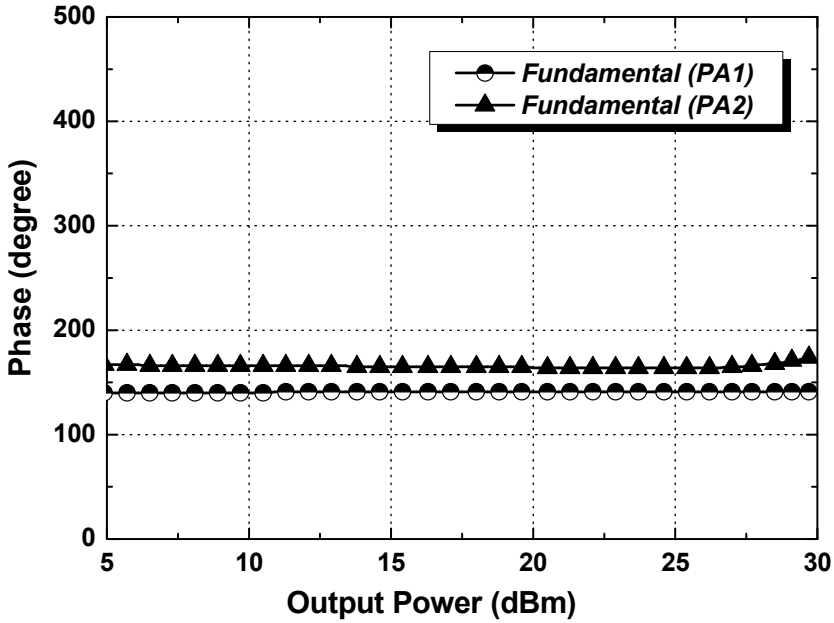


Figure 8. Two-tone simulated results for the phase of fundamental currents.

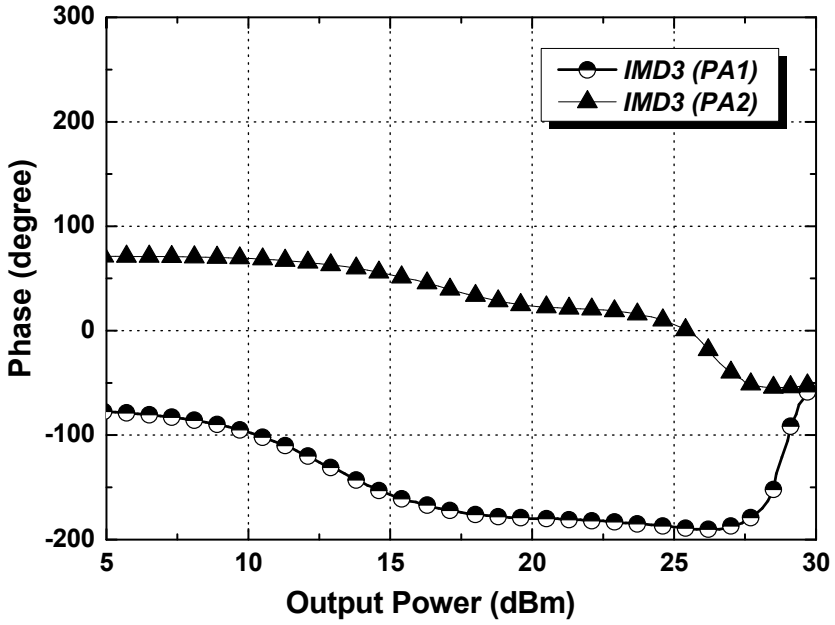


Figure 9. Two-tone simulated results for the phase of IMD3 currents.

The phase difference in IMD3 currents between PA1 and PA2 is in the range of $180° \pm 40°$ for an output power of up to 27.3 dBm. As shown in Figure 6, when the phase of the IMD3 currents from PA1 and PA2 is close to 180° out-of-phase, the IMD3 currents will cancel each other out at the output. Figure 10 shows the IMD3 comparison between the condition with IMD3 cancellation and that without the IMD3 cancellation under identical values of R_b, R_{b1}, and C_{b1}. For the case of the PA without the IMD3 cancellation, the condition of $R_{b,PA1} = R_{b,PA2}$, $R_{b1,PA1} = R_{b1,PA2}$, and $C_{b1,PA1} = C_{b1,PA2}$ is chosen. An IMD3 performance of −40 dBc can be maintained for an output power of up to 28.1 dBm by applying the IMD3 cancellation condition.

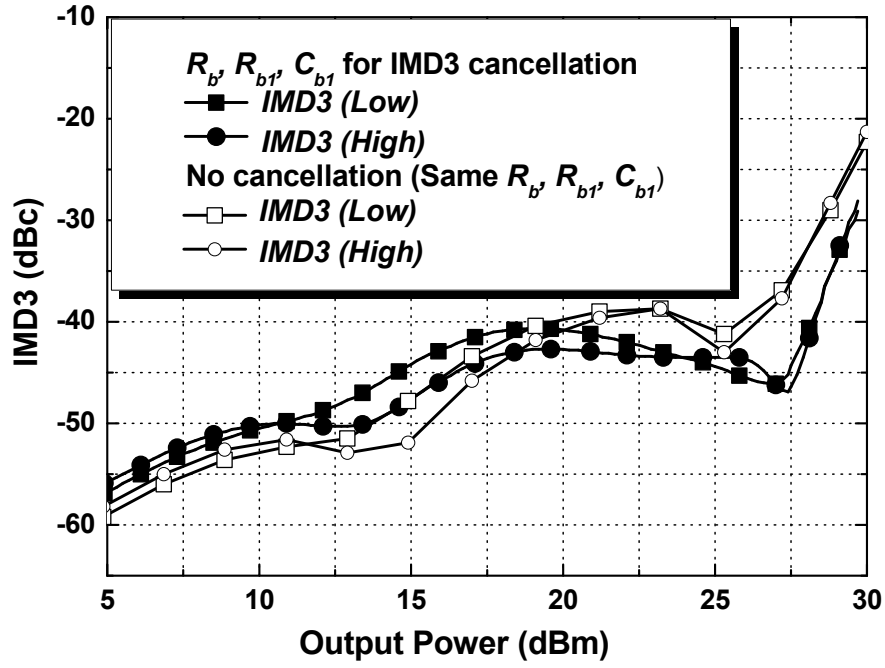


Figure 10. Simulated total IMD3 results with and without IMD3 cancellation.

4. Measurement Results

A two-stage dual-mode InGaP/GaAs HBT PA was constructed with fabricated DA/PA devices, including input/inter-stage matching [21] and the proposed PCT implemented using a PCB. Figure 11 shows a photograph of the PA designed with the PCT. The proposed PA was operated at a supply voltage of 5 V.

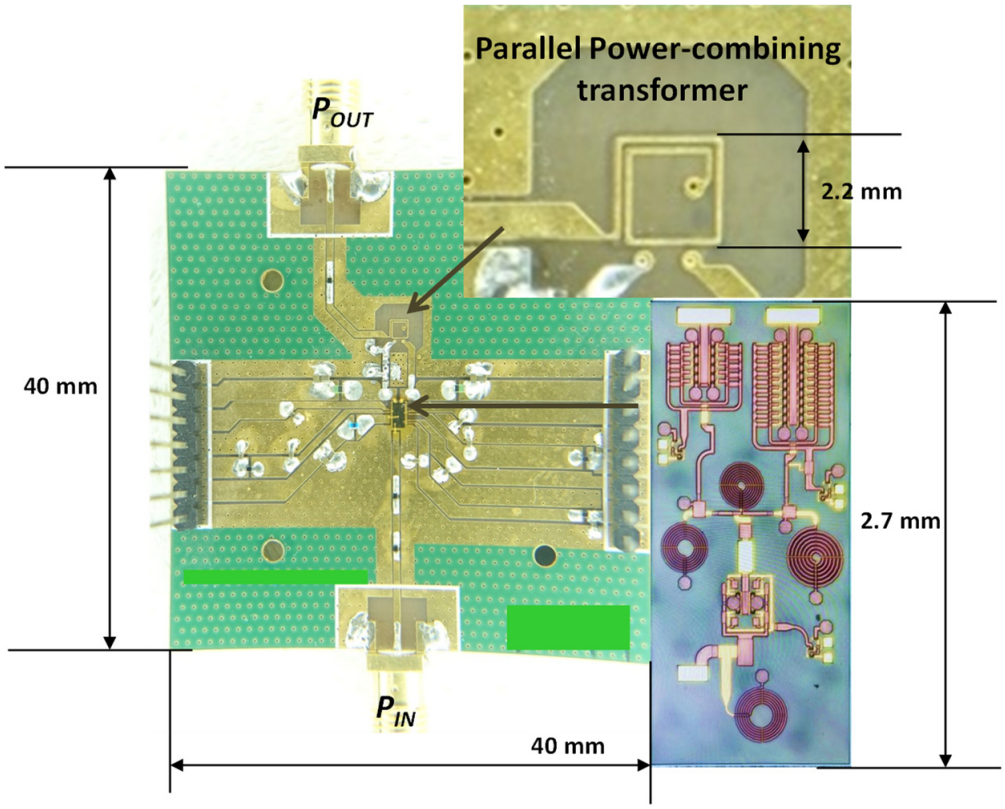


Figure 11. Photograph of the dual-mode HBT PA using PCB PCT.

The measured S-parameter results are shown in Figure 12. The implemented PA was tested with a 0.91 GHz single-tone continuous wave (CW). Figure 13 shows the measured power gains and power-added efficiencies (PAEs) of the dual-mode operation (HP and LP modes). Both PA1 and PA2 are turned on for the HP-mode operation. Meanwhile, for the LP mode operation, PA1 is turned on, whereas PA2 is turned off. The measured power gains of the implemented PA are 34.6 dB and 18.9 dB for the HP and LP modes, respectively. The saturated output powers, P_{SAT}, are 33.8 dBm and 22.5 dBm for the HP and LP modes, respectively. The P_{SAT} of the PA is over 2 W with the proposed high-Q parallel power-combining transformer. The peak PAEs for the HP and LP modes are 54.5% and 15.4%, respectively.

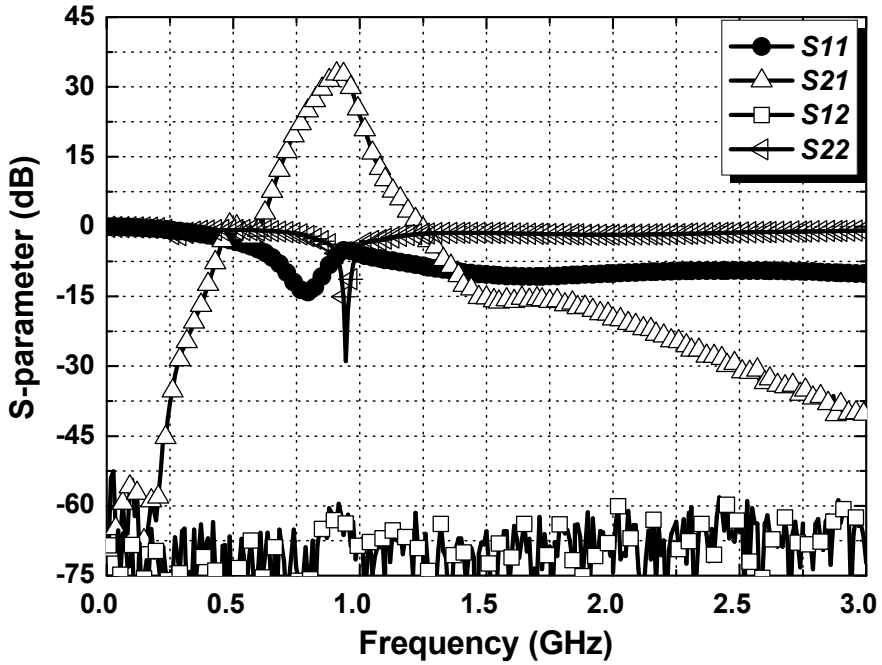


Figure 12. Measured S-parameter performances.

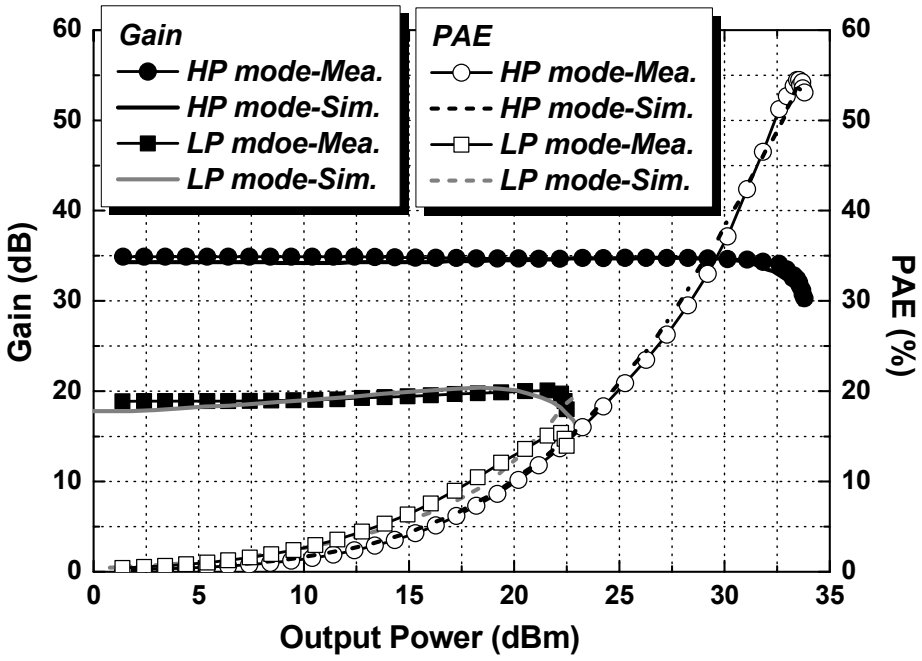


Figure 13. Measured 0.91 GHz continuous wave performance.

Additionally, the PA was also tested with a two-tone signal centered at 0.91 GHz with a tone spacing of 10 MHz. Figure 14 shows the measured IMD3 results versus the output power. The PA yields output powers of 27.5 dBm and 13.0 dBm in the HP and LP modes, respectively, while attaining IMD3 results of less than −35 dBc. As shown in Figure 9, owing to the mechanism of the IMD3 cancellation, the IMD3 results of less than −35 dBc are obtained up to an output power of 27.5 dBm in the HP mode.

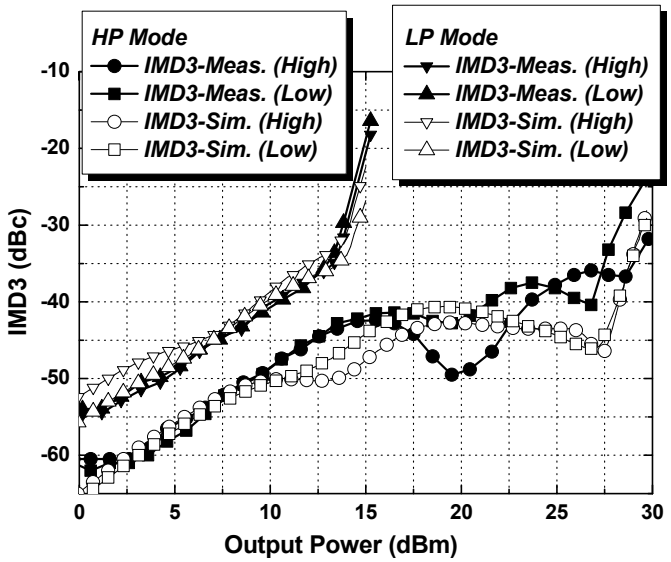


Figure 14. Measured IMD3 results.

A modulated signal measurement was performed with an orthogonal frequency division multiplexing (OFDM) 64-quadrature amplitude modulation (64-QAM) signal with a bandwidth of 10 MHz and a PAPR of 7.8 dB at 0.91 GHz. Figure 15 shows the measured adjacent channel leakage ratio (ACLR) and PAE versus the average output power. The PA achieves an average output power of 25.2 dBm with PAEs of 20.2%, while attaining ACLR results of less than −42 dBc. As shown in Figure 16, the operation in the LP mode can reduce the current consumption in the low output power range by 48% (i.e., by 68 mA) from that in the HP mode (143 mA), while attaining ACLR results of less than −42 dBc at an average output power of 10.4 dBm. Figure 17 shows the measured PA output spectrums in the HP and LP modes for the OFDM 64-QAM signal with a bandwidth of 10 MHz at 910 MHz. Without a digital pre-distortion (DPD) applied, the ACLR of the proposed PA is obtained at less than −42 dBc, up to 25.2 dBm and 10.4 dBm in the HP and LP modes, respectively.

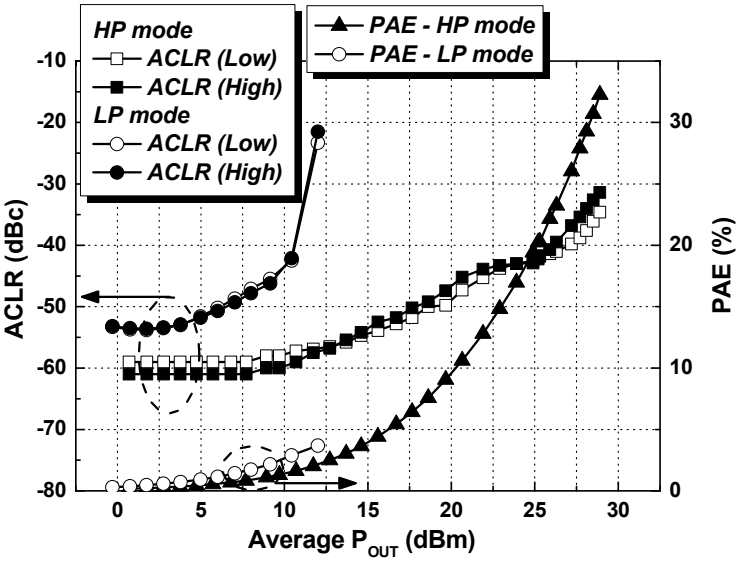


Figure 15. Measured ACLR and PAE for the 64-QAM OFDM signal with a bandwidth of 10 MHz at 0.91 GHz.

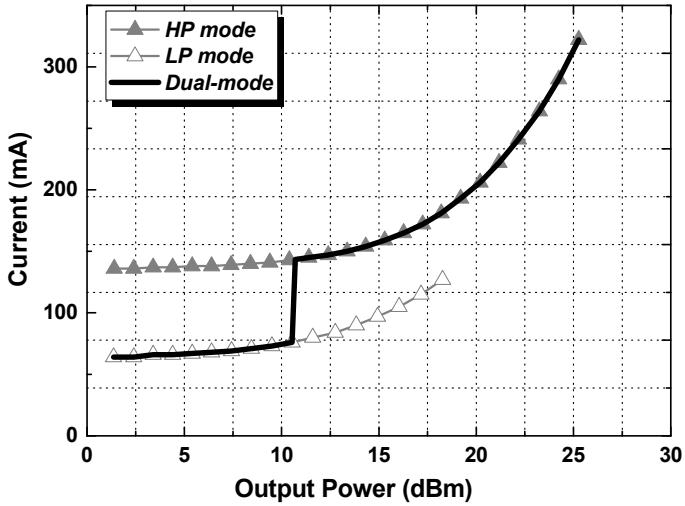
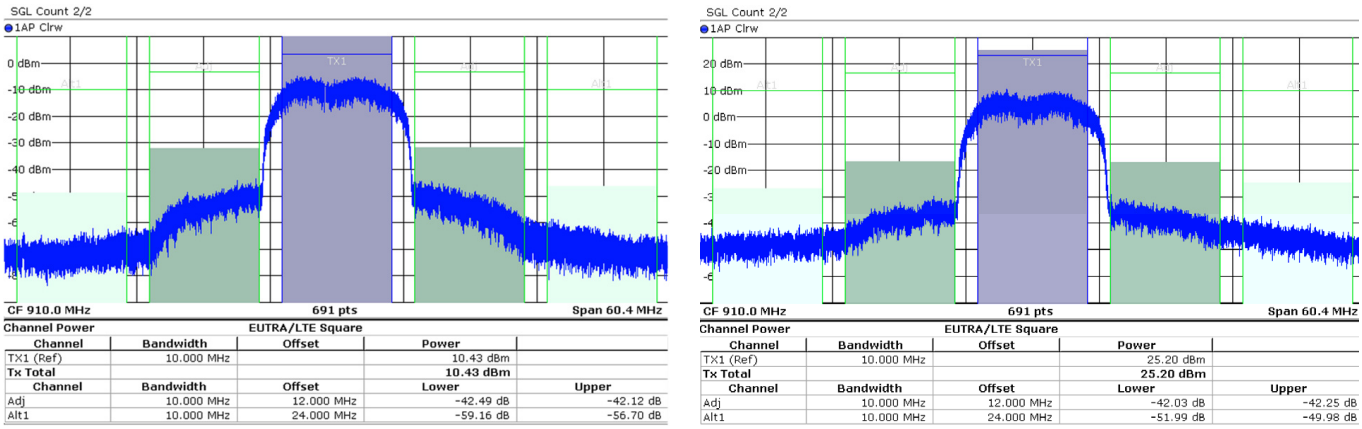


Figure 16. Measured current consumption for the 64-QAM OFDM signal with a bandwidth of 10 MHz at 0.91 GHz.



(**a**) (**b**)

Figure 17. Measured PA output spectrum for the OFDM 64-QAM signal with a bandwidth of 10 MHz at 0.91 GHz: (**a**) output power of 10.4 dBm in the LP mode, (**b**) output power of 25.2 dBm in HP mode.

Table 1 compares the PA developed in this work to the other PAs using other power-combining transformers on a PCB. A PCT can be implemented on a PCB with an area smaller than that of the SCT. Table 2 summarizes the HBT PAs for the femto-cell applications. Among the PAs in the comparison table, the proposed PA demonstrates a dual-mode operation to reduce the current consumption at a lower power level with a high-*Q* PCT configuration.

Table 1. Performance comparison of PAs with power-combining transformers on a PCB.

Ref.	Power-Combining Transformer (Size: mm^2)	Tech.	Freq. (GHz)	$P_{SAT.}$ (dBm)	Gain (dB)	Peak PAE (%)
[9]	SCT (5.1 mm × 2.4 mm)	CMOS	0.875	31.7	30.3	62
This work	Dual-mode PCT (2.2 mm × 2.2 mm)	HBT	0.91	33.8 (HP) 22.5 (LP)	34.6 (HP) 18.9(LP)	54.5 (HP) 15.4 (LP)

Table 2. Performance comparison with linear femto-cell HBT PAs.

	Output Features	Freq. (GHz)	$P_{SAT.}$ (dBm)	Gain (dB)	Peak PAE (%)	Signal	Pout (dBm) @ −42 dBc ACLR	PAE (Current) @ Pout
[22]	LC Matching	0.85	34.5 *	31.8 *	N/A	WCDMA 64DPCH	26.0 *	(540 mA) @ 25 dBm
[23]	LC Matching	0.9	N/A	31.7	N/A	10-MHz LTE TM1.1	19.8 *	14.0% * @ 19.8 dBm
[21]	Single- & Two-Winding Transformer	0.91	33.3	34.3	61.3	10-MHz 64QAM (7.8 dB PAPR)	26.0	26.8% (297 mA) @ 26.0 dBm
[14]	On-chip Transformer	2.3	31.0	26.0	27.6	10-MHz LTE (7.3 dB PAPR)	18.1 *	4.7% * @ 18.1 dBm
This work	Dual-Mode PCT	0.91	33.8 (HP) 22.5 (LP)	34.6 (HP) 18.9 (LP)	54.5 (HP) 15.4 (LP)	10-MHz 64QAM (7.8 dB PAPR)	25.2 (HP) 10.4 (LP)	20.1% (322 mA) @25.2 dBm (HP) 143 mA (HP)/75 mA (LP) @10.4 dBm

* graphically estimated

5. Conclusions

In this paper, an HBT PA with a high-*Q* parallel power-combining transformer to efficiently combine two individual amplifiers with a relatively compact area is proposed. In addition, dual-mode operation is adopted in the PA with the PCT configuration to reduce the current consumption. Furthermore, an IMD3 cancellation technique using the PCT combiner is presented to satisfy the stringent ACLR requirement for femto-cell base-station PAs. The implemented PA achieves a saturated output power, power gain, and peak PAE of 33.8 dBm, 34.6 dB, and 54.5%, respectively. Current consumption saving of 48% can be obtained with the LP mode operation at an output power of 10.4 dBm.

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