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High Power Density, High-Voltage Parallel Resonant Converter Using Parasitic Capacitance on the Secondary Side of a Transformer

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Abstract: High-voltage DC power supplies are used in several applications, including X-ray, plasma, electrostatic precipitator, and capacitor charging. However, such a high-voltage power supply has problems, such as a decrease in reliability, owing to an increase in output ripple voltage, and a decrease in power density, owing to an increase in volume. Therefore, this study proposes a method for improving the power density of a parallel resonant converter using the parasitic capacitor of the secondary side of the transformer. Due to the fact that high-voltage power supplies have many turns on the secondary side, a significant number of parasitic capacitors are generated. In addition, in the case of a parallel resonant converter, because the transformer and the primary resonant capacitor are connected in parallel, the parasitic capacitor component generated on the secondary side of the transformer can be equalized and used. A parallel cap-less resonant converter structure developed using the parasitic components of such transformers is proposed. Primary side and secondary side equivalent model analyses are conducted in order to derive new equations and gain waveforms. Finally, the validity of the proposed structure is verified experimentally.

Keywords: cap-less parallel resonant converter; high power density; high-voltage power supply; parasitic capacitance; equivalent model analysis



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1. Introduction

High-voltage DC power supplies are used in several applications, including X-ray generators, plasma generators, electrostatic precipitators, and capacitor charging. However, such a high-voltage power supply has problems, such as a decrease in reliability owing to an increase in output ripple voltage and a decrease in power density owing to an increase in volume. Consequently, several studies have been conducted in order to reduce the output voltage ripple or improve the power density and to ensure the miniaturization, high efficiency, and reliability of high-voltage DC power supplies [1–7].

In high-voltage DC power supplies, soft-switching-based resonant converter topologies, such as a series resonant converter, parallel resonant converter, and LCC resonant converter, are mainly used to increase system efficiency. However, owing to the characteristics of the high-voltage output, a high rated voltage and a large current are induced in the resonant network on the primary side of the topology. Accordingly, a resonant capacitor comprising the resonant network also requires a high rated voltage and a large current. The resonant capacitor is applied as a bank, comprising several capacitors connected in series or parallel, in order to satisfy these required characteristics. This configuration of the resonant capacitor bank is a major cause of the deterioration of the power density of the resonant converter in a high-voltage DC power supply. In addition, in a high-voltage DC power supply, increasing the output voltage is an important factor. Therefore, in many current high-voltage DC power supply applications, voltage multiplier circuits are frequently used to increase the output voltage itself. However, in the case of the voltage multiplier circuit,

the number of diodes and capacitors increases as the output voltage increases; therefore, the power density of the entire system decreases [2].

Several studies have been conducted in order to increase the switching frequency and power density of the system. However, if the switching frequency is increased, the efficiency of the system generally decreases, owing to the high switching loss, and the heat dissipation design becomes difficult. In [7,8], the authors proposed methods to reduce the size of passive components, such as resonant inductors, transformers, and capacitors, by increasing the switching frequency through applying wide-bandgap (WBG) switching components. In this case, the switching loss did not increase significantly, owing to the fast-switching characteristics of the WBG switching element. However, applying such an element to an actual system is not favorable because it leads to an increase in the price of the switching device used in the system.

To increase the power density of the system, some studies [9,10] proposed a method that uses the leakage inductance of a transformer as a resonant inductor. In [10,11], the power density was improved by applying a planar transformer. However, it is difficult to implement a large number of windings when the frequency increases, owing to the structure of a planar transformer that forms windings using a PCB pattern. Consequently, it is difficult to apply a high-voltage DC power supply that requires several turns on the secondary side of the transformer.

Applying a conventional device, such as using the planar transformer and WBG switching components, to a high-voltage DC power supply is difficult because the transformer turns are limited and the cost increases. This paper proposes a method for improving the power density of a parallel resonant converter by employing the secondary side parasitic capacitor of the transformer without using a resonant capacitor on the primary side. Due to the fact that high-voltage power supplies have many turns on the secondary side, a significant number of parasitic capacitors are generated. In addition, in the case of a parallel resonant converter, because the transformer and the primary resonant capacitor are connected in parallel, the parasitic capacitor component generated on the secondary side of the transformer can be used. Primary side and secondary side equivalent model analyses are performed in order to derive new equations and gain waveforms. Finally, the validity of the proposed structure is verified experimentally.

2. Proposed Parallel Resonant Converter

2.1. Structure of the Proposed Parallel Resonant Converter

Figure 1a shows the structure of a conventional parallel resonant converter applied with a voltage multiplier circuit on the secondary side, and Figure 1b shows the structure of a parallel resonant converter in which the primary resonant capacitor is equalized to the secondary side of the transformer. The conventional parallel resonant converter shown in Figure 1a is composed of switching components S_1 – S_4 , a resonant inductor L_r , a magnetizing inductance L_m existing in the transformer primary side, a resonant capacitor C_r , a high-frequency transformer T_r , capacitors C_1 – C_{4n} and rectifier diodes D_1 – D_{4n} forming the secondary side voltage multiplier circuit, and a load R_o . However, after considering the rated voltage and current that flows in the resonant inductor, the resonant capacitor is configured in series or parallel, which increases the size of the system. Consequently, a resonant capacitor on the primary side is not used in the proposed converter (Figure 1b), and a resonant circuit can be constructed through the secondary side parasitic capacitance of a high-frequency transformer. Thus, it is possible to improve the power density compared to that of the conventional structure.

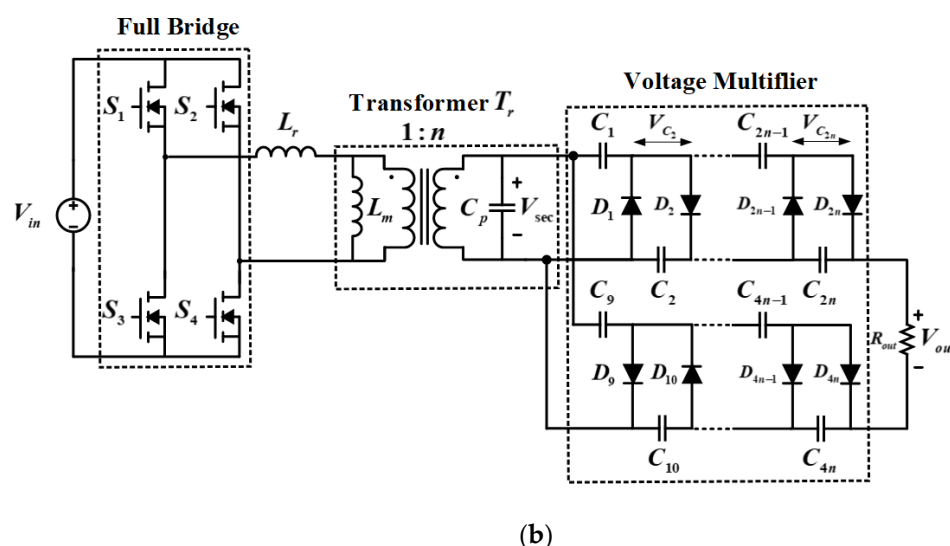
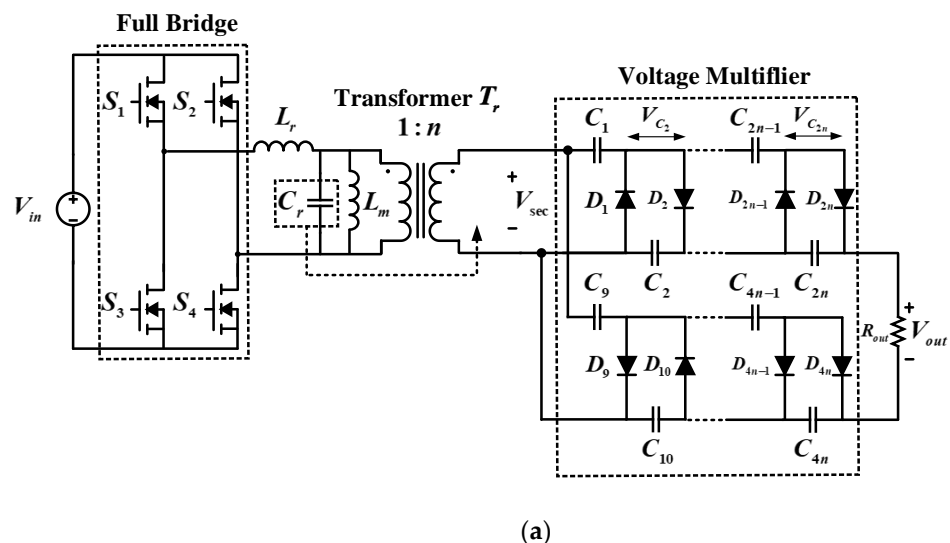


Figure 1. System structure of the parallel resonant converter applied with a voltage multiplier: (a) conventional system structure; (b) proposed system structure.

In the proposed structure, if the high-voltage DC output characteristic is used, the secondary side has a significant amount of parasitic capacitance compared to the primary side of the transformer, owing to the higher number of turns on the secondary side. Consequently, in contrast to the conventional parallel resonant converter, the proposed parallel resonant converter uses a resonant capacitor to replace the parasitic capacitance generated in the transformer. In Equation (1), the resonant capacitor C_r on the primary side is equalized to the secondary side by considering the ratio of the number of turns of the transformer. In the proposed parallel resonant converter, the resonant capacitance is $n^2 \cdot C_p$ instead of C_r [12,13]. Consequently, the resonant inductor L_r and the secondary side parasitic capacitor C_p of the transformer resonate, and the resonant frequency can be expressed using Equation (2). In addition, when the secondary side parallel structure is used, the upper voltage multiplier circuit produces a voltage of +50 kV and the lower voltage multiplier circuit produces a voltage of -50 kV, resulting in an output voltage of 100 kV.

$$C_r = n^2 \cdot C_p \tag{1}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r \cdot n^2 C_p}} \tag{2}$$

2.2. Operating Principle

Figures 2 and 3 show the operating principle and key waveforms of the proposed parallel resonant converter, respectively. For an analysis of the operation of the converter, the parasitic components generated at the primary side of the transformer and the components generated at the capacitor of the voltage multiplier circuit stage are not considered.

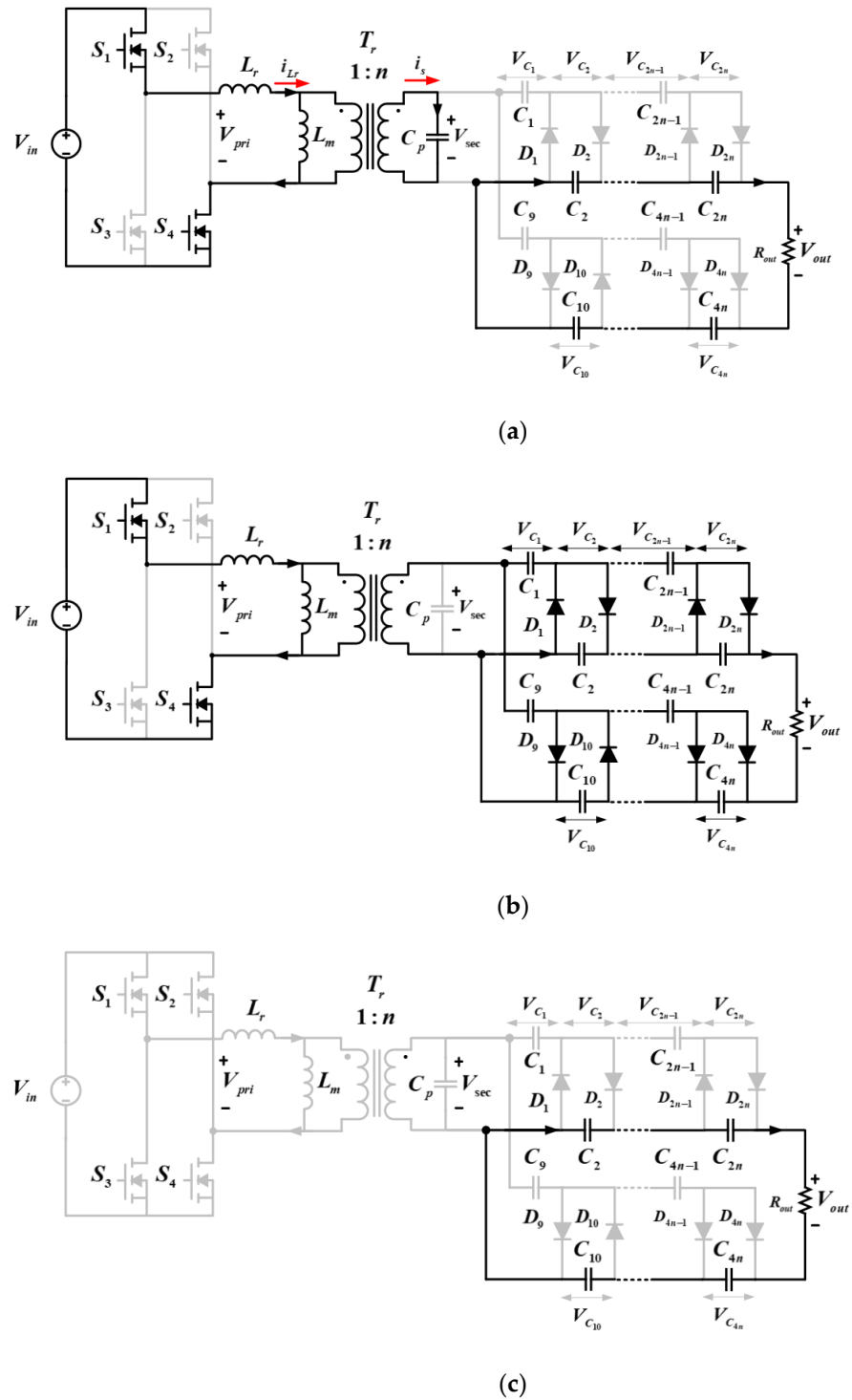


Figure 2. Cont.

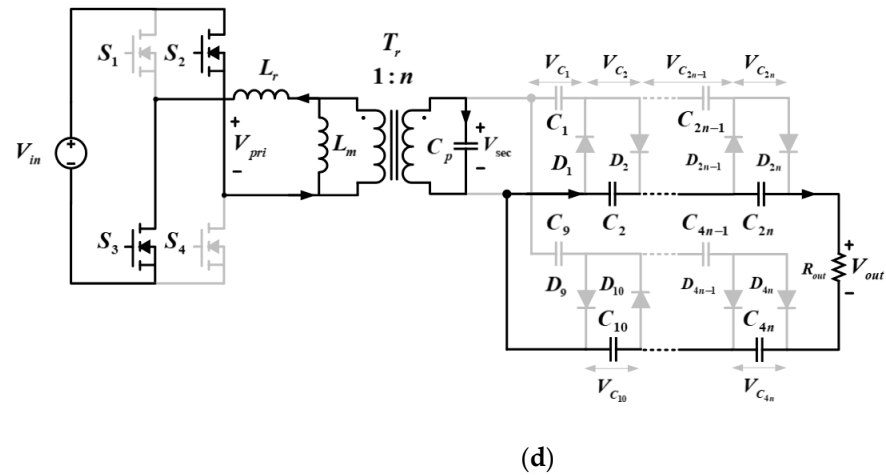


Figure 2. Operation mode of the proposed parallel resonant converter: (a) MODE 1 $[t_0 - t_1]$; (b) MODE 2 $[t_1 - t_2]$; (c) MODE 3 $[t_2 - t_3]$; (d) MODE 4 $[t_3 - t_4]$.

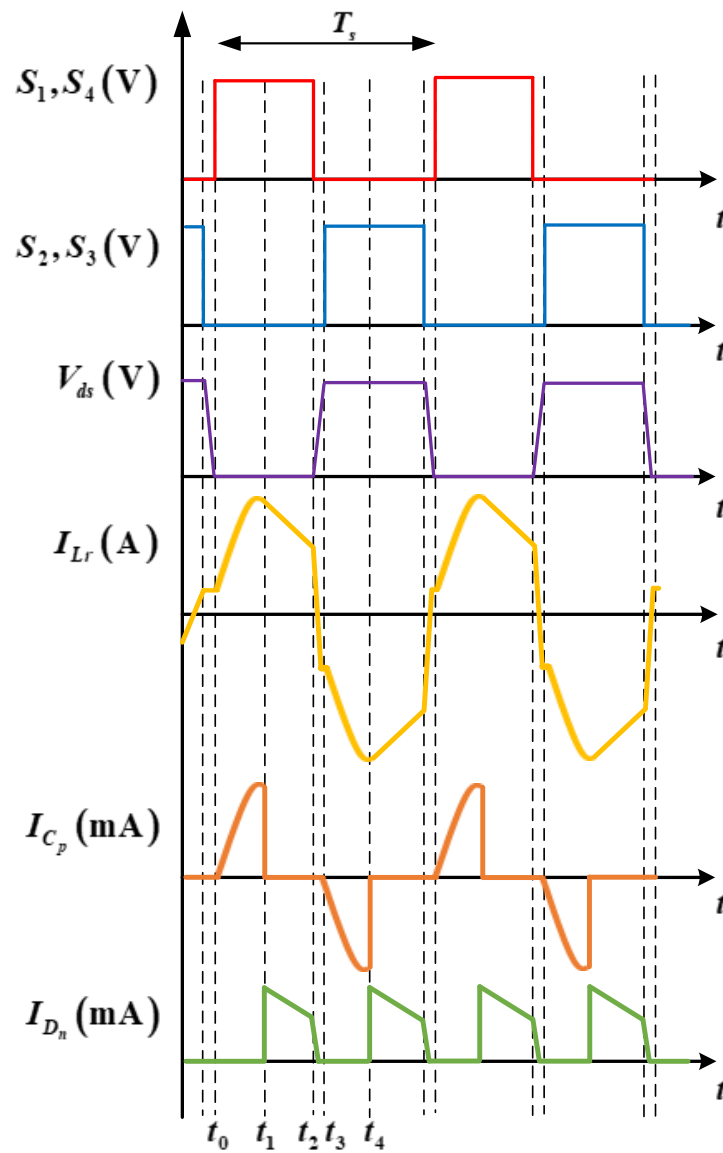


Figure 3. Key waveforms of the proposed parallel resonant converter.

MODE 1 [$t_0 - t_1$]: this mode starts when S_1 and S_4 are conducting. During this period, the primary side resonant current I_{Lr} flows in the positive direction and flows through the transformer to the secondary side parasitic capacitor C_p . In this operation period, because the capacitor voltage V_{C1} at the voltage multiplier circuit is greater than the voltage on the secondary side of the transformer V_{sec} , diode D_1 becomes reverse biased so that all currents flowing in the secondary side flow toward the secondary side parasitic capacitor C_p . Consequently, the rectifier diodes $D_1 - D_{4n}$ at the voltage multiplier circuit do not conduct, and the resonant inductor L_r at the primary side and C_p at the secondary side participate in resonance. In addition, the current path is formed by the voltage charged in the capacitor at the voltage multiplier. This mode ends as soon as the voltage across the secondary side parasitic capacitor becomes greater than the capacitor voltage V_{C1} at the voltage multiplier circuit.

MODE 2 [$t_1 - t_2$]: in mode 2, S_1 and S_4 are still conducting, and this mode starts when V_{sec} becomes higher than V_{C1} at the voltage multiplier circuit. At this time, the current flows to diodes $D_1 - D_{4n}$ and becomes forward biased, making the diodes at the upper and lower voltage multiplier conduct. Consequently, no current flows to the secondary side C_p , and the transformer voltage V_{sec} is clamped at V_{out} . In addition, because the output voltage is clamped at C_p , the primary side magnetizing inductor L_m connected in parallel assumes a voltage. This results in the resonant inductor L_r , the secondary-side C_p , and the primary side magnetizing inductor L_m not participating in resonance, and the primary side resonant current I_{Lr} being linearly decreased. This mode ends when the switching components S_1 and S_4 are turned OFF.

$$V_{pri} = L_m \frac{di_m}{dt} \quad (3)$$

MODE 3 [$t_2 - t_3$]: this mode represents a dead time period and starts when $S_1 - S_4$ are turned OFF. Consequently, power is not transferred from the primary side to the secondary side. In addition, $S_1 - S_4$ do not conduct; thus, I_{Lr} and the rectifier diode current I_D decrease significantly. This mode ends when S_2 and S_3 conduct.

MODE 4 [$t_3 - t_4$]: after the switching half cycle is complete at t_3 , a new half cycle starts when S_2 and S_3 conduct.

3. Analysis of Equivalent Circuit of the Proposed Parallel Resonant Converter

The fundamental harmonic approximation (FHA) is used to analyze the primary and secondary sides of the proposed parallel resonant converter and to obtain the voltage gain [14]. For the analysis, only the first-order harmonic component of the square wave of the input voltage is considered; thus, it is easy to analyze the proposed parallel resonant converter. In addition, the structure of the proposed parallel resonant converter comprises a parallel voltage multiplier at the secondary side and produces a total output voltage of 100 kV. However, in this study, only one voltage multiplier stage producing a 50 kV output voltage is considered.

Equation (4) considers several harmonic components of the primary side voltage. In Equation (5), the equation used for FHA, only the first-order harmonic component is considered; that is, other harmonic orders are not considered. Thus, Equation (5) is used to calculate the voltage gain of the proposed converter.

$$V_{pri} = \frac{4V_{in}}{\pi} \sum_{n_1=1,3,5,\dots} \frac{1}{n_1} \sin(n_1\omega t) \quad (4)$$

$$V_{pri}^F = \frac{4V_{in}}{\pi} \sin(\omega t) \quad (5)$$

Figure 4 shows the circuit for deriving the equivalent load resistance value. The component on the primary side is replaced by a sinusoidal current source, and the input voltage on the secondary side is expressed as a square wave component. In addition, the

average value of the sinusoidal current is the output current, expressed by Equation (6). Equation (7) represents the voltage across the secondary transformer. In the voltage multiplier circuit, this voltage is 1/8 times that of the output voltage. In addition, by dividing Equation (9) by the current component Equation (6), the equivalent load resistance Equation (10) can be obtained.

$$I_{ac} = \frac{\pi \cdot I_{out}}{2} \sin(\omega t) \tag{6}$$

$$V_{sec} = +\frac{1}{8}V_{out} \text{ if } \sin(\omega t) > 0 \quad V_{sec} = -\frac{1}{8}V_{out} \text{ if } \sin(\omega t) < 0 \tag{7}$$

$$V_{sec} = \frac{4V_{out}}{\pi} \sum_{n_1=1,3,5\dots} \frac{1}{n_1} \sin(n_1\omega t) \tag{8}$$

$$V_{sec}^F = \frac{4V_{out}}{\pi} \sin(\omega t) \tag{9}$$

$$R_{ac} = \frac{V_{sec}^F}{I_{ac}} = \frac{8}{\pi^2} \frac{V_{out}}{I_{out}} = \frac{8}{\pi^2} R_o \tag{10}$$

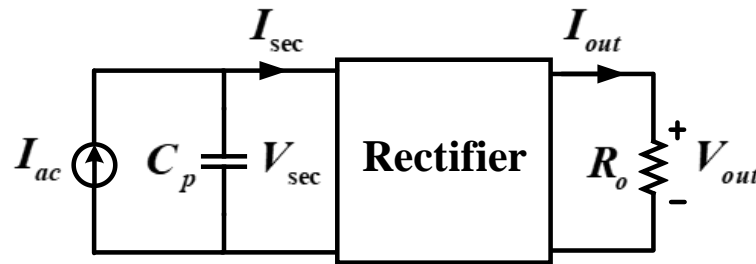


Figure 4. Circuit diagram to derive the equivalent load resistance.

In high-voltage applications, the secondary side of the transformer has a higher turn ratio than the primary side. If the turn ratio is equalized to the primary side, the equivalent load resistance can be expressed by Equation (11). Therefore, the equivalent resistance equation can be derived, and the voltage gain of the converter can be obtained through the Equations (5) and (9). When the secondary side voltage V_{sec} is equalized to the primary side, we obtain the voltage gain Equation (12). When the primary side and secondary side voltages are calculated, the voltage gain can be expressed as Equation (13).

$$R_{ac} = \frac{8}{n^2 \cdot \pi^2} R_o \tag{11}$$

$$M = \frac{\frac{1}{n} \cdot V_{sec}^F}{V_{pri}^F} \tag{12}$$

$$M = \frac{\frac{4V_{out}}{n\pi} \sin(\omega t)}{\frac{4V_{in}}{\pi} \sin(\omega t)} = \frac{1}{n} \frac{V_{out}}{V_{in}} \tag{13}$$

Figure 5 shows the AC equivalent circuit of the proposed parallel resonant converter. In order to derive the necessary equation for the parallel resonant converter, it is necessary to calculate the characteristic impedance Z_o using the resonant inductor L_r , magnetizing inductance L_m , equivalent resistance R_{ac} , and the equivalent resonant capacitance $n^2 \cdot C_p$. These resonance tank components can be expressed as follows.

$$M = \frac{(L_m || n^2 \cdot C_p || R_{ac})}{L_r + (L_m || n^2 \cdot C_p || R_{ac})} \tag{14}$$

$$Z_o(s) = \left(sL_r \parallel \frac{1}{sn^2 \cdot C_p} \parallel R_{ac} \right) \tag{15}$$

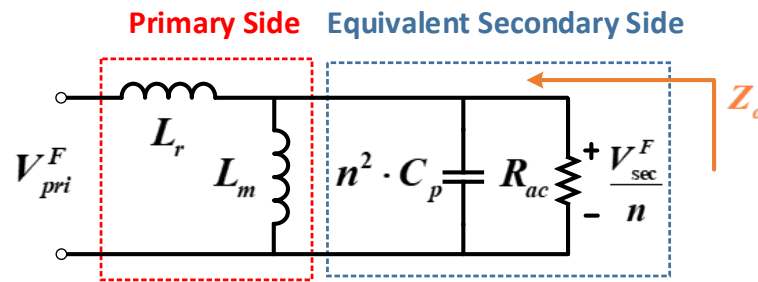


Figure 5. AC equivalent circuit of the proposed parallel resonant converter.

In the case of a parallel resonant converter, the impedance of the inductor, which can be expressed as $|Z_o(s)| \cong \omega L_r$, is more dominant at a low frequency, whereas the impedance of the capacitor component, which can be expressed as $|Z_o(s)| \cong \frac{1}{\omega n^2 C_p}$, is more dominant at a high frequency. In addition, the resonant inductance and resonant capacitance are canceled at the resonant frequency, as shown in Equation (16). The resonant inductor and resonant capacitor values of the proposed parallel resonant converter can be derived from Equations (17)–(19).

Figure 6 shows the voltage gain curve for an output voltage of 50 kV. This curve is obtained using the equivalent circuit shown in Figure 5 and the calculated Equations (14) and (17)–(19).

$$||Z_o(s)||_{s=j\omega_s} = \frac{1}{\frac{1}{j\omega_o L_r} + j\omega_o \cdot n^2 \cdot C_p + R_{ac}} = R_{ac} \tag{16}$$

$$\omega_o L_r = \frac{1}{\omega_o \cdot n^2 \cdot C_p} = Z_o \tag{17}$$

$$L_r = \frac{Z_o}{\omega_o} \tag{18}$$

$$C_p = \frac{1}{\omega_o \cdot n^2 \cdot Z_o} \tag{19}$$

$$\omega_o L_r = \frac{1}{\omega_o \cdot n^2 \cdot C_p} = Z_o \tag{20}$$

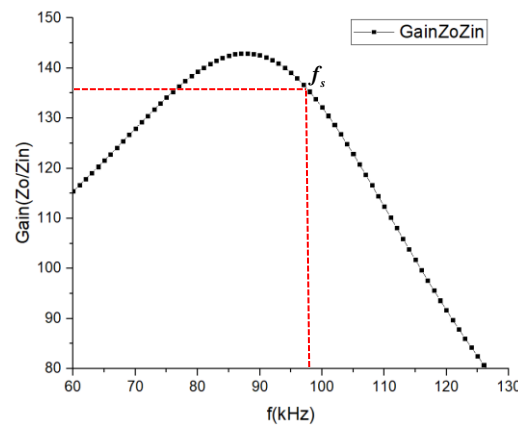


Figure 6. Gain curve of the proposed parallel resonant converter.

4. Analysis of the Secondary Side Voltage Multiplier

In high-output-voltage applications, a voltage multiplier circuit is used to obtain a much higher output voltage by using a rectifier diode and a capacitor [15–19]. For example, in the case of a parallel resonant converter used in high-output-voltage applications such as medical devices, because the output voltage is greater than 5 kV, voltage multiplier circuits are mostly used at the rectifier stage of the converter. Consequently, in this study, four stages and a parallel-structure voltage multiplier are used to obtain an output voltage greater than 100 kV.

The voltage at the secondary side transformer V_{sec} is required in order to increase the output voltage V_o . Based on the resonant inductor L_r on the primary side and the parasitic capacitor C_p on the secondary side, as shown in Figure 1, the voltage applied to the secondary side of the transformer V_{sec} has a pulse waveform with a peak value of 6.25 kV. In addition, this voltage is applied to the capacitor at the voltage multiplier circuit C_1 when the rectifier diode is turned ON. With this principle, the voltage V_{C_2} of 12.5 kV is applied, and $V_{C_{2n}}$, the current from the four-stage voltage multiplier circuit, is obtained as 50 kV. With this principle, the proposed parallel resonant converter can obtain a final output voltage of 100 kV, with a voltage ranging from -50 kV to 50 kV, using upper and lower voltage multiplier circuits. The pulsed voltage waveforms can be expressed as shown in Figure 7.

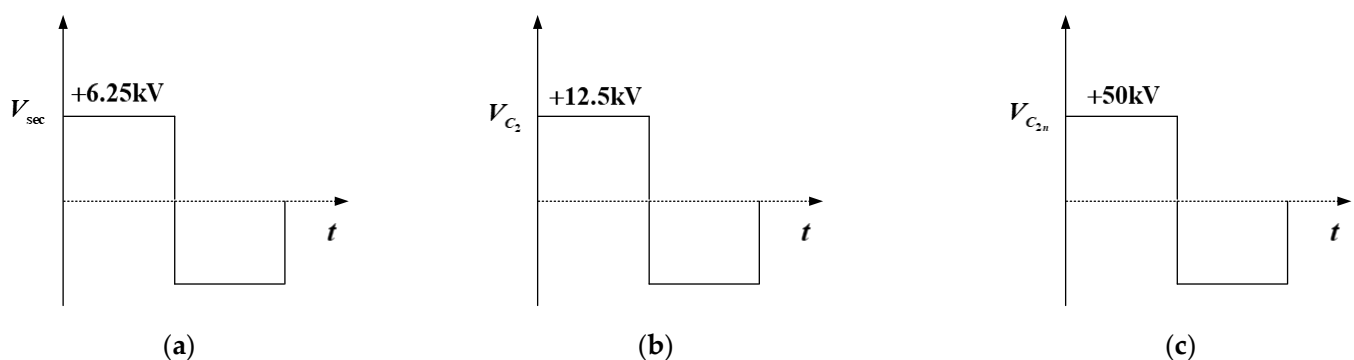


Figure 7. (a) Voltage at the secondary side of the transformer. (b) Voltage after 1st voltage multiplier. (c) Voltage after 4th voltage multiplier.

5. Experimental Results

Experiments are conducted to verify the effectiveness of the proposed parallel resonant converter. The operating conditions for the experiment are listed in Table 1. Figure 8 shows the experimental setup of the parallel resonant converter comprising the AC–DC stage, controller, DC–DC primary side, and DC–DC secondary side. It receives an input voltage of 220 V from the AC–DC terminal and converts it to a DC voltage of 380 V, and the converted value, using the transformer and voltage multiplier circuits on the secondary side of the DC–DC converter, finally results in an output voltage of 100 kV, as shown in Figure 8. In addition, in the experimental setup, the transformer stage and voltage multiplier circuits are separated from the primary side for high-voltage insulation using insulating oil. In addition, a constant current electronic load was applied and operated in a constant current mode.

Table 1. System parameters.

Symbol	Quantity	Value (Unit)
V_{in}	Input voltage	385 (V)
V_{out}	Rated output voltage	100 (kV)
P_{out}	Rated output power	1.7 (kW)
I_{out}	Output current	1.7 (mA)
L_r	Resonant inductor	106 (μ H)
L_m	Magnetizing inductance	1000 (μ H)
C_p	Parasitic capacitance	0.134 (nF)
$n_1 : n_2$	Turns ratio	1:12
f_s	Switching frequency	98 (kHz)

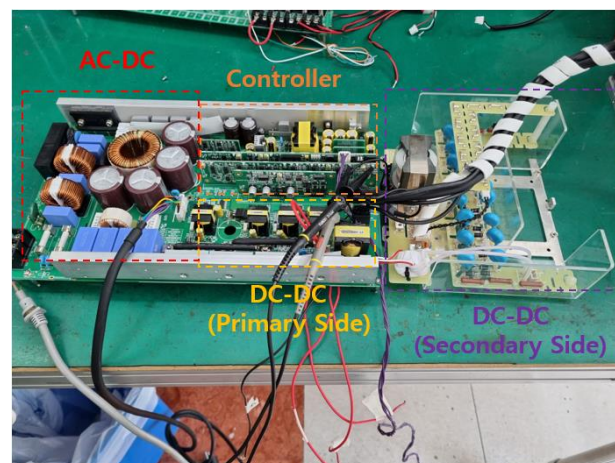
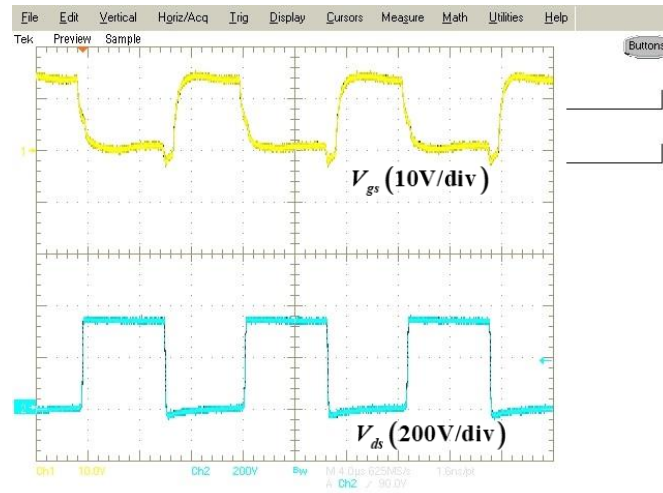
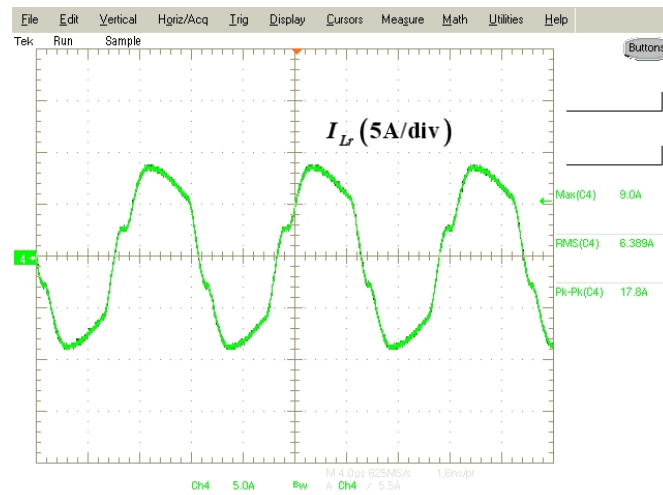
**Figure 8.** Experimental setup for the proposed parallel resonant converter system.

Figure 9 shows the experimental results of the proposed parallel resonant converter. Figure 9a shows the input gate voltage V_{gs} of the switching components and voltage V_{ds} across the switch component. The drain–source voltage is zero because switching components S_1 and S_4 are conducting. In addition, the input voltage V_{in} is applied to the voltage V_{ds} when S_1 and S_4 are not conducting. Figure 9b shows the primary side resonant inductor current I_{Lr} under the rated load condition. Therefore, the proposed parallel resonant converter has 1.7 kW output power, with an output voltage of 100 kV and an output current of 1.7 mA. In addition, a comparison with the key waveforms analyzed (Section 2) reveals that the experimental waveforms of the proposed converter are similar to the analyzed waveform, as a resonance between the resonant inductor and the parasitic capacitance occurs in $t_0 - t_1$. Figure 9c shows the primary side resonant inductor current I_{Lr} at a 50% load. In this case, the current flowing to the secondary side decreases because the output current is less than that of the rated load condition. Under these conditions, the proposed converter operates effectively at a 50% load; however, the primary side resonant current waveform becomes relatively small, owing to the difference in the output current.

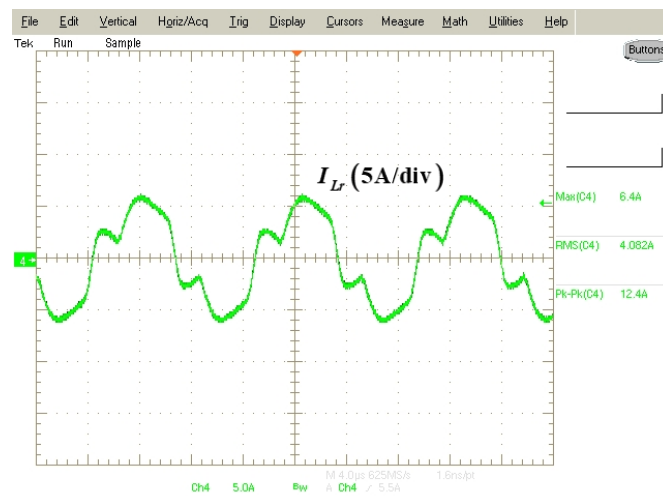
Figure 10 shows the feedback-sensing waveforms of the output voltage and output current at the rated output voltage. Using these voltage waveforms, it is confirmed that the proposed parallel resonant converter has a rated output voltage of 100 kV and an output current of 17 mA. In addition, in high-voltage applications, especially in medical X-rays, because the machines operate for a short time, a constant current load is usually used. Consequently, the sensed output voltage and output current waveforms are different.



(a)



(b)



(c)

Figure 9. Experimental test waveforms; (a) gate input voltage V_{gs} and switching drain–source voltage V_{ds} ; (b) resonant inductor current I_{Lr} at full-load condition; (c) resonant inductor current I_{Lr} at half-load condition.

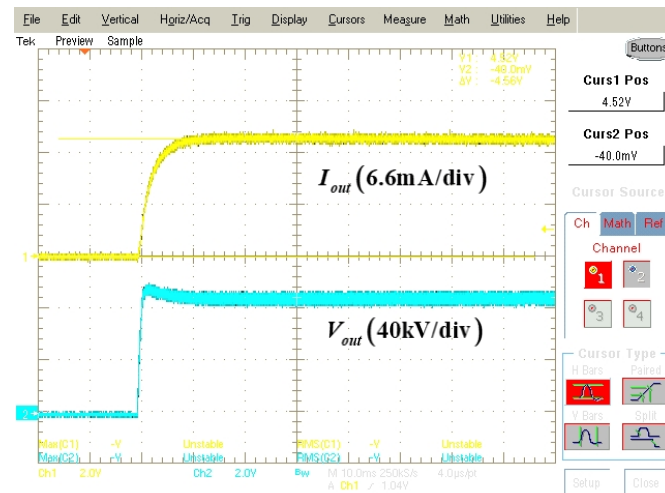


Figure 10. Feedback voltage for predicting the output voltage and output current.

6. Conclusions

In this paper, a novel parallel resonant converter structure using parasitic capacitor components on the secondary side of the transformer is proposed. The proposed parallel resonant converter uses the parasitic capacitance of the secondary side transformer instead of using the resonant capacitor on the primary side, which can secure the space on the primary side and so the power density of the parallel resonant converter can be improved. The effectiveness of the proposed structure is confirmed through the analysis of the equivalent model, derivation of new equations, and analysis of the voltage multiplier circuits. In addition, the operation of the proposed parallel resonant converter is verified through an experiment in which the system has an output power, voltage, and current of 1.7 kW, 100 kV, and 1.7 mA, respectively.

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