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A 33 MHz Fast-Locking PLL with Programmable VCO and Automatic Band Selection for Clock Generator Application

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Abstract: This paper presents a prototype of an auto-ranging phase-locked loop (PLL) with low jitter noise over a wide operating frequency range using the multiband programmable voltage-controlled oscillator (VCO) gain stage with automatic band selection. We successfully reduce the VCO gain (Kvco) and retain the desired frequency band. The proposed PLL comprises a prescaler, phase frequency detector (PFD), charge pump (CP), programmable VCO and automatic band selection circuit. The PLL prototype with all subblocks was implemented using the TSMC 0.18 µm 1P6M process. Contrary to conventional PLL architectures, the proposed architecture incorporates a real-time check and automatic band selection circuit in the secondary loop. A high-performance dual-loop PLL wide tuning range was realized using an ASIC digital control circuit. A suitable way to maintain the Kvco low is to use multiple discrete frequency bands to accommodate the required frequency range. To maintain a low Kvco and fast locking, the automatic frequency band selection circuit also has two indigenous, most probable voltage levels. The proposed architecture provides the flexibility of not only band hopping but also band twisting to obtain an optimized Kvco for the desired output range, with the minimum jitter and spurs. The proposed programmable VCO was designed using a voltage-to-current-converter circuit and current DAC followed by a four-stage differential ring oscillator with a cross-coupled pair. The VCO frequency output range is 150–400 MHz, while the input frequency is 25 MHz. A sequential phase detection loop with a negligible dead zone was designed to adjust fine phase errors between the reference and feedback clocks. All circuit blocks of the proposed PLL were simulated using the EDA tool HSPICE and layout generation by Laker. The simulation and measured results of the proposed PLL show high linearity, with a dead zone of less than 10 pV. The differential VCO was used to improve the linearity and phase noise of the PLL. The chip measured results show rms jitter of 19.10 ps. The PLL prototype also has an additional safety feature of a power down mode. The automatic band selection PLL has good immunity for possible frequency drifting due to temperature, process and supply voltage variations. The proposed PLL is designed for −40 to +85 °C, a wide temperature range.

Keywords: phase-locked loop (PLL); voltage-controlled oscillator (VCO); digital-to-analog converter (DAC); fast locking; jitter; phase detector; frequency synthesizer

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1. Introduction

Phase-locked loops (PLLs) are the integral building blocks of microprocessor, microcontroller and many wireless communication systems to generate a high-frequency and accurate clock signal from a reference frequency signal. Nowadays, the exponential growth in mobile communication devices also drives the demand for low-power integrated precise frequency synthesizers [1–4].

A classical PLL uses a single large frequency band for a large locking range, and it has a large voltage-controlled oscillator (VCO) gain. As a result, large jitter noise and dependency

on process, voltage and temperature (PVT) variation are observed in VCOs Refs. [5–9]. Hence, small Kvco is desirable to reduce the VCO jitter noise and PVT variation, but a small Kvco causes the tuning range to be narrower Refs. [10–14]. Using both continuous and discrete frequency bands in the form of many overlapping sub-bands can maintain the desired frequency range with a low VCO gain [15,16].

The proposed architecture uses equally spaced, sufficiently overlapped discrete VCO sub-bands to overcome these issues and to obtain a wide frequency tuning range for the desired locking frequency. In this way, the tuning range is increased and VCO jitter noise is suppressed due to the small Kvco gain. Supply voltage scaling also renders the proposed architecture more attractive and vital. To select the required frequency band among multiband effectively, an automatic band selection circuit block is also proposed. The automatic band selection feature is also useful when the PLL acknowledges a change in the divider ratio. The VCO circuit of multiple overlapped discrete bands produces low jitter noise at a variable power supply. The self-calibration technique provides the required low Kvco. In Section 2, the PLL architecture and different blocks are described with an analysis of the loop stability. The design parameters and simulations are considered in Section 3. The measurement setup and measured results are discussed in Section 4, along with the conclusion in Section 5.

2. Proposed PLL Architecture

The classical PLL with the newly introduced circuit block to optimize the conventional architecture is shown in Figure 1. It consists of a reference frequency divider at the input, phase frequency detector (PFD), charge pump, passive loop filter, programmable VCO and automatic band selection circuit. A quartz crystal with a 25 MHz frequency is used as the reference frequency. It is further divided by a multi-modulus frequency divider, N = 5, to generate a 5 MHz reference frequency. The multi-modulus frequency divider is used at the feedback loop M = 66 to match the VCO central frequency with the input reference frequency. The PFD senses the phase difference, and, consequently, the charge pump generates an error current, which charges or discharges the loop filter. After filtering the high-frequency component, a DC control voltage Vctr is received at the input of the VCO. The VCO is replaced with a programmable VCO. The proposed VCO contains a voltage-to-current (V to I) converter with a programmable current digital to analog converter (iDAC) and a four-stage differential ring oscillator as the delay cell. The programmable iDAC is used to optimize the VCO delay cells. The programmable VCO is aided in its operation by the automatic band selection block. The inclusion of auto-ranging and a multiband selection circuit converts a classical PLL into a programmable PLL. It renders the programmable PLL capable of automatically adjusting the nominal center frequency of the VCO to an optimum required value suitable to operate over a wide frequency range. The proposed PLL architecture with a detailed automatic band selection circuit block is shown in Figure 2. On execution, it continuously monitors two important upper band voltages and lower band voltages with DC control voltage Vctr to remain in the desired frequency range. Its sub-block implementation and operation procedure are discussed in the following sections.

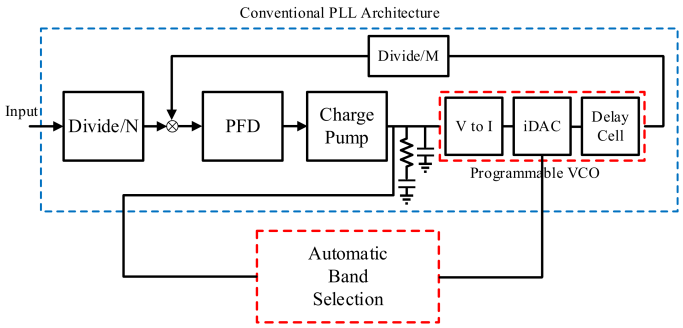
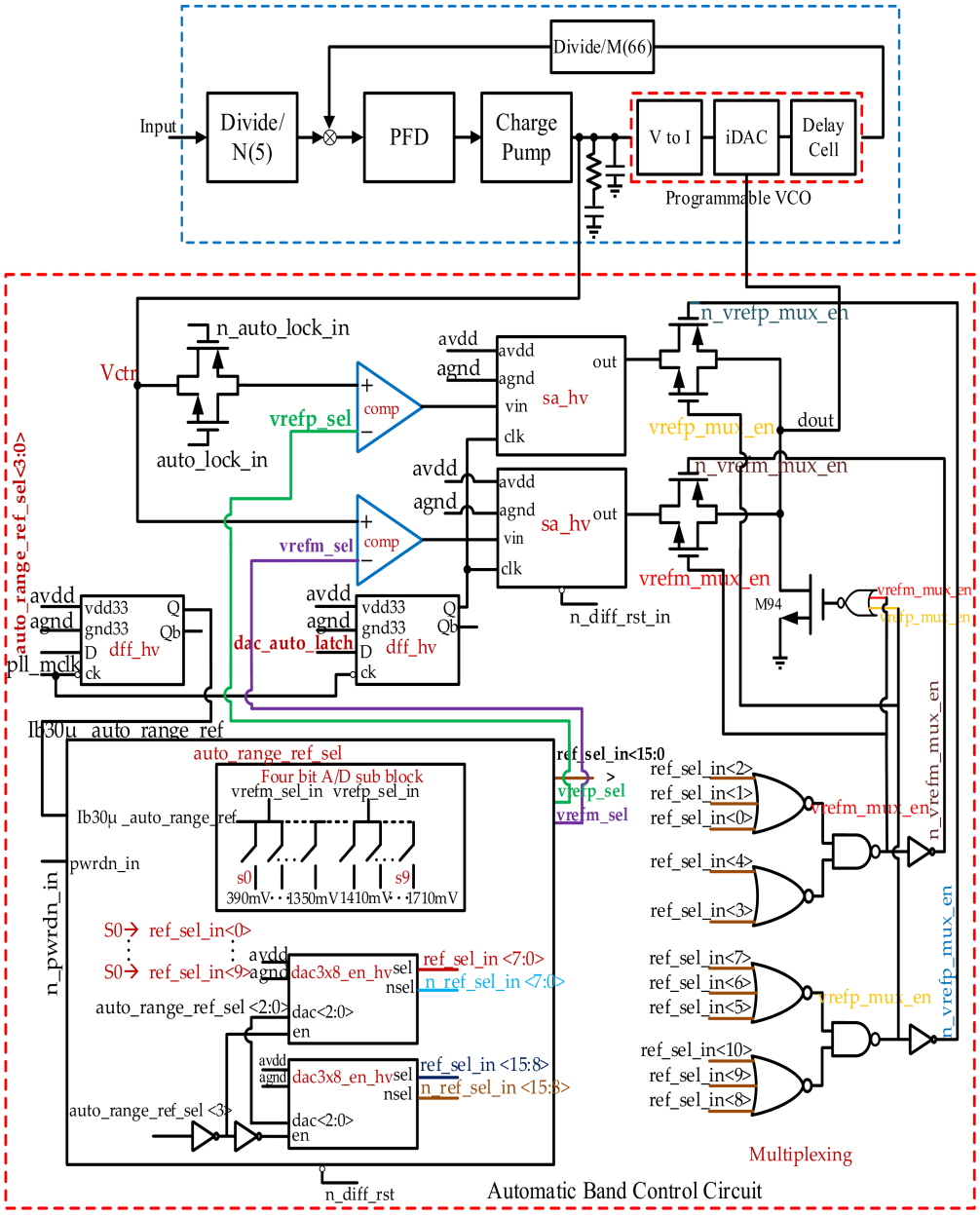


Figure 1. Block diagram of the proposed frequency synthesizer.

2.1. PLL Automatic Band Selection Circuit Block

The automatic band selection circuit block contains 3 × 8 decoders to select 11 voltage reference levels. These voltage levels are implemented by a resistive divider circuit shown in Figure 2b. It also contains a multiplexing circuit and a regenerative latch, followed by a dynamic comparator. The operation of the automatic band selection circuit is implemented by a four-bit ADC and digital control ASIC. The digital control ASIC is the integral part of the automatic band selection circuit. It sends an instruction sequence to generate a digitally controlled algorithm for the automatic band selection circuit to select various voltage levels for the comparison with Vctr. The digital control ASIC ensures a wide frequency operation range and applies self-calibration, whenever the VCO appears to cross frequency limits and to be unable to lock in the present frequency range.



(**a**)

Figure 2. *Cont.*

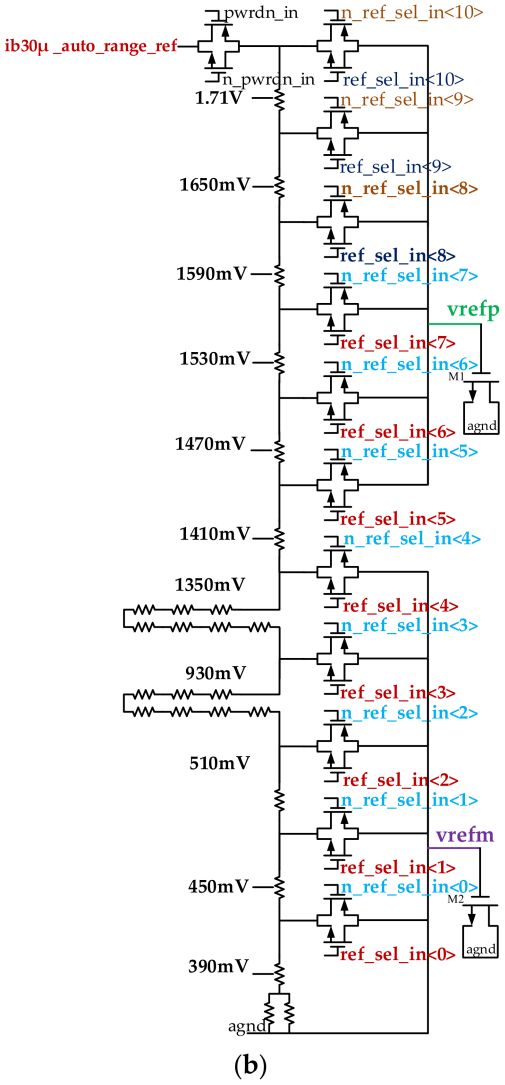


Figure 2. (**a**) Proposed PLL with an automatic band selection circuit; (**b**) four-bit ADC sub-block with two indigenous custom voltage steps.

2.2. Band Selection Procedure

Band selection execution is implemented by the proposed circuit block realization shown in Figure 2a. As shown in the schematic diagram, the four-bit ADC architecture is implemented to generate the 11 reference voltages by using a resistor network and transmission gates. Here, two non-equal customized resistor values are implemented in the divider network to produce the two most probable reference voltage ranges. These two unique voltage levels' resistive circuit is shown in Figure 2b, while the customized voltage values are displayed in Figure 3. Two 3 × 8 decoders were designed to select any one of the 11 reference voltages by enabling the ASIC digital control. One PMOS input pair comparator for a low-range reference voltage and one NMOS input pair comparator for a high-range reference voltage were designed with a hysteresis of 5 mV. These two dynamic comparators compare reference voltages with the DC control voltage Vctr. The comparator output moves to the regenerative latch to strengthen the logic value. To make the circuit compact, two comparators compare the Vctr and reference voltage levels vrefp_sel and vrem_sel multiplexed with eleven voltage levels. Eleven clock cycles are applied sequentially to compare all subdivided voltage reference levels and then obtain the final output voltage at dout.

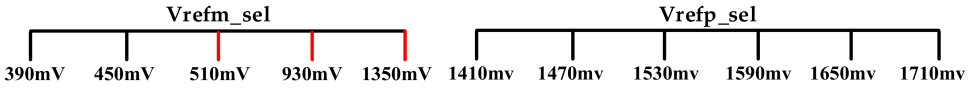


Figure 3. Two major reference voltage levels vrefm_sel and vrefp_sel.

Based on the comparator signal, the band moves/switches to the upper or lower frequency band or may remain in its present frequency band, if Vctr is among Vrefm_sel and Vrefp_sel. There are eleven voltage levels from 390 mV to 1.7 V as reference voltages in the ADC sub-block, out of which two indigenous voltage steps of 420 mV were designed along with the other 60 mV steps for the fast locking of the PLL, with the flexibility of a wide range selection.

In the case that PLL power down is observed for the Vctr, there may be an output at the dout. To overcome this unwanted condition, the circuit block comprises an NMOS, and an NOR gate is implemented at the output (dout), whose inputs are connected with the multiplexing output and ensure a ground path for the Vctr. Hence, based on ASIC mapping, these outputs (dout) move to the iDAC and provide a suitable change in the bias voltage of the delay cell. In the proposed PLL, the most probable locking voltage range is 0.7–1.7 V. The complete locking mechanism is displayed in Figure 4 along with the band selection simulation in Figure 5. In Figure 5, the automatic band selection simulation graph shows the ringing of the DC control voltage and the final convergence. It sequentially compares all eleven voltage references represented by the DAC data latch for one cp_break_d high pulse, then Vctr increases, and the pattern repeats until achieving the final lock-in range.

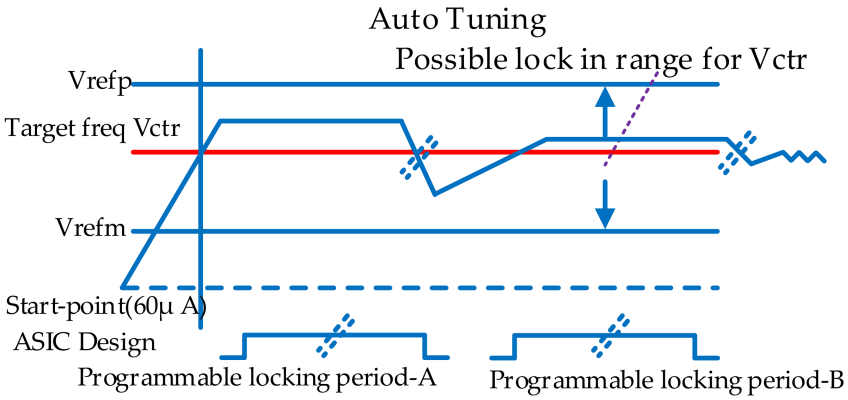


Figure 4. Lock-in range for Vctr with the minimum and maximum Vref levels.

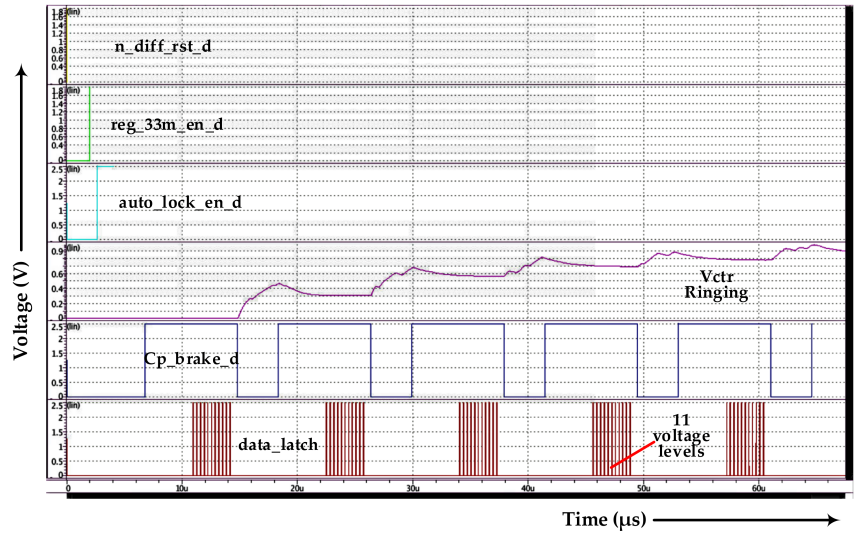
2.3. Programmable VCO Circuit

In the proposed PLL architecture, the VCO is tunable, meaning that its output frequency can be optimized based on the change in the input control voltage.

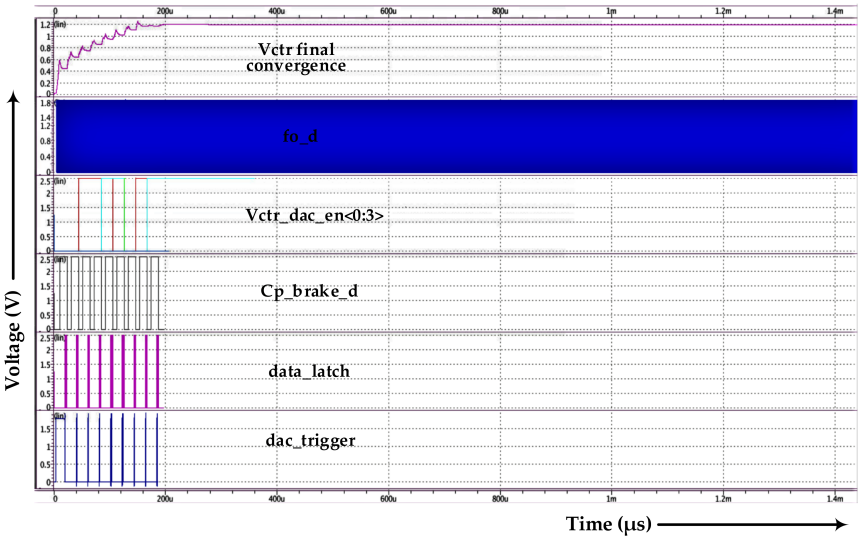
As we know for the VCO output,

$$\omega_{out} = \omega_o + Kvco.Vctr \quad (1)$$

Here, the proposed VCO contains a voltage-to-current (V–I) converter with a programmable iDAC and a four-stage differential ring oscillator as the delay cell. The V–I converter provides a linear relationship between the output current and the control voltage. As Vctr increases, there is a corresponding increment in the output current, and bias Vbp1 is observed with a constant resistor value. The programmable iDAC is used to optimize VCO delay cells by increasing or decreasing the tail current for a change in bias Vbp1<0:3> and Vbp2<0:3> values. A VCO with sub-blocks is shown in Figure 6.



(**a**)



(**b**)

Figure 5. Simulation results of (**a**) automatic band selection circuits (ringing) and (**b**) automatic band selection circuits (final convergence).

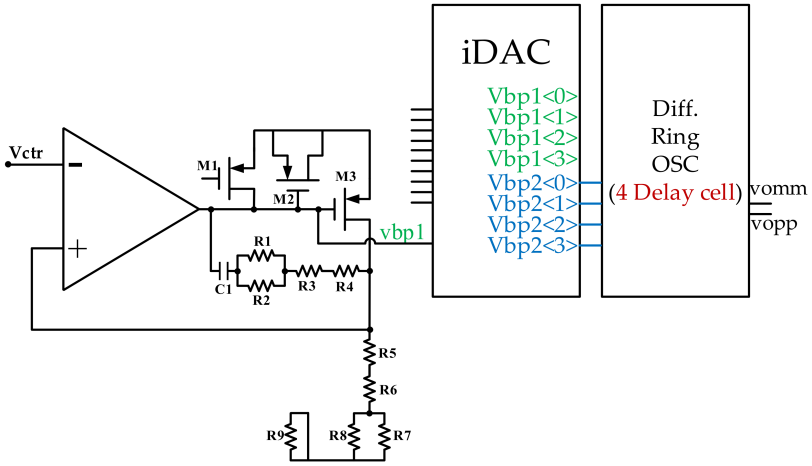


Figure 6. VCO circuit sub-blocks.

2.4. Programmable Current DAC for Wide Frequency Range Selection

Kvco is a VCO frequency/voltage gain having the unit of Hz/V. It measures how much the VCO output frequency changes relative to the VCO input control voltage Vctr change. Kvco is the slope of the curve of frequency vs. Vctr. For a high Kvco, fast settling with higher jitter occurs. It also creates loop stability and accuracy degradation. On the other hand, a very small Kvco value results in a slow VCO response and a narrow output frequency range. Hence, by dividing the target frequency into several sub-bands, each band's Kvco can be reduced. This results in small jitter without sacrificing the required frequency range.

The programmable VCO is optimized by a 3-bit current DAC, which contains a weighted current mirror in section B to generate multiple current values. By using the weighted current mirror, the Kvco gain can be controlled, as with Kvco-1, Kvco-1/4, Kvco-1/8 and Kvco-1/16. It also operates as a DC current into the V–I converter. The programmable iDAC is the most important circuit block of the VCO to obtain a low Kvco gain through multiple VCO bands. The automatic band selection circuit output moves into the iDAC and provides the required change in the bias voltage Vbp2. From Figure 7, Vbp2<0:3> along with Vbp1<0:3> optimizes the delay cell tail current. As we can see in Figure 8a, section B provides multiple band twisting options for retaining a low VCO Kvco gain such as Kvco-1, Kvco-1/4, Kvco-1/8 and Kvco-1/16, while section A further adjusts the Kvco by providing band hopping to obtain the desired centralized frequency operation range.

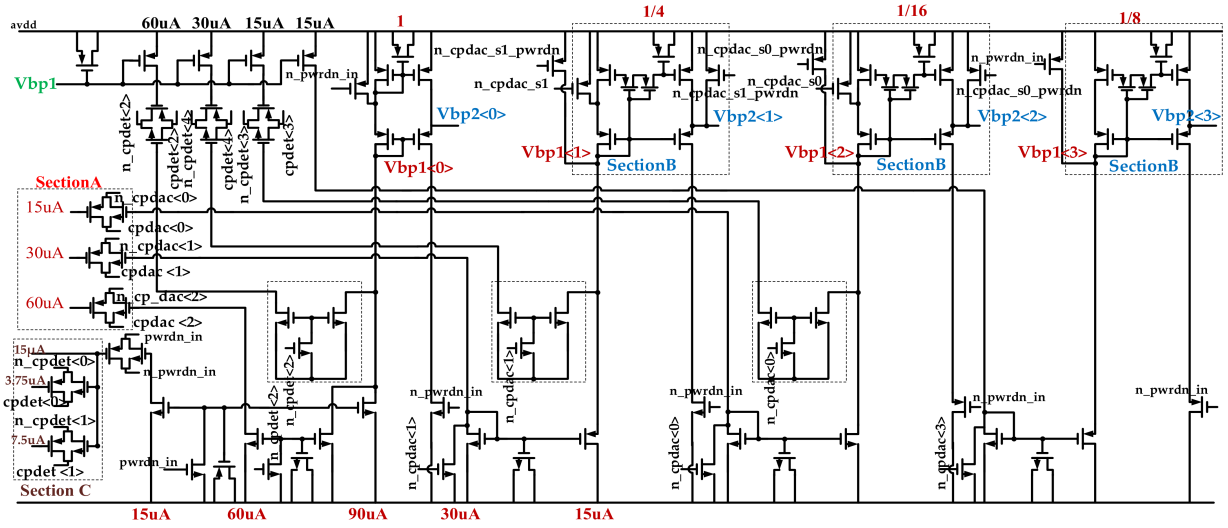


Figure 7. VCO circuit programmable iDAC.

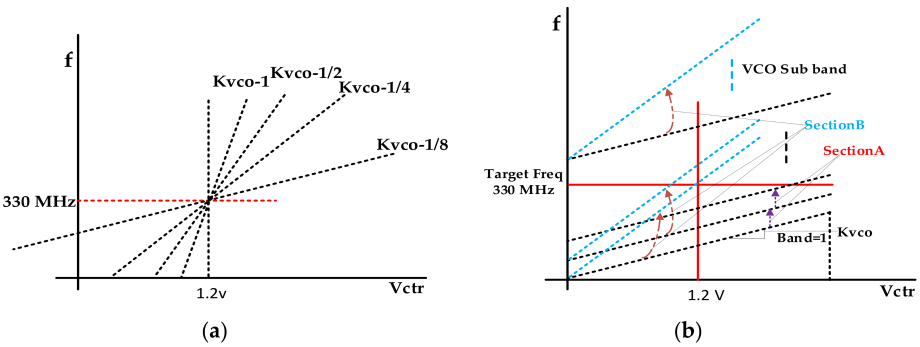
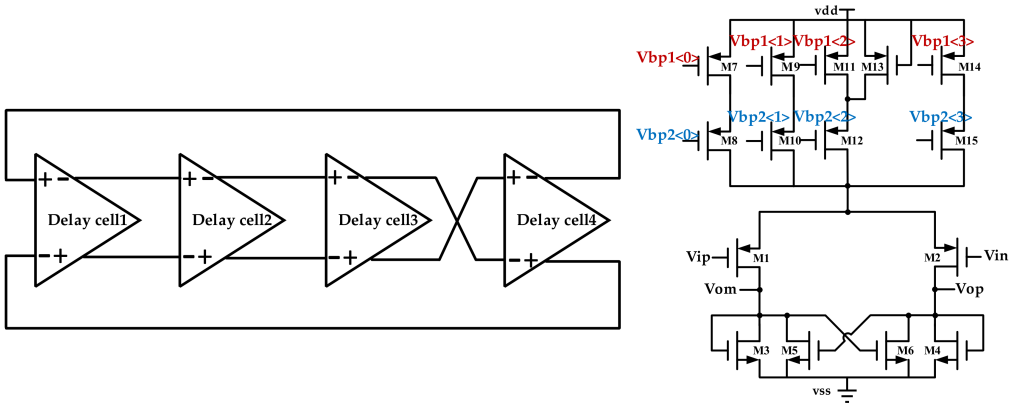


Figure 8. (**a**) Frequency vs. VCO tuning voltage; (**b**) frequency vs. VCO sub-band optimization.

2.5. Four-Stage Differential Ring Oscillator and Delay Cell

The programmable VCO has a four-stage differential ring oscillator for low noise and low power supply applications, as shown in Figure 9a. The circuit of the proposed

delay cell of the differential ring oscillator is shown in Figure 9b. The differential pair of PMOS transistors M1 and M2 acts as the input stage of the delay cell, and the tail current is provided by the different options of the bias voltage generation. The active loads are composed of a pair of NMOS transistors, M3 and M4, and a pair of cross-coupled latches, NMOS transistors M5 and M6.



(**a**) (**b**)

Figure 9. (**a**) Four-stage differential ring oscillator; (**b**) differential cross-coupled delay cell with multiband option.

2.6. s-Domain Analysis

A second order loop filter is implemented to avoid the unwanted ripple occurrence because of the exponential charging of C. The system will oscillate as there is just two integrators, hence the need to add a zero in the system to make it stable by placing an R in series with C [1,17–24]. There is another C_x placed to suppress the jumpy response of the series RC network during charging and discharging. A s-domain analysis block diagram is shown in Figure 10.

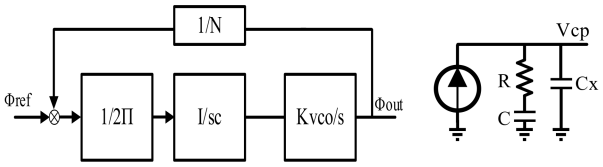


Figure 10. s-Domain analysis block diagram.

Open loop gain:

$$A = \frac{I_0}{2\pi} \cdot \frac{k}{s^2(C + C_X)} \cdot \frac{1 + sCR}{1 + sC_1R} \tag{2}$$

Closed loop gain:

$$\frac{\varnothing_{ref}}{\varnothing_{out}} = \frac{1 + sCR}{1 + sCR + s^2(C + C_X)\frac{2\pi}{I_0K} + s^3\frac{(C+C_X)C_1R2\pi}{I_0K}} \tag{3}$$

The proposed architecture obtains a phase margin of 60°, with C = 600 pF, C_x = 42 pF and R = 24.3 kΩ. Hence, it is a stable system. For a clock synthesizer with a VCO of the frequency range 330 MHz, the feedback divider M in the loop equations is 66 times.

2.7. Programmable Prescaler for 32/33 Divider Ratio

In the proposed PLL, the frequency divider is N = 5 at the input and M = 66 in the feedback loop. A programmable prescaler is used for the frequency divider circuit. Figure 11a

shows a dual-modulus prescaler circuit block that could divide by N or N + 1 according to the external control [2–5]. Here, a dual-modulus prescaler cell is implemented to allow the multi-moduli frequency divider at the input, as well as at the feedback loop, to produce an output frequency equal to the reference frequency. The multi-modulus divider provides flexibility to the PLL architecture and maintains the future relevancy.

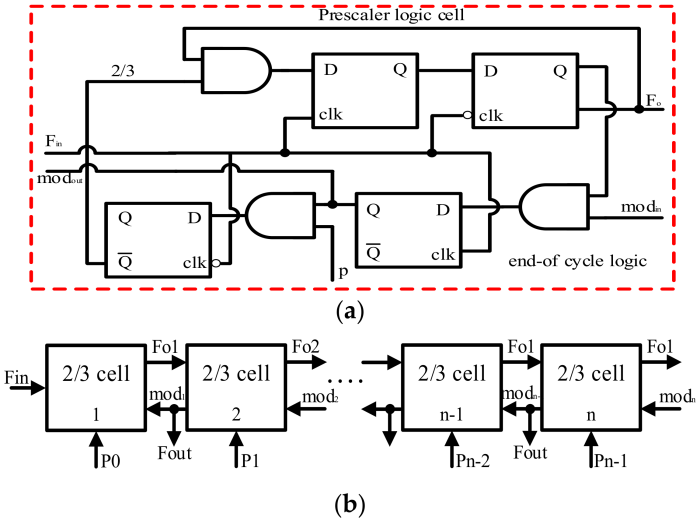


Figure 11. (**a**) Prescaler logic cell; (**b**) multi-modulus divider architecture.

The multi-modulus divider architecture is depicted in Figure 11. It consists of a chain of divide-by-2/3 dual-modulus prescalers in a cascade, connected similarly to a ripple counter. In every division period, the last cell of the dual-modulus prescaler in the chain generates signal $\mathrm{mod}_{\mathrm{in}}-1$. The signal then propagates up the chain. Its simulation is shown in Figure 12.

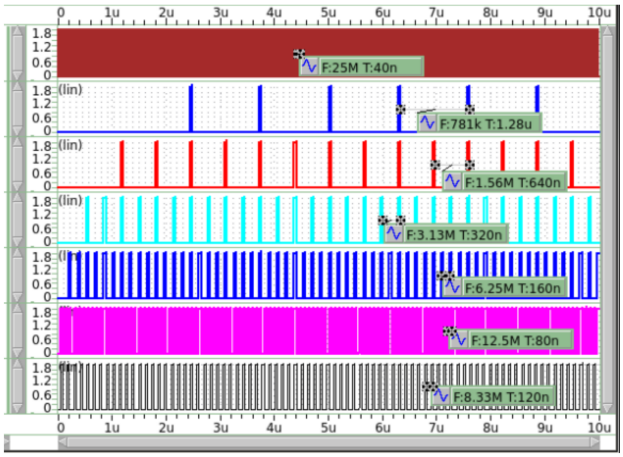
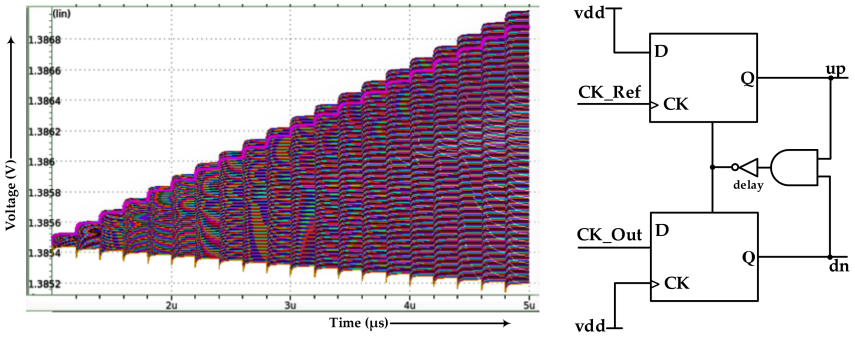


Figure 12. Multi-modulus divider simulation (781 kHz–33 MHz).

2.8. Phase Frequency Detector (PFD)

A PFD compares the rising/falling edge difference between the reference and feedback signals; thus, it can extract not only the phase difference but also the frequency difference. As a PFD detects the phase difference between the reference and the feedback frequency, when there is zero phase difference, it may go into a dead zone. In this condition, the charge pump cannot be fully turned on. In the proposed PLL architecture, the PFD has a dead zone voltage of less than 10 pV, as shown in Figure 13; still, a delay block of the inverter chain is used, having a delay from 0.9 to 2.6 ns in reset to avoid/minimize the unwanted dead zone.



(**a**) (**b**)

Figure 13. (**a**) PFD dead zone simulation; (**b**) PFD block diagram (delay inclusion).

The charge pump requires 1 µs for the Vctr settling after the PFD is off due to the unavoidable I_up and I_dn tail current mismatch. Figure 14 shows the delay setting and inverter chain delay to avoid the dead zone.

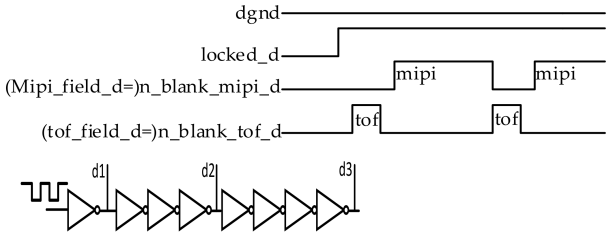
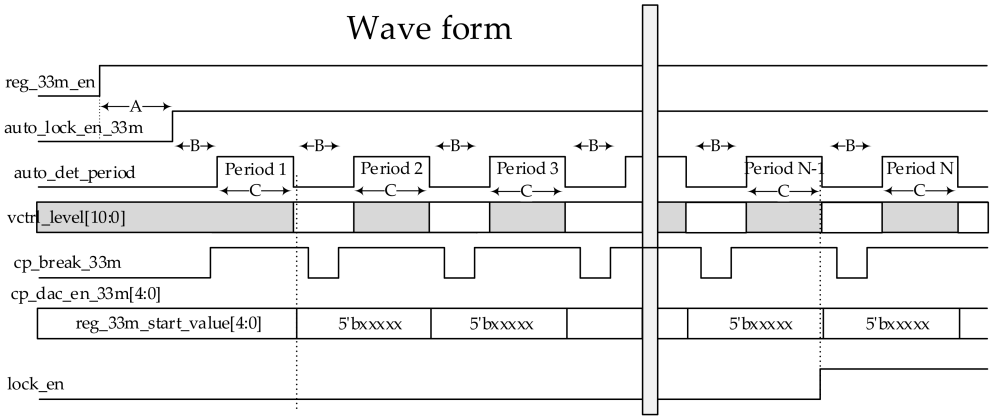


Figure 14. Inverter chain delay (0.3–0.9 ns).

2.9. PLL Locking Operation Sequence Waveform

The PLL locking timing sequence instruction waveform is generated with a digital control ASIC. The locking operation is shown in the following Figure 15. As shown in the diagram, A is the initialization period before enabling PLL locking. It takes some time to initialize all the biasing and to provide a sufficient time margin to all the transition points. When cp_break_33 m is high, then the loop is broken and obtains a stable output frequency, compared with the ASIC block, where the feedback and control of the iDAC change. After this first step, cp_break_33 m moves down, and the loop will continue and use the changed iDAC value to settle. After a certain period of locking, the ASIC compares the frequency again. The process continues several times until reaching a locking value.



A: initial front-porch time of auto_lock_en_33m to reg_33m_en = (reg_33m_init_fp[15:0] + 1) clk
B: low time of auto_det_period = (reg_33m_period_low[15:0] + 1) clk
C: high time of auto_det_period = 88 clk
N: cycles of lock period = reg_33m_lock_cyc[4:0]

Figure 15. PLL locking instruction sequence.

3. Simulation Results

The VCO output frequency with multiple bands is shown in Figure 16a. The Vctr range is 0.4–2.1 V, with a VCO tuning range of 0.84 V. The center frequency of the designed VCO is 330 MHz, with a variation absorption of ±10%, i.e., 297–363 MHz. The frequency sub-band step size is 8.25 MHz, with an average Kvco of 23 MHz. To ensure the wide-range frequency continuity, the two adjacent bands are overlapped with each other up to 30%. Figure 16b depicts a typical VCO gain characteristic at a typical 010 frequency sub-band case.

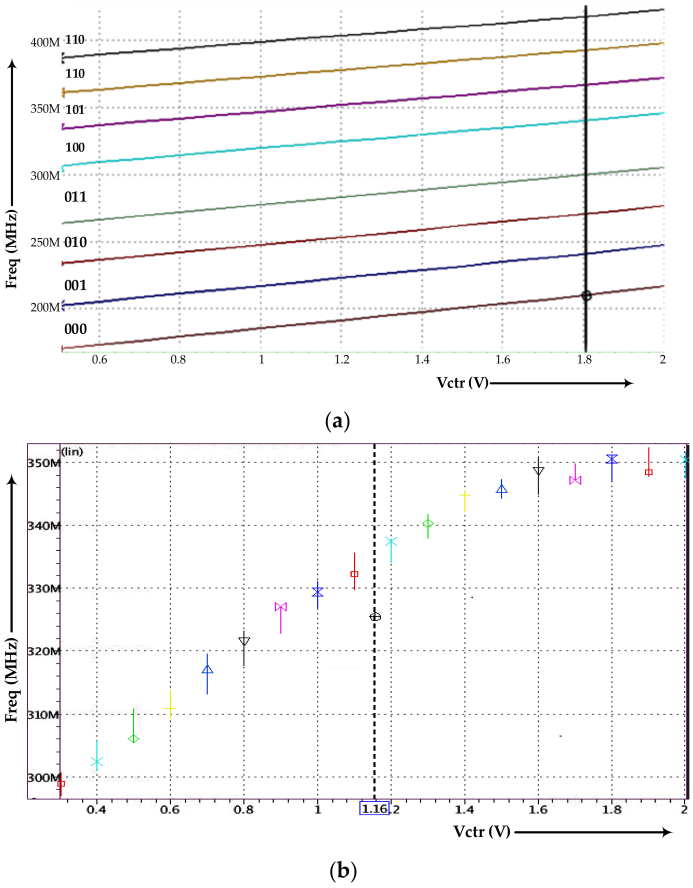


Figure 16. (**a**) VCO multiple bands; (**b**) VCO frequency vs. Vctr for 010 band.

Figure 17 shows the whole PLL closed-loop output and lock-in timing. After converting the time domain output into the frequency domain, the graph shows a stable 33 MHz output frequency.

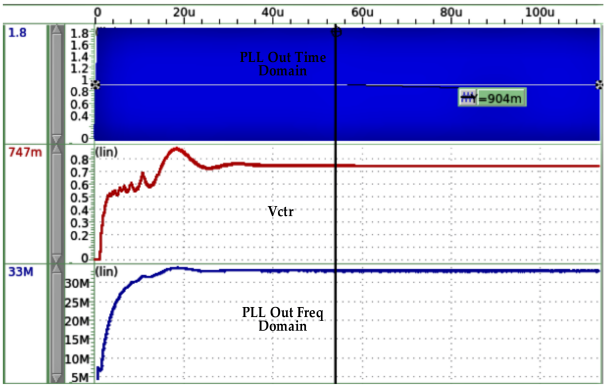


Figure 17. Transient simulation result for whole PLL.

Chip Layout and Results

This chip was fabricated in the TSMC 0.18 µm 1P6M process. The new proposed PLL architecture's complete and compact layout is shown in Figure 18. Its dimensions are 379.765 × 1325.115 µm. The measurement was carried out at the CIC (National Chip Implementation Center).

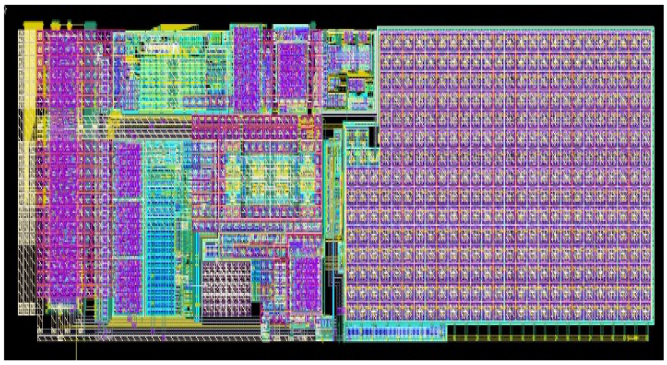


Figure 18. PLL layout (379.765 × 1325.115 µm).

Tables 1 and 2 summarize the performance of the PLL architecture.

Table 1. Summary of PLL post-simulations.

Post_Simulation@TT_50 °C	
Fin (MHz)	25
N	5
M	66
Fvco (MHz)	330
Fout (MHz)	33
C (pF)	600
Cx (pF)	42
R (kΩ)	24.3
Icp (µA)	30
Kvco (MHz/V)	23
BW	18.1 KHz
PM (°)	60
RJrms Jitter (ps)	25

Table 2. Summary of PLL performance.

Process Technology	180 nm
Power Supply	1.8 V
Center Frequency	330 MHz
VCO Tuning Range	0.84 V
Range of Control Voltage	0.4–2.1 V
Kvco	23 MHz/V
Modulus of Divider	66
Reference Frequency	25 MHz
Lock-in Time	40 µs
VCO Gain	23 MHz/V
Bandwidth	18.1 KHz
Power Consumption	2 mW
PLL Layout Area	1.325115 × 0.379765 mm

4. Measurement

This section presents the proposed PLL output measurement results including the duty cycle and the frequency standard deviation. The PLL measurement setup is shown in Figure 19a–c.

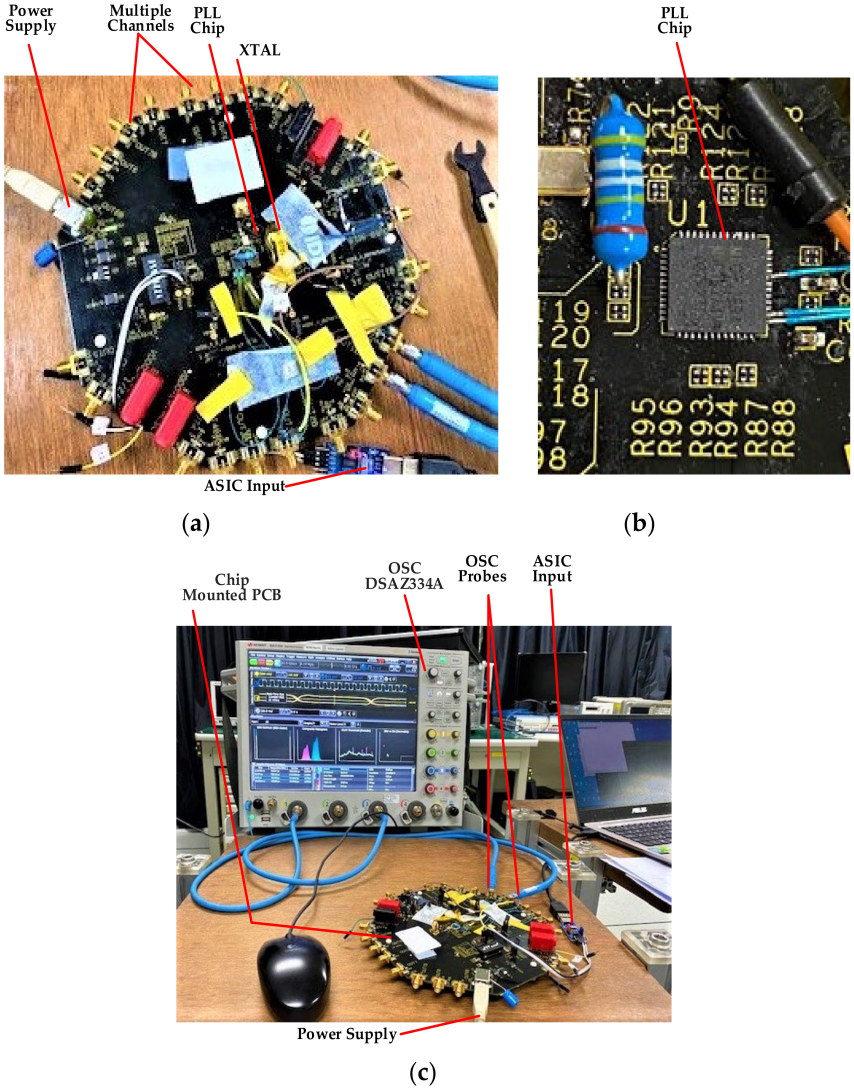


Figure 19. (**a**) PLL chip mounted on PCB; (**b**) PLL chip; (**c**) PLL measurement setup.

4.1. Printed Circuit Board for Measurement

In high-speed chip measurement, the ideal and optimum method is to use a high-speed probe directly on the chip pad. However, due to the large number of pads on the chip, it is difficult to directly probe which requires a wider pad spacing. Therefore, a printed circuit board (PCB) is used in measurement to provide the path for the DC power, bias voltage, bias current, digital control signal and also the input/output signal. As the power supply is placed at a distant position, a capacitor is necessarily added on the PCB to eliminate the noise. In Figure 19a, the printed circuit board with its important components is shown. It contains a quartz crystal for the reference frequency, PLL chip, ASIC input, multiple channels and a supply input.

The SMA connectors are used to monitor the 33 MHz signal, and also for the input reference frequency. The chip is mounted in the middle of a hexagonal PCB to maintain an equal distance from all channels. Bonding wires are used to connect the chip pads and PCB pads. The PCB is made of FR4 material. To eliminate the reflection along its path, 50Ω transmission lines were designed to match the equipment impedance.

4.2. Measurement Results

Figure 19c shows the complete setup overview of the measurements. The chip was measured by a DSAZ334A Infiniium Oscilloscope with a 20 GSa./s sample rate and up to 4,194,304 pts memory depth per channel feature. The oscilloscope was well calibrated and

enabled measuring 6-bit pattern length. Using this oscilloscope, we measured PLL output. Figure 20 shows the PLL output and the corresponding eye diagram. For two rising edges, the measured values of channel 1 (point1) and channel 3 (point 3) are 509 mV with an offset of −14 mV, and 461 mV with an offset of −31 mV, respectively. Table 3 summarizes the measured duty cycle and frequency with standard deviation. The eye diagram in Figure 20 also provides all jitter value information, which is summarized in Table 4. Figure 21a depicts the bathtub histogram for the total jitter (TJ) with a bit error rate of (1E-12), while Figure 21b shows a Gaussian profile for the random jitter (RJrms,narrow).

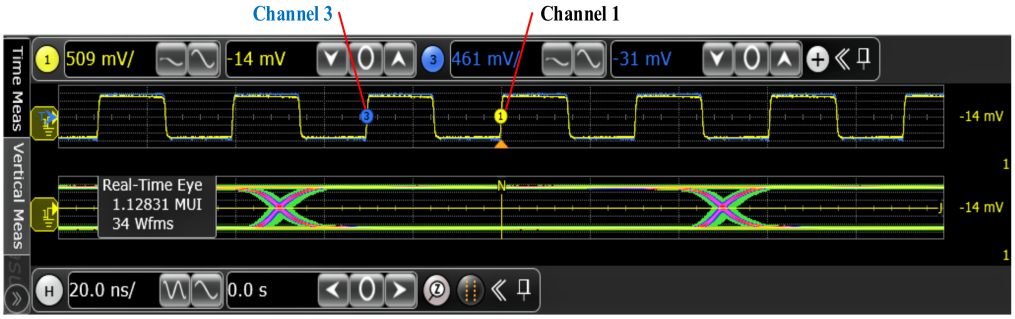


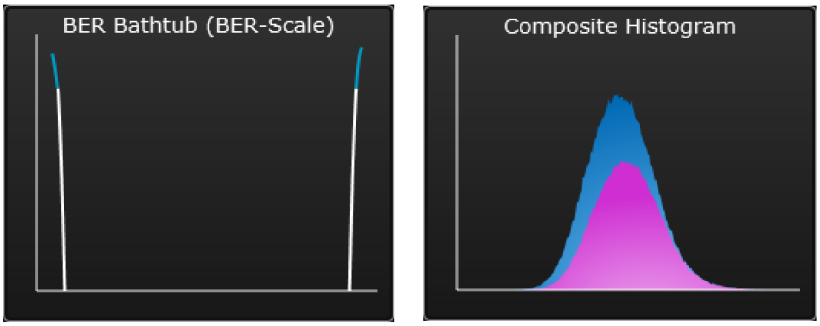
Figure 20. Measured eye diagram.

Table 3. Summary of duty-cycle and frequency measurements for channel 1 (point 1) and channel 2 (point 3).

Measurement	Current	Mean	Min	Max	Range	Std Dev	Count
Duty Cycle (1)	50.10%	50.00%	49.80%	50.30%	450 m%	62.6 m%	235,276
Frequency (1)	32.995145 MHz	32.997494 MHz	32.845768 MHz	33.132852 MHz	287.08341 KHz	43.579266 KHz	235,276
Frequency (3)	33.016368 MHz	32.997502 MHz	32.821353 MHz	33.161631 MHz	340.27749 KHz	46.565005 KHz	325,269
Duty cycle (3)	50.00%	50.00%	49.80%	50.30%	510 m%	66.3 m%	235,269
1 Period (3)	32.28801 ns	30.3053842 ns	30.15533 ns	30.46797 ns	312.64 ps	42.7670 ps	235,269
1 Per-Per (3)	4.22 ps	−2.0 fs	−2.97.72 ps	230.76 ps	528.48 ps	82.1440 ps	235,235
1 Per-Per (1)	7.92 ps	−2.2 fs	−243.87 ps	211.33 ps	455.20 ps	77.7530 ps	235,242
1 Period (1)	30.30749 ns	30.3053838 ns	30.18152 ns	30.44532 ns	263.80 ps	40.0235 ps	235,276

Table 4. Summary of Jitter measurements.

Measurement	Value
Source	Channel 1
RJ Method	Spectral
Data Rate	197.9856 Mb/s
Pattern Length	6 bits
TJ(1E-12)	347.43 ps
RJrms,narrow	19.10 ps
DJδδ	77.70 ps
Transitions	376.002 k
PJrms	21.35 ps
PJδδ	77.70 ps
DDJpp	0.0 s
DCD	11.50 ps
ISIpp	0.0 s
DDPWS	n/a
F/2 (Even/Odd)	n/a
Clock Recovery	Second Order
Edge Direction	Rising
Measurement	TIE (Phase)



(**a**) (**b**)

Figure 21. (**a**) Bathtub histogram (BER Tj Jitter); (**b**) Gaussian histogram (Rj Jitter).

The bathtub curve slope continuity and smoothness along with Gaussian distribution profile show absence of cross talk in the measured jitter.

Table 4 includes the TJ with a bit error rate of (1E-12), RJrms,narrow, the periodic jitter rms value (PJrms) and the duty cycle distortion (DCD). RJ is also known as unbounded jitter, while PJ and DCD are known as bounded jitter. PJ and DCD are parts of deterministic jitter. The total jitter TJ comprises deterministic (bounded) jitter and random (unbounded) jitter. RJrms,narrow measured value is 19.10 ps. The low random jitter ensures precise and stable clock generator application of proposed PLL. This is a spectral jitter measurement, which has more accuracy at critical low cross-talk. Abbreviations are defined below.

5. Conclusions

In this paper, a PLL prototype with a programmable VCO and automatic band selection was presented. The PLL chip was fabricated using the TSMC 0.18 µm 1P6M process. The programmable VCO frequency output was 330 MHz, while a PLL output frequency of 33 MHz was achieved for an input reference frequency of 25 MHz. The PLL prototype is designed for wide-range frequency selection with a low VCO gain to obtain low jitter. The architecture provides multiple overlapped band switching, as well as band twisting, with a programmable current DAC to obtain the desired central frequency operation. The chip measurement results show a 19.10 ps rms jitter. The Gaussian histogram and smooth bathtub curve show no cross-talk. The prototype also has an additional safety feature of a power down mode. It was shown that a differential design approach also reduces noise, possibility in the analog block. The proposed PLL is designed for −40 to s85 °C, a wide temperature range.

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Abbreviations

PLL	Phase-locked loop
Kvco	Voltage-controlled oscillator gain
DAC	Digital-to-analog converter
PDF	Phase frequency detector
PVT Variation	Process, voltage and temperature variation
ADC	Analog-to-digital converter
V to I	Voltage-to-current converter
Vctr	VCO control voltage
PCB	Printed circuit board
DC	Direct current
Fin	Input reference frequency
MHz	Mega hertz
N	Reference frequency divider ratio
M	Feedback frequency divider ratio
Fvco	Voltage-controlled oscillator frequency
Fout	Output frequency
C	Capacitor
R	Resistor
f	Frequency
Icp	Charge pump current
Kvco	Voltage-controlled oscillator gain
BW	Band width
PM	Phase margin
Rj	Random jitter
rms	Root mean square
BER	Bit error ratio
TIE	Time interval error

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