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Device and Circuit Exploration of Multi-Nanosheet Transistor for Sub-3 nm Technology Node

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Abstract: A multi-nanosheet field-effect transistor (mNS-FET) device was developed to maximize gate controllability while making the channel in the form of a sheet. The mNS-FET has superior gate controllability for the stacked channels; consequently, it can significantly reduce the short-channel effect (SCE); however, punch-through inevitably occurs in the bottom channel portion that is not surrounded by gates, resulting in a large leakage current. Moreover, as the size of the semiconductor device decreases to several nanometers, the influence of the parasitic resistance and parasitic capacitance increases. Therefore, it is essential to apply design–technology co-optimization, which analyzes not only the characteristics from the perspective of the device but also the performance from the circuit perspective. In this study, we used Technology Computer Aided Design (TCAD) simulation to analyze the characteristics of the device and directly fabricated a model that describes the current–voltage and gate capacitance characteristics of the device by using Berkeley short-channel insulated-gate field-effect transistor–common multi-gate (BSIM–CMG) parameters. Through this model, we completed the Simulation Program with Integrated Circuit Emphasis (SPICE) simulation for circuit analysis and analyzed it from the viewpoint of devices and circuits. When comparing the characteristics according to the presence or absence of bottom oxide by conducting the above research method, it was confirmed that subthreshold slope (SS) and drain-induced barrier lowering (DIBL) are improved, and power and performance in circuit characteristics are increased.

Keywords: multi-nanosheet FETs; bottom oxide; DTCO; TCAD/SPICE simulation

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1. Introduction

Semiconductor device technology has continued to develop rapidly in line with the rapidly developing information industry. According to Moore's law proposed in 1965, the performance of semiconductor-integrated circuits doubles every 24 months; thus, the development of semiconductor devices has increased at an exponential rate over time. To increase the performance of semiconductors, reduction in the device size and high integration have been achieved in the form of a scale-down in the structure of the metal–oxide-semiconductor field-effect transistors (MOSFETs); however, the development of this type of device has reached its limit. For the MOSFETs to operate correctly, the role of the gate is significantly important; however, as the channel length is shortened, the source and drain become close and the gate cannot perform its role owing to the short-channel effect (SCE) [1,2]. Accordingly, the structure of the device has been developed by increasing the number of junction surfaces between the channel and the gate. The structure has evolved from planar MOSFETs with one channel–gate junction surface to fin-shaped field-effect transistors (FinFETs) [3] with three channel–gate junction surfaces, thereby increasing the control by gates and enabling technology nodes to develop up to several nanometers.

However, the structure of FinFETs has also reached its limit as the size of technology nodes has been reduced to less than 3 nm; consequently, it has become essential to develop a device having a gate-all-around (GAA) structure, which wraps all parts of the channel with a gate [4,5]. Such a structure maximizes the channel control capability of the gate. Owing to this structure, the SCE is significantly improved, and the operating voltage can be reduced. A typical GAA-structured transistor is in the form of a nanowire in which the channel region has a cylindrical and elongated shape. However, the channel width is not sufficiently wide to allow the flow of a large amount of current; therefore, it is difficult to obtain sufficient current in the nanowire structure. To compensate for this, a nanosheet transistor structure was developed. In this structure, the area where the channel touches the gate is maximized by modifying the wire-shaped channel structure into a nanosheet. However, there is a disadvantage as a large leakage current component is generated owing to punch-through due to the SCE in the lower channel portion that is not surrounded by the gate. To prevent this leakage current, a punch-through stopper (PTS) doping was added to the existing multi-nanosheet transistor to minimize the occurrence of leakage current; however, the increase in process cost owing to PTS doping appears to be a significant disadvantage [6,7]. Therefore, by using a structure in which an insulator is added to the lower part of the source and drain regions, instead of PTS doping, to prevent leakage current components, it is possible not only to reduce the process cost but also to simplify the process.

A technology node represents a specific semiconductor manufacturing technology and design rule. In general, as the size of the technology node decreases, the transistor size decreases, resulting in faster and more power-efficient features [8,9]. The name of the technology node was originally based on half the length of the gate or half the pitch between the lowermost interconnections; however, currently, owing to the limitations of Moore's law, this naming is not well maintained. Thus, as the technology node becomes increasingly smaller, micro-processing becomes technically difficult and the design cost of the chip also increases exponentially. Therefore, it is significantly important to develop and design semiconductor devices through simulation before actual fabrication. As technology nodes become smaller, in the order of several nanometers, the simulation method requires design–technology co-optimization (DTCO) that not only refines but also optimizes the design process. The use of DTCO technology has the advantage of shortening the time to commercialization as well as achieving cost reduction in the advanced process development of semiconductor devices. In addition, DTCO technology can be used to reduce the cell area in situations where it is difficult to obey Moore's law because of the limitation of miniaturization. By reducing the cell area, it is possible to increase the degree of integration, which can supplement the limitations of Moore's law to a certain extent; consequently, it is necessary to utilize DTCO technology [10–12].

Therefore, in this study, calibration was performed to extract parameter values to be used for accurate analysis of the channel portion and drift–diffusion simulation for multi-nanosheet field-effect transistor (mNS-FET) devices. In simulation-based studies of such nanoscale devices, a calibration process is essential to increase accuracy. The TCAD calibration process can be carried out in two main directions as follows. (1) The value calculated at the lower level of material properties and carrier transport is used as a calibration target, and (2) the measured value of the made device is used as a calibration target. In this study, we take the process of calibrating a drift–diffusion-based carrier transport model for computational efficiency after obtaining accurate, raw data by solving a Monte Carlo (MC)-based Boltzmann transport equation operation. This is detailed in the paper [13] previously published by our research group. In addition, the physical dimensions (e.g., Contacted poly pitch, Gate length, Source/Drain length) in the recent nanoscale technology node have very different characteristics for each foundry company that develops semiconductor process technology, even in the same technology node [14]. Since the specific physical dimensions have not yet been known for the 3 nm technology node, the most recently announced content is utilized in this paper, considered from the

International Roadmap for Devices and Systems (IRDS) for the 7 nm technology node [15]. Second, the extracted parameters were applied to the entire device structure to perform a drift–diffusion simulation. Third, the characteristic graph of the device, which is a simulation result, was extracted. Fourth, we directly manufactured a model that describes the extracted device characteristic graph. Then, the Berkeley short-channel insulated-gate field-effect transistor–common multi-gate (BSIM–CMG) parameter was used. Finally, SPICE simulation for circuit analysis was conducted, based on a manually created model, and the circuit characteristics were analyzed.

2. Analysis of Characteristics According to the Presence or Absence of Bottom Oxide

2.1. Device Characteristic Analysis

To proceed with the technology–computer-aided design simulation to perform the analysis at the device level for the mNS-FET device, refer to the prediction roadmap for the 3/2.1/1.5 nm technology nodes of the International Roadmap for Devices and Systems (IRDS) institute, as listed in Table 1. As shown in Figure 1, an mNS-FET structure has nitride in the spacer area, and the channel is surrounded by SiO_2 and HfO_2. Figure 1a shows a structure where an insulator is added to prevent the leakage current component of the lower channel, and in Figure 1b, the existing mNS-FET structure is illustrated. In Table 1, the structural information of all mNS-FET devices is specifically listed.

Table 1. Detailed structural information of the multi-nanosheet field-effect transistor device of a 3 nm technology node.

Technology Node	**3 nm**	**2.1 nm**	**1.5 nm**
Symbol (Units)		**Value**	
L_{sp} (nm)	6	5	4
L_{sd} (nm)	8.5	9	10
L_g (nm)	16	14	12
T_{ch} (nm)	8	7	6
T_{sp}(nm)	10	10	10
T_{ox} (nm)	0.3	0.27	0.27
T_{hk} (nm)	1.1	1.1	1.1
T_{BO} (nm)	20	20	20
W (nm)	30	30	30

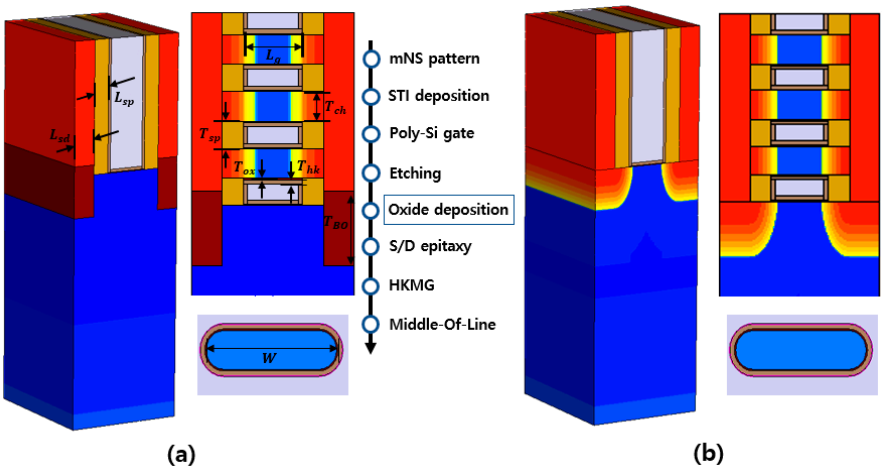

Figure 1. Three-dimensional scheme and cross-section of the multi-nanosheet field-effect transistor (mNS-FET): (**a**) mNS-FET with bottom oxide; (**b**) mNS-FET without bottom oxide.

Before proceeding with the simulation of the entire structure, for an accurate analysis of the channel part, as shown in Figure 2, a structure considering one part of the channel of

the mNS-FET was created separately, and a Monte Carlo simulation [16,17] was performed to calibrate the drift–diffusion simulation. Then, the values of the trajectory transport coefficient and velocity saturation parameter were extracted. The reason for using this simulation is that complementary metal–oxide-semiconductor technology has evolved to a technology node of 10 nm or less, ballistic transport alone cannot quantitatively explain the loss of mobility in a small channel length, and the Boltzmann transport equation must be solved. Figure 3 shows the Monte Carlo simulation results and the calibration results of the drift–diffusion simulation through the above process. Figure 3a shows the results for the N-type structure and Figure 3b shows the results for the P-type structure.

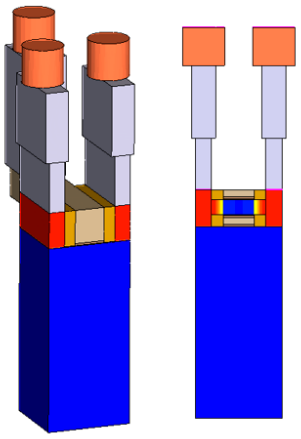

Figure 2. Three-dimensional scheme and cross-section of the simple mNS-FET structure.

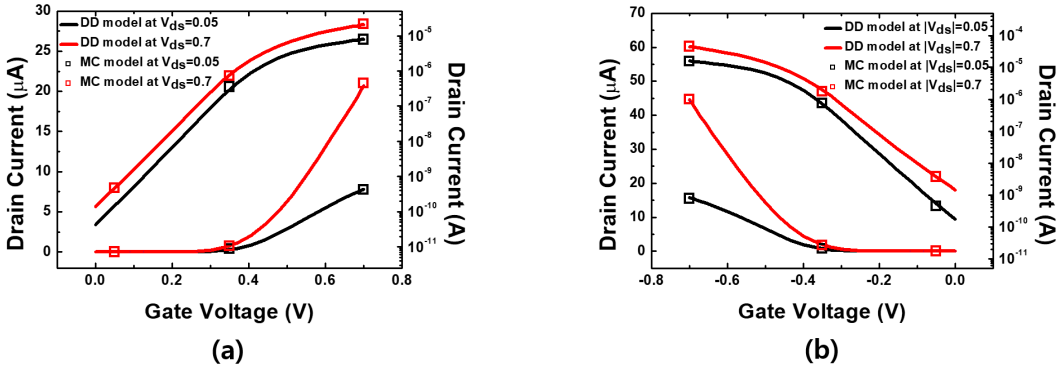

Figure 3. Calibration result between Monte Carlo simulation and drift–diffusion simulation: (**a**) N-type and (**b**) P-type.

Figure 4 shows the current–voltage characteristic graph according to the presence or absence of bottom oxide in the entire structure by applying the parameters extracted as the calibration result. At this time, targeting was performed so that the off-current value could be 0.1 nA when the supply voltage was 0.7 V, by adjusting the work function. As a result of targeting and comparing the graphs, it was confirmed that the on–off ratio was larger in the structure with bottom oxide in both N- and P-types. Through the graph, the characteristics of the device, that is, subthreshold slope (SS) and drain-induced barrier lowering (DIBL), were obtained, which are listed as specific values in Table 2. In particular, the following formula was used to calculate the DIBL value.

$$\mathrm{DIBL}[\mathrm{mV/V}] = \frac{|V_{t_{lin}} - V_{t_{sat}}|}{|V_{DD} - 0.05|} \times 1000 \quad (1)$$

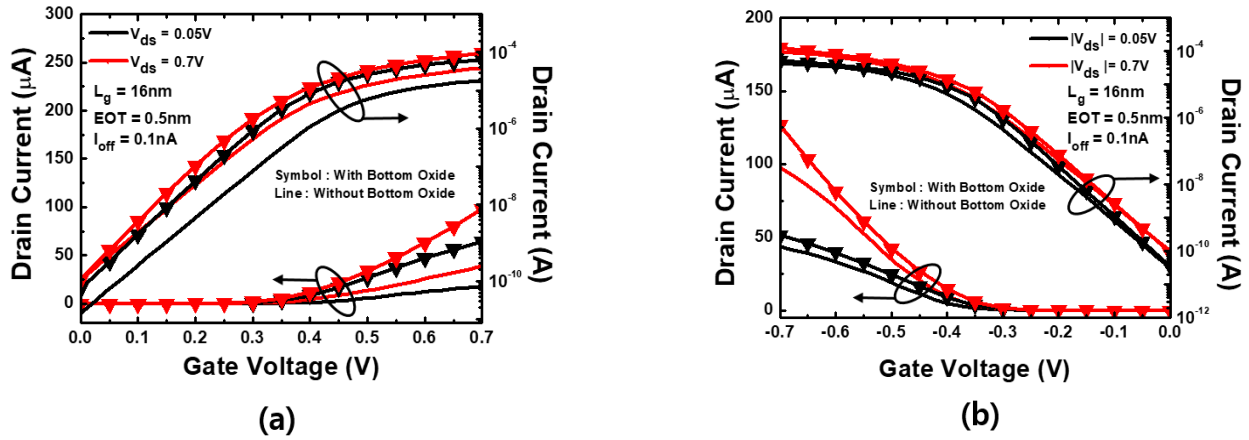

Figure 4. Current–voltage characteristic graph according to the presence or absence of bottom oxide: (**a**) N-type; (**b**) P-type.

Table 2. Specific values of subthreshold slope (SS) and drain-induced barrier lowering (DIBL).

Type	Structure	SS(mV/dec)	DIBL(mV/V)
NMOS	With BO	66.259	43.077
	Without BO	80.442	107.692
PMOS	With BO	67.516	33.846
	Without BO	72.028	49.231

To determine the threshold in the linear region, a specific current value was set in the current–voltage graph when the drain voltage was low; moreover, the gate voltage was determined when the specific current value was set to the threshold in the linear region. The gate voltage in the saturation region was also determined as the gate voltage when it had a specific current value. At this time, the specific current value was determined using the following equation:

$$I_{ds}[A] = 100 \times \frac{W}{L} \times 10^{-9} \quad (2)$$

As shown in Equation (2), the method of extracting the threshold voltage using a constant current is very simple and convenient compared to the classical method [18–20].

From Table 2, it can be confirmed that the SS and DIBL characteristics were improved, regardless of the N- or P-type in the structure, with the bottom oxide structure. Figure 5 shows the comparison of the measured current–voltage characteristics of the multi-nanosheet FET, fabricated in the previous paper [4], to the TCAD simulation used in this paper. Although it is difficult to make a perfect comparison because all device dimension values are not clearly presented in [4], it is confirmed that there is no significant difference from our TCAD simulation results. Note that the comparison was made only for N-Metal Oxide Semiconductor (NMOS). This is because N/P-Metal Oxide Semiconductor (N/PMOS) is expected to have symmetric current–voltage characteristics because off-current target and on-current balancing are performed with the same N/PMOS current characteristics. Therefore, in the current–voltage characteristic graph, it can be observed that when the bottom oxide is present, the leakage current component of the lower channel is controlled, and performance is improved correspondingly. Gate capacitors can be largely divided into parasitic capacitor components and intrinsic capacitor components. As technology nodes become smaller, the influence of parasitic capacitor components increases and is a major cause of deterioration in performance owing to the increase in the delay time in devices and circuits. As shown in Figure 6, it can be observed that the structure with bottom oxide has a smaller gate capacitor value. Unlike the existing structure, it can be

observed that the bottom oxide occupies the source/drain portion, and thus, the parasitic capacitors in the gate-source and gate-drain portions are reduced.

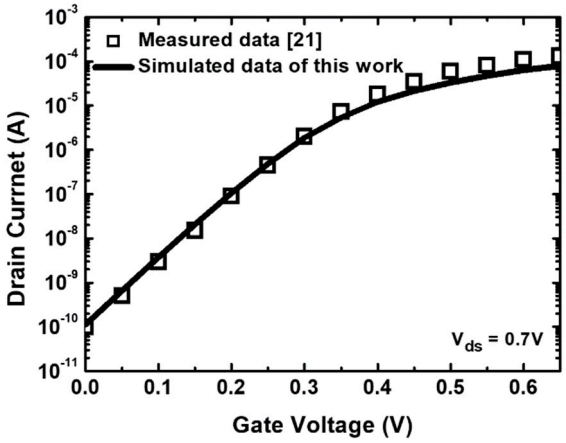

Figure 5. Comparison of current–voltage characteristics of simulation results and measured results.

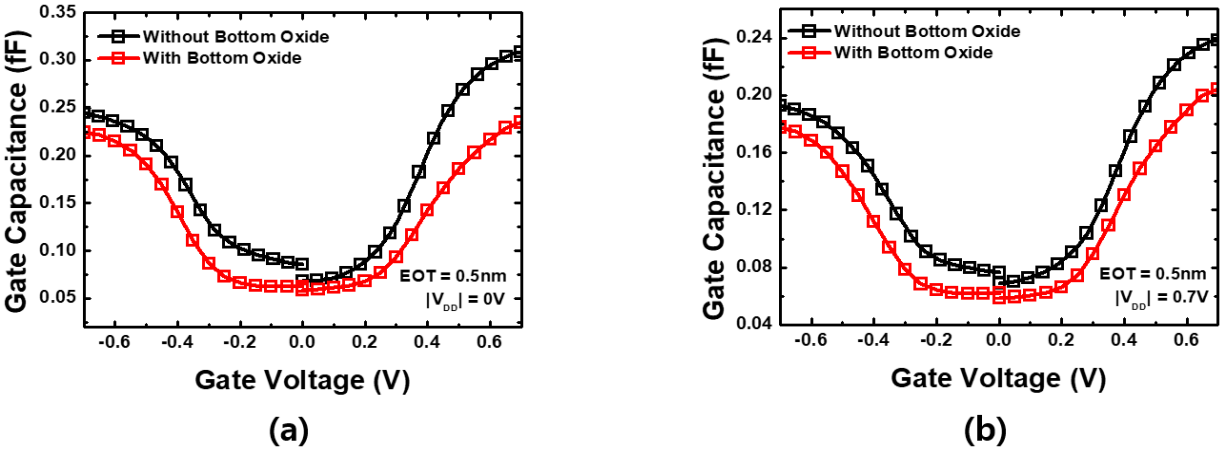

Figure 6. Gate capacitance characteristic graph according to the presence or absence of bottom oxide: (**a**) $|V_{DD}| = 0$ V; (**b**) $|V_{DD}| = 0.7$ V.

As shown in Figure 6, since the capacitance value is very small in the nanoscale technology node, it is difficult to accurately measure due to the resolution limit of the measurement equipment, so the TCAD simulation characteristics can be utilized very usefully.

2.2. Circuit Characteristic Analysis

Before proceeding with the analysis at the circuit level, Figure 7 shows that the off-current for each N- and P-type was set as 0.1 nA, according to the presence or absence of bottom oxide.

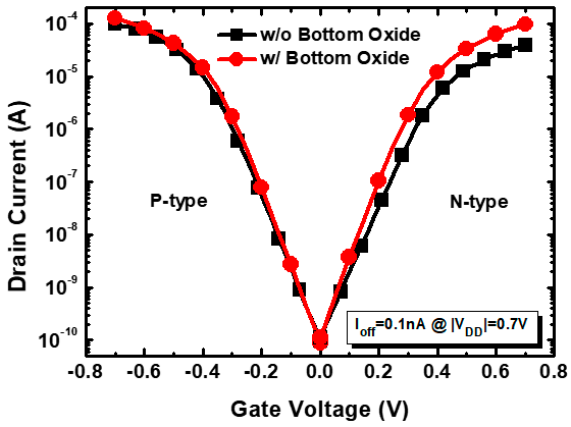

Figure 7. Off-current targeting according to the presence or absence of bottom oxide.

After creating a model using the BSIM–CMG parameters, circuit analysis was performed by benchmarking the circuit diagram, as shown in Figure 8 [21].

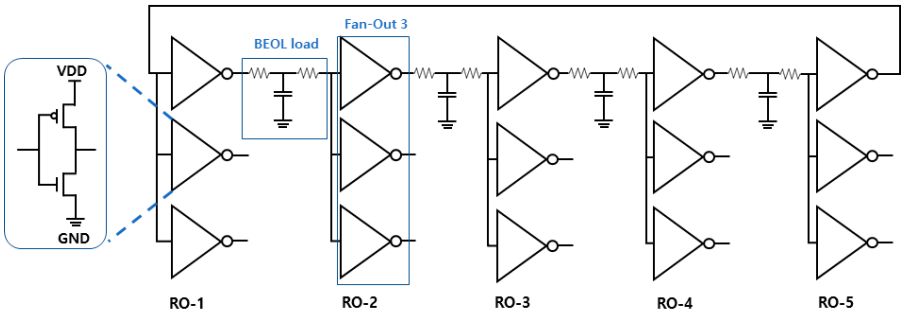

Figure 8. Benchmark circuit with five-stage ring oscillator, a fan-out of three, and backend-of-line (BEOL) load.

Then, the contact resistance, resistance of the backend-of-line (BEOL) load, and BEOL capacitance were set, as listed in Table 3.

Table 3. Values of contact resistance, backend-of-line (BEOL) resistance, and BEOL capacitance.

Technology Node (nm)	R_{cont}[Ω/um]	R_{BEOL}[Ω/um]	C_{BEOL}[aF/um]
3	257	497	314

Based on the circuit diagram in Figure 8, we confirmed the performance improvement in terms of power consumption and speed of the circuit. Figure 9 shows the performance graph according to the presence or absence of the BEOL load. Figure 9a shows the performance graph when there is no BEOL load according to the supply charge, and Figure 9b illustrates the performance graph when there is a BEOL load. From the graph, it can be observed that the graph is located on the right at all supply voltages when the result of the structure with bottom oxide is compared with the result of the structure without bottom oxide, regardless of the presence of the BEOL load. This result indicates that when bottom oxide is present, the speed is improved for the same power consumption and the power consumption is reduced at the same speed.

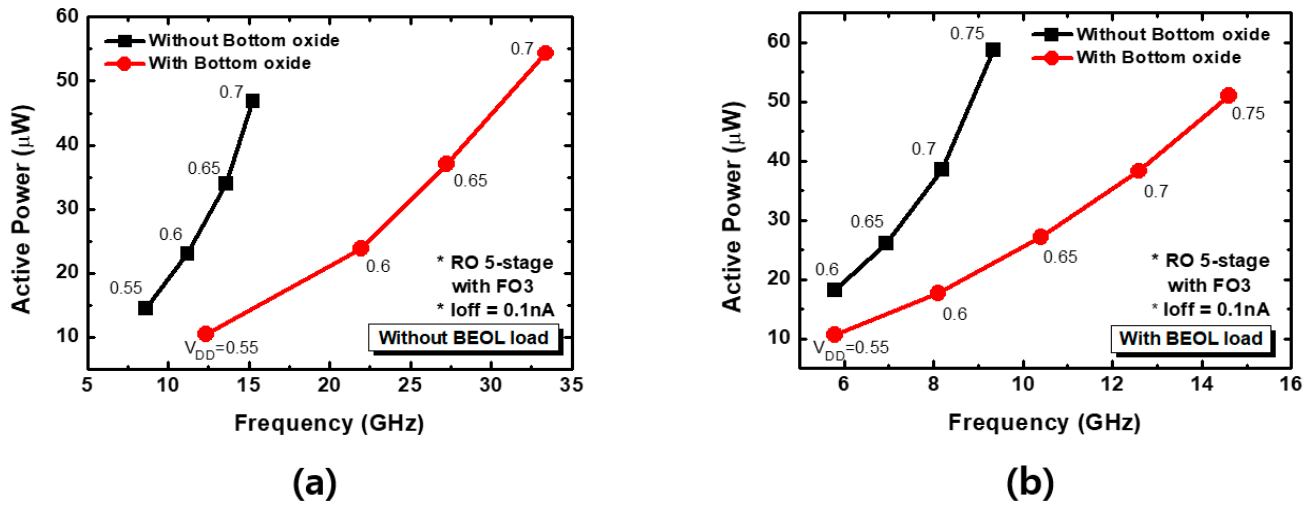

Figure 9. Power–frequency graph according to BEOL load: (**a**) without BEOL load and (**b**) with BEOL load.

In the structure with bottom oxide, it was confirmed that both device and circuit characteristics were improved. To verify the improvement of the characteristics in more detail, the change in components according to the presence or absence of bottom oxide was investigated through segmentation of the resistance and capacitor components. In Figure 10a,b, the capacitor components are segmented according to the presence or absence of bottom oxide, respectively. To compare the components of the capacitor, the capacitor components of the BEOL load, parasitic capacitor components, and intrinsic capacitor components were divided. In Figure 10a, it can be observed that the parasitic resistance component occupies approximately half of the total capacitance component and is reduced by more than 10% in Figure 10b when bottom oxide is present. In Table 4, the total capacitor value and the capacitance component, which change depending on the presence or absence of bottom oxide, are listed as specific values. As can be observed from the table, the presence of bottom oxide reduces the total capacitor value by approximately 32%. In addition, it was confirmed that the reduction in parasitic and intrinsic capacitor components decreased at most by approximately 50%.

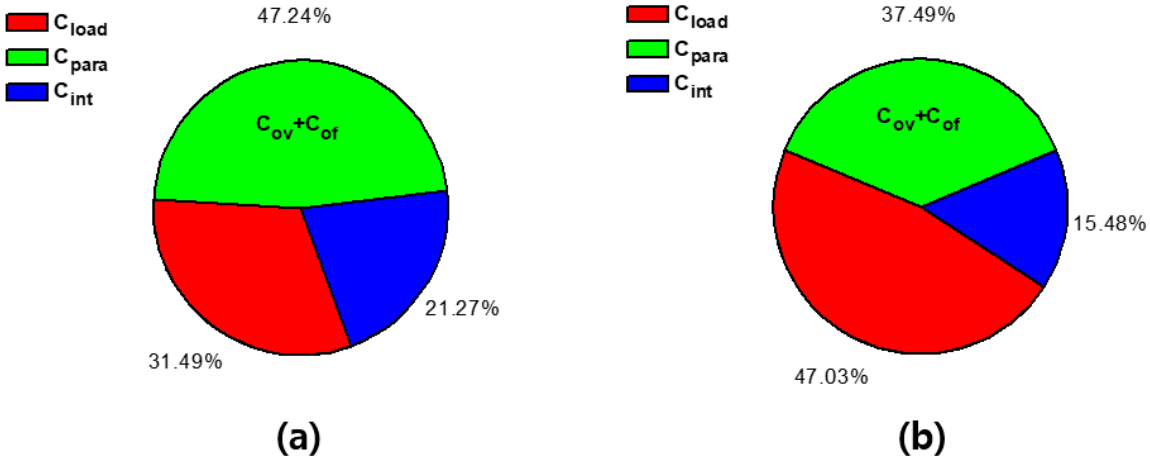

Figure 10. Components of capacitance according to the presence or absence of bottom oxide (%): (**a**) without bottom oxide; (**b**) with bottom oxide.

Table 4. Capacitance value and rate of change according to the presence or absence of bottom oxide.

Capacitance Component	Without BO	With BO	Variation Ratio [%]
C_{eff_total} [fF]	1.82	1.24	−31.868
C_{load} [fF]	0.57	0.577	+1.22
C_{para} [fF]	0.855	0.46	−46.199
C_{int} [fF]	0.385	0.19	−50.649

Figure 11a,b shows the resistance components according to the presence or absence of bottom oxide, respectively. The resistance components constituting all components were divided into BEOL load resistance, contact resistance, and intrinsic resistance components, and compared. From the graph, it can be observed that among the three components, in the structure with bottom oxide, the intrinsic resistance component decreases at the largest rate. For a more accurate comparison, the rate of change was measured by comparing the resistance values of each component according to the presence or absence of bottom oxide, which is listed in Table 5. Owing to the presence of bottom oxide, the total resistance component decreased by approximately 7.5%; moreover, it can be observed that the intrinsic resistance component is the component that causes the total resistance component to decrease.

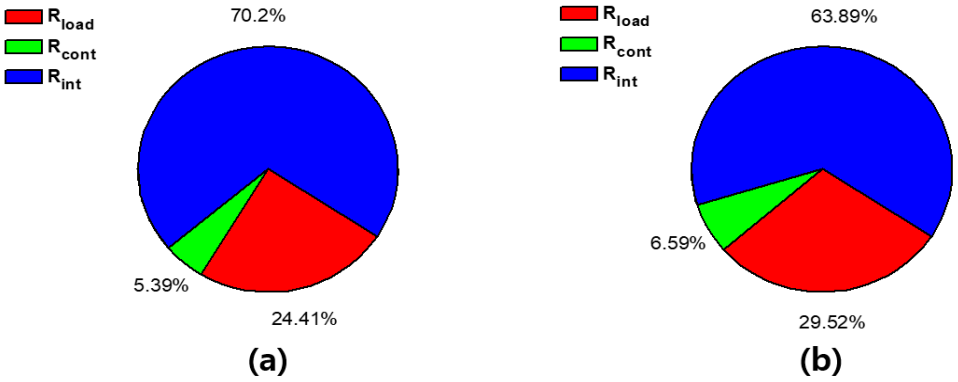

Figure 11. Components of resistance according to the presence or absence of bottom oxide (%): (**a**) without bottom oxide; (**b**) with bottom oxide.

Table 5. Resistance value and rate of change according to the presence or absence of bottom oxide.

Resistance Component	Without BO	With BO	Variation Ratio [%]
R_{eff_total} [kΩ]	6.923	6.402	−7.514
R_{load} [kΩ]	1.69	1.89	+11.834
R_{cont} [kΩ]	0.373	0.422	+13.137
R_{int} [kΩ]	4.86	4.09	−15.844

3. Analysis of Characteristics According to the Position of Bottom Oxide

Analyses at the device and circuit levels according to the presence or absence of bottom oxide were conducted in a previous study. Based on the previous study, it was confirmed that both the device and circuit characteristics were improved in the structure of the device with bottom oxide. Therefore, in this study, the same research was conducted on structures with different locations of the bottom oxide. As shown in Figure 12, three structures were fabricated according to the location of the bottom oxide. Figure 12a illustrates the "Top" structure, where the location of the bottom oxide predominantly occupies the source/drain; Figure 12b illustrates the "Center" structure, where the bottom oxide occupies a small portion of the source/drain; Figure 12c illustrates the "Bottom" structure, where the bottom

oxide does not occupy portions of the source/drain.

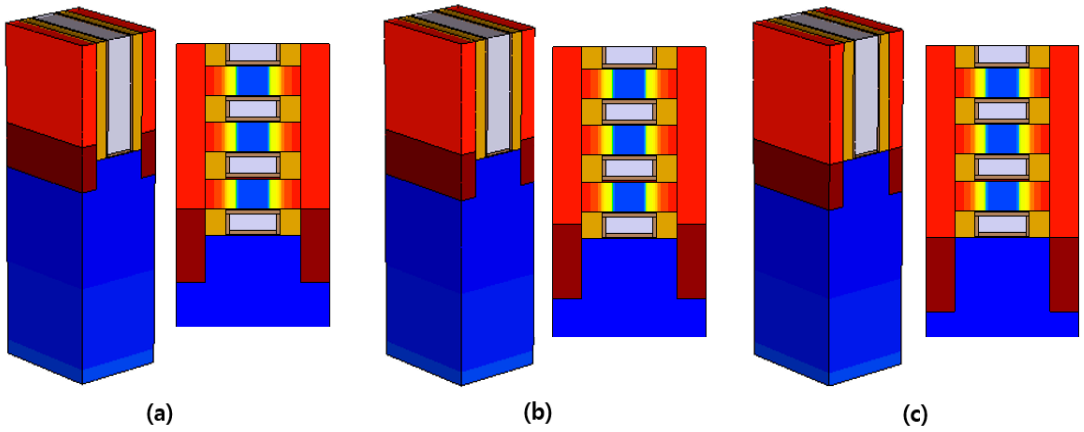

Figure 12. Structure and cross-sectional view according to bottom oxide location: (**a**) Top; (**b**) Center; (**c**) Bottom.

3.1. Device Characteristic Analysis

Figure 13 shows the graphs of the current–voltage characteristics according to the location of the bottom oxide in the N- and P-type devices. Similarly, targeting was performed by adjusting the work function. In the N- and P-type device, when the absolute drain voltage is 0.7 V, the off-current value is 0.1 nA, as shown in Figure 13b,d. As a result of targeting and comparing the current–voltage graphs, it was confirmed that the on–off ratio was further improved in the structure with bottom oxide in both N- and P-types.

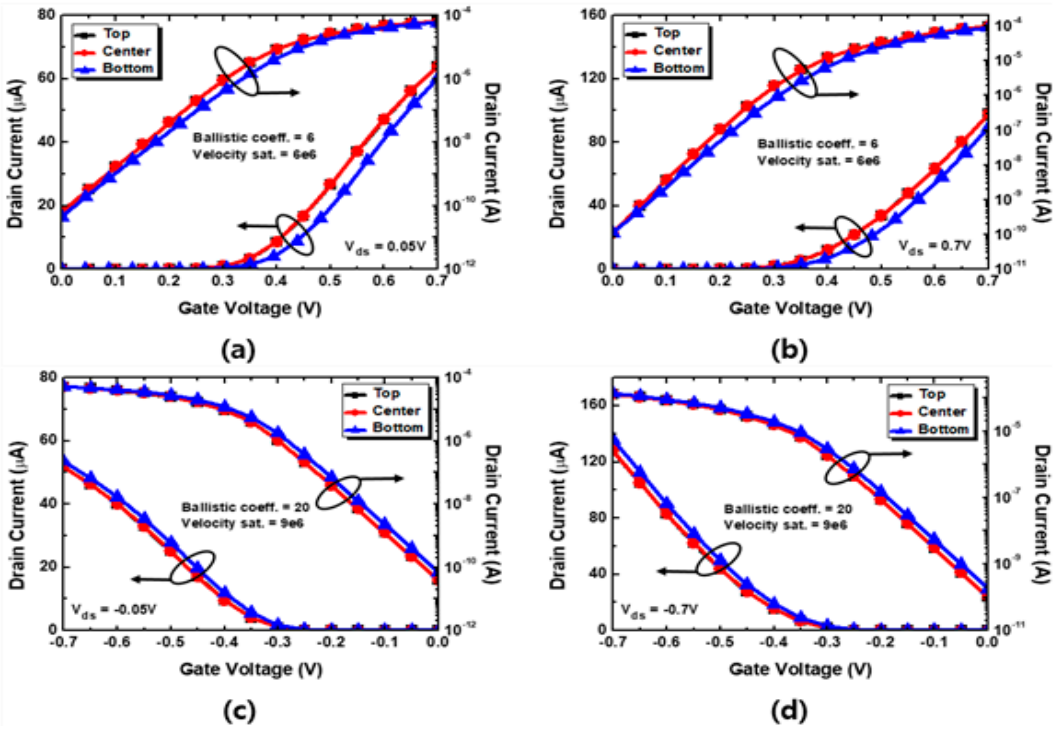

Figure 13. Current–voltage characteristic graph according to bottom oxide positions: (**a**) $V_{ds} = 0.05$ V; (**b**) $V_{ds} = 0.7$ V; (**c**) $|V_{ds}| = 0.05$ V; (**d**) $|V_{ds}| = 0.7$ V.

In Table 6, specific values for the device characteristics (SS and DIBL) according to the location of the bottom oxide are listed. Then, the method used in the previous study was used, without any modifications, to obtain the device characteristics.

Table 6. Specific values of SS and DIBL.

Type	Structure	SS(mV/dec)	DIBL(mV/V)
NMOS	Top	66.254	43.077
	Center	66.259	43.077
	Bottom	75.065	45.021
PMOS	Top	67.512	33.846
	Center	67.516	33.846
	Bottom	67.635	36.127

From Figure 13 and Table 6, it can be noted that the "Top" and "Center" structures show superior results in SS and DIBL characteristics; in contrast, the "Bottom" structure demonstrates comparatively inferior characteristics. It can be observed that the leakage current component is not well controlled in the "Bottom" structure. Figure 14 shows a characteristic graph for the gate capacitance according to the bottom oxide position. From the results of Figure 6, it was confirmed that the gate capacitance decreases as the proportion of the region where the bottom oxide occupies the source and the drain increases. Similarly, from Figure 14, it can be confirmed that the bottom oxide has the largest gate capacitor value in the "Bottom" structure, which occupies less source and drain.

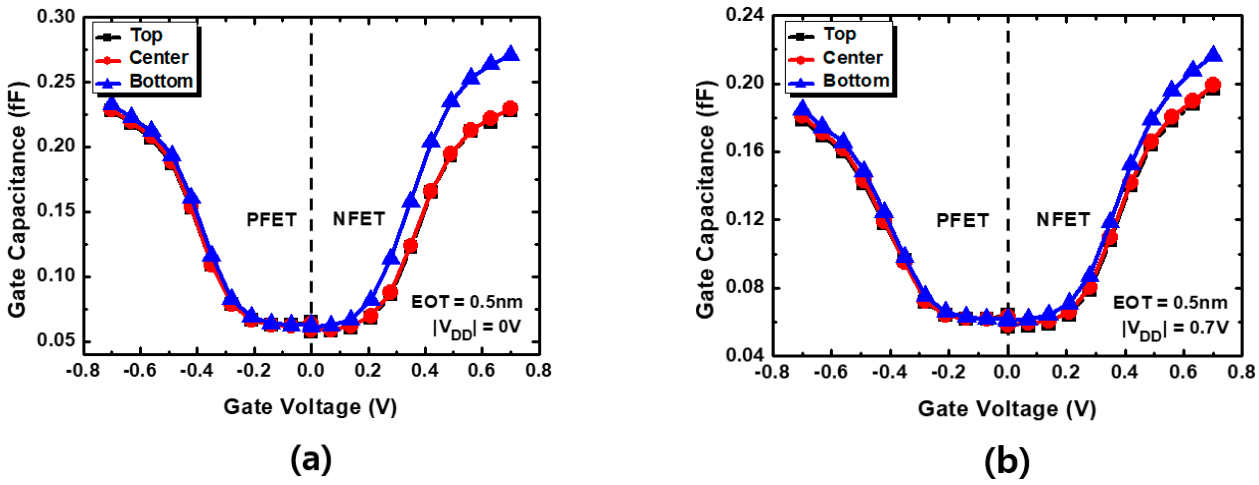

Figure 14. Gate capacitance characteristic graph according to the presence or absence of bottom oxide: (**a**) $|V_{DD}| = 0$ V; (**b**) $|V_{DD}| = 0.7$ V.

3.2. Circuit Characteristic Analysis

As shown in Figure 8, circuit characteristics are analyzed using the same circuit diagram that added the five-stage ring oscillator, fan-out of three, and BEOL loads, which are benchmark circuits. In Figure 15a, the power–frequency graph is drawn when there is no BEOL load, and Figure 15b shows the graph with a BEOL load. When compared to the "Top" and "Center" structures, it can be observed that the characteristics are the worst for a "Bottom" structure. It can be predicted that this is because it has the largest gate capacitance characteristic in terms of device characteristics; consequently, the delay time is long and the resistance component is large; therefore, the power consumption is large.

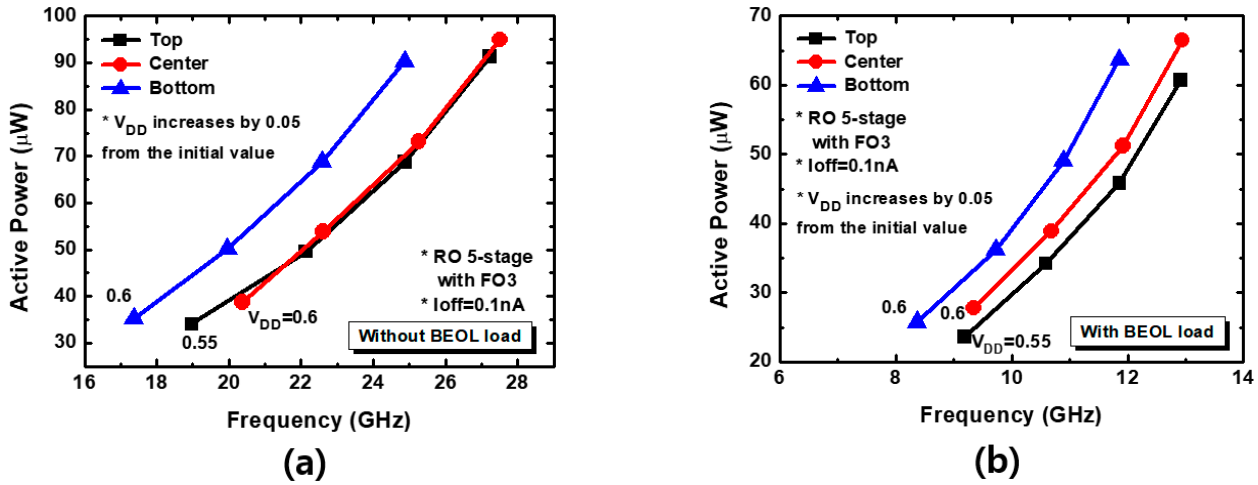

Figure 15. Power–frequency graph according to BEOL load: (**a**) without BEOL load and (**b**) with BEOL load.

In Table 7, the components of the total capacitance are listed according to the location of the bottom oxide. As listed in the table, when the location of the bottom oxide corresponds to the "Bottom" structure, it has the largest total capacitance, which is due to the parasitic capacitor component.

Table 7. Capacitance value according to the position of bottom oxide.

Capacitance Component	Top	Center	Bottom
C_{eff_total} [fF]	1.73	1.74	1.84
C_{load} [fF]	0.57	0.572	0.597
C_{para} [fF]	0.599	0.647	0.737
C_{int} [fF]	0.541	0.503	0.473

In Table 8, the components of the total resistance are listed according to the location of the bottom oxide. It can be observed that the intrinsic resistance component is a factor that determines the value of the total resistance. In this case, it was confirmed that the intrinsic resistance component in the "Bottom" structure has a larger value than the remaining structures. As such, it was possible to prove that the "Bottom" structure shows the worst performance in the power–frequency graph through segmentation of the capacitor and resistance components.

Table 8. Resistance value according to the position of bottom oxide.

Resistance Component	Top	Center	Bottom
R_{eff_total} [kΩ]	4.42	4.85	4.99
R_{load} [kΩ]	1.36	1.38	1.43
R_{cont} [kΩ]	0.313	0.317	0.325
R_{int} [kΩ]	2.75	3.15	3.24

4. Conclusions

In this paper, we analyzed the change in characteristics caused by adding bottom oxide to the mNS-FET device from the perspectives of the device and circuit. Furthermore, the analysis was conducted from these perspectives according to the location of the bottom oxide. First, it is possible to reduce the process cost by using bottom oxide instead of PTS doping. Second, in the comparison according to the presence or absence of bottom oxide, it was confirmed that the SS, DIBL, and gate capacitance characteristics were improved

for the device to which bottom oxide was added, and the leakage current and capacitor components were significantly improved when compared to the conventional device without bottom oxide. Specifically, in the presence of bottom oxide, each 17.6% to 6.3% of the N/PMOS was improved in the SS, and 59.9% to 31.3% was improved in the DIBL characteristics. In addition, circuit characteristics were analyzed by benchmarking circuits with the five-stage ring oscillator, fan-out of three, and BEOL loads for analysis from the perspectives of both the device and the circuit. When compared to the device without bottom oxide, it was confirmed that the device with the same power rate was improved and the power consumption was reduced when the same speed was considered. In addition, through the segmentation of the entire capacitor and resistance components from the perspective of the circuit, it was confirmed that the component was improved owing to the bottom oxide. In the case of capacitor components, by adding bottom oxide, the intrinsic capacitance and parasitic capacitance were significantly decreased by 50.65% and 46.12%, respectively. Correspondingly, the overall capacitor value decreased. In the case of the resistance component, the overall reduction of the resistance component decreased the intrinsic resistance component. Specifically, the intrinsic resistance was decreased by 15%. Third, it was confirmed that the presence of bottom oxide confirmed the improvement in performance from the perspective of the device and circuit, and on comparing the performance according to the location, the worst case of the device and circuit characteristics was observed for the "Bottom" structure when compared to the "Top" and "Center" structures.

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