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A 28 nm CMOS 10 bit 100 MS/s Asynchronous SAR ADC with Low-Power Switching Procedure and Timing-Protection Scheme

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Abstract: This paper presents a 10 bit 100 MS/s asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) without calibration for industrial control system (ICS) applications. Several techniques are adopted in the proposed switching procedure to achieve better linearity, power and area efficiency. A single-side-fixed technique is utilized to reduce the number of capacitors; a parallel split capacitor array in combination with a partially thermometer coded technique can minimize the switching energy, improve speed, and decrease differential non-linearity (DNL). In addition, a compact timing-protection scheme is proposed to ensure the stability of the asynchronous SAR ADC. The proposed ADC is fabricated in a 28 nm CMOS process with an active area of 0.026 mm^2. At 100 MS/s, the ADC achieves a signal-to-noise-and-distortion ratio (SNDR) of 51.54 dB and a spurious free dynamic range (SFDR) of 55.12 dB with the Nyquist input. The measured DNL and integral non-linearity (INL) without calibration are +0.37/−0.44 and +0.48/−0.63 LSB, respectively. The power consumption is 1.1 mW with a supply voltage of 0.9 V, leading to a figure of merit (FoM) of 35.6 fJ/conversion-step.

Keywords: SAR; ADC; high linearity; low power; switching procedure

1. Introduction

In recent years, as a key part of data acquisition and transmission units, ADCs have played an essential role in industrial control system (ICS) and intelligence factory applications, which not only requires low power and compactness, but also cares about the response speed, linearity and reliability [1]. With the CMOS process and supply voltage scaling down, SAR ADCs are well suited for these applications, owing to their low hardware cost and digital-friendly architecture. Importantly, the low latency of SAR ADCs can provide timely feedback for ICS so as to realize an accurate control loop with good transient response [2].

During the last decade, the performance of SAR ADCs was improved prominently by many researchers throughout the world. Seung-Tak Ryu et al. proposed SAR-assisted (SA) SAR ADC that uses a double clock-rate coarse decision technique to enhance the DAC settling speed [3]. Zhichao Tan et al. combined oversampling and mismatch error shaping with redundancy and digital error correction to enable high resolution [4]. Shubin Liu et al. adopted the output offset storage method to improve linearity and the novel switching scheme to obtain power efficiency [5]. Moreover, non-binary search with redundancy solution is often utilized to improve the capacitor digital-to-analog converter (CDAC) settling and reduce reference current [6–10]. From these works, it can be found that reducing the number of capacitors is the foundation of power-efficient SAR ADC design.

However, the less the capacitance, the worse the linearity, unless increments of hardware complexity and power on calibration can be accepted.

In this paper, a power- and area-efficient SAR ADC with high linearity in a 28 nm CMOS process is presented, which requires no calibration. Bottom-plate sampling is used to realize better linearity with little power penalty. In addition, the combination of a partially thermometer-coded and parallel split capacitor array can further optimize DNL. Subsequently, a CDAC switching scheme is proposed to symmetrically realize a constant common-mode voltage, thus avoiding linearity degeneration. The power and area efficiency mainly benefit from the advanced process, low power supply, parallel split capacitor array and single-side-fixed technique. For ICS applications, the reliability and the stability are important, but asynchronous SAR timing logic may collapse, as the comparator is operated in a metastable state. Therefore, a compact and effective timing-protection scheme is proposed to ensure that the asynchronous controller works normally.

The remainder of the paper is organized as follows. The architecture and design concept of the proposed SAR ADC and switching procedure are described in Section 2. The building blocks implementation is shown in Section 3. Section 4 reveals the measurement results. Finally, the drawn conclusions are presented in Section 5.

2. ADC Architecture

2.1. SAR ADC Architecture

In order to have good common-mode noise rejection and achieve high precision, the fully differential architecture is often applied in the ADC. Figure 1 shows the block diagram of the proposed 10 bit SAR ADC mainly composed of the SAR control logic, timing-protection scheme, dynamic comparator, differential CDAC array, bootstrapped switch and voltage reference circuit.
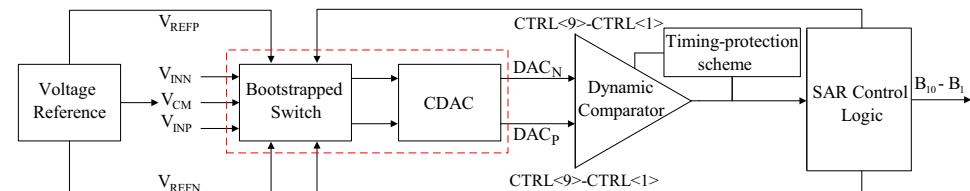

Figure 1. The proposed SAR ADC architecture.

To improve the DNL of the SAR ADC, a segmented CDAC array with parallel split capacitor is adopted by the ADC. Figure 2 shows the architecture of the bootstrapped switch and CDAC array in detail. All capacitors and switches are split into two equal parts, except capacitors C_2 and C_1. For clarity, S_{P3P}, representing the switch connected to $1/2C_3$, is set to V_{REFP} in the DAC_P side during the holding period. In addition, the first 4 bits are achieved by the thermometer coding in MSB array with 15 capacitor of C_6, while the remaining 6b-LSBs are binary coded in LSB array. As the single-side-fixed technique is applied, the proposed CDAC array has a 512 unit capacitor, less than the conventional 10 bit V_{CM}-based SAR ADC with a 1024 unit capacitor [11]. What is more, most of the capacitors are only switched to V_{REFP}/V_{REFN} in the conversion process, which decreases the switching energy and realizes a constant V_{CM}. To expedite the conversion time, asynchronous control logic is utilized in the ADC. Meanwhile, a potential problem in the asynchronous logic must be considered. When the comparator is in a metastable state, the timing collapse will occur in the ADC. Therefore, a timing-protection scheme is proposed to ensure the stability of the time.

The CDAC array is controlled by true single phase clock (TSPC) logic. Compared with traditional static CMOS logic, TSPC logic consumes low power and operates at a high speed with a smaller number of transistors. Unfortunately, TSPC logic has poor anti-noise ability, due to charge leakage.
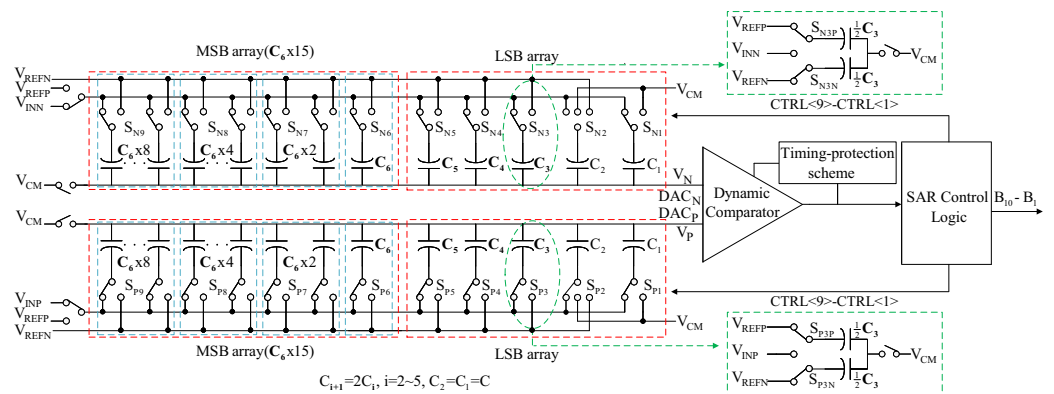
Figure 2. The architecture of the bootstrapped switch and CDAC array in detail.

2.2. Switching Procedure

To improve the conversion speed and decrease power, a partially thermometer-coded CDAC with a parallel split capacitor switching scheme is presented. The flow chart of the proposed switching procedure is shown in Figure 3. During the sampling period, the top plates of all capacitors are connected to the common-mode voltage V_{CM} through bootstrapped switches. In the meantime, to obtain good linearity, the input signal is sampled on the bottom plate of the capacitor when all switches are set to V_{INP}/V_{INN}. During the holding period, the top plates are disconnected from V_{CM}. In addition, S_{P2}, S_{P1}, S_{N2}, and S_{N1} are switched to V_{CM} on the bottom plate, while S_{P9P} to S_{P3P} and S_{N9P} to S_{N3P} are switched to V_{REFP}, and other parallel ones are switched to V_{REFN}. As $V_{CM} = (V_{REFP} + V_{REFN})/2$, all capacitors are connected to V_{CM}. When the conversion starts, the first comparison is carried out directly by the dynamic comparator without switching any capacitor. Next, the most significant bit (MSB) B_{10} is determined via the comparative result. In the advance node, the partially thermometer-coded structure can obtain good trade-off between additional decoder and power consumption versus achieved linearity improvement [12]. Therefore, thermometer coding is adopted in the MSB array, and the number of capacitors C_6 which need to be operated is 8/4/2/1 on the DAC_P/DAC_N side, respectively. As an example, if $V_P > V_N$ ($B_{10} = 1$), there are 8 capacitor of C_6 selected to operate. S_{P9P} is switched to V_{REFN}, and the S_{P8N} switched to V_{REFN} is kept unchanged on the DAC_P side. Then, 2nd-MSB B_9 is obtained after comparing V_P and V_N. The ADC repeats the process until the first eight bits ($B_{10}{\sim}B_3$) are obtained. In particular, there is a unit capacitor in the capacitor C_2. If $B_3 = 1$, S_{P2} and S_{N2} connecting the capacitor C_2 are switched from V_{CM} to V_{REFN} and V_{REFP}.

Moreover, a single-side-fixed technique is utilized to reduce the number of capacitors. The conventional MCS switching procedure has the unswitched dummy capacitor in the last conversion step [13], while the proposed one takes full advantage of the capacitor. For the dummy capacitor C_1, only S_{P1} on the DAC_P side is switched, and S_{N1} is fixed to V_{CM} as usual. At the same resolution, the number of unit capacitors using the single-side-fixed technique is half of that using the MCS switching procedure. Then, the least significant bit (LSB) B_1 is achieved by the last comparison.
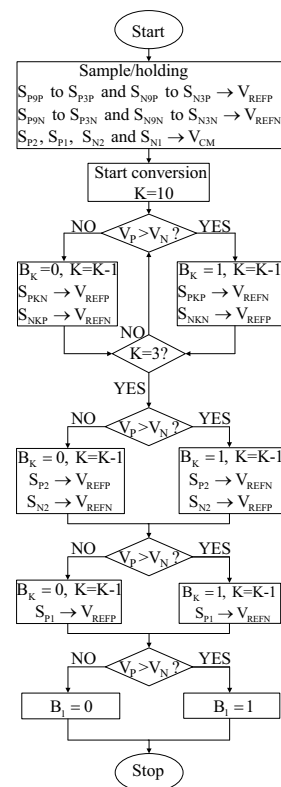
Figure 3. The flow chart of the proposed switching procedure.

3. Building Blocks Implementation

3.1. SAR Control Logic

In this paper, an asynchronous control logic is applied to optimize the conversion time. Figure 4 shows a timing diagram of the asynchronous control logic involved in first two comparison. Next, the comparison process is controlled by the asynchronous logic, which is discussed in detail. *Clks* is the control signal of the sampling and holding processes. $CTR < 9 >$ and $CTR < 8 >$ are control signals of the CDAC array. Q/QN and *Valid* are the complementary output and the comparison complete signal of the dynamic comparator, respectively. *Clkc* is to control per comparison. Though there is no synchronous clock, the conversion still has a strict sequence. If conversion starts, the first comparison is carried out directly. When *Clkc* goes high, the comparator begins to operate until a valid result is obtained, followed by output latch. At the same time, the *Valid* signal is generated by the comparator and digital circuits, and then the CDAC array begins to be switched when $CTR < 9 >$ goes high. The ADC starts the next comparison until the settling of the CDAC array. Moreover, the *Valid* signal can be generated in advance to the regeneration process, which is also beneficial for improving the conversion speed of the ADC.

3.2. Timing-Protection Scheme

A timing-protection circuit is presented to ensure that the conversion process has a strict sequence in the asynchronous logic. As the comparator is operated in a metastable state, the results cannot be obtained during the preset time. It is not a serious potential problem in synchronous logic [14], but the timing logic may collapse in asynchronous SAR ADC. A compact and reliable method is to adopt the proposed circuit. Figure 5 shows the schematic and timing diagram of the timing-protection circuit mainly composed of a NAND gate, which has the delay time τ_{NAND}, delay circuit and NOR gate. The timing protection module is mainly composed of digital logic circuits, so it is not much affected by PVT. To ensure that the asynchronous ADC continues to work normally, the delay time τ_{delay} is slightly less than the maximum comparator decision time τ_{comp} that the ADC can tolerate. In the reset phase of the comparator when the Clkc is low, the outputs Q/QN are

charged to the positive supply (AVDD). Therefore, the output *Valid*1 of the NAND gate is logic 0. *Valid/Valid*2 is the comparison complete signal and delay signal generated by clock *Clkc*, respectively. Next, the comparator enters the operating state when the *Clkc* is high. When the input voltage difference $|V_p - Vn|$ is far greater than LSB in the comparator, the circuit completes the comparison quickly and $\tau_{comp} + \tau_{NAND} < \tau_{delay}$. Meanwhile, the output *Valid*1 of the NAND gate and the comparison complete signal *Valid* are changed to logic 1. When $|V_p - V_n| \approx 0$, the comparator is operated in a metastable state and $\tau_{comp} + \tau_{NAND} > \tau_{delay}$. *Valid*2 is changed to logic 1, and the output *Valid*1 of the NAND gate still keeps logic 0 due to the unfinished comparison. Next, the comparison completes the signal and *Valid* is changed to logic 1. To ensure that the asynchronous controller works normally, the output logic level of the comparator is changed to logic 0/1 with a pseudo-random PN code circuit. Since the analog input signal is quantified to the LSB, the output logic level (logic 0 or logic 1) of the comparator does not affect the final quantization result.
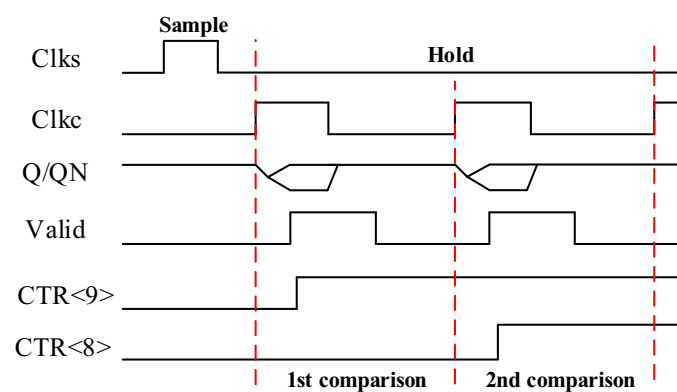

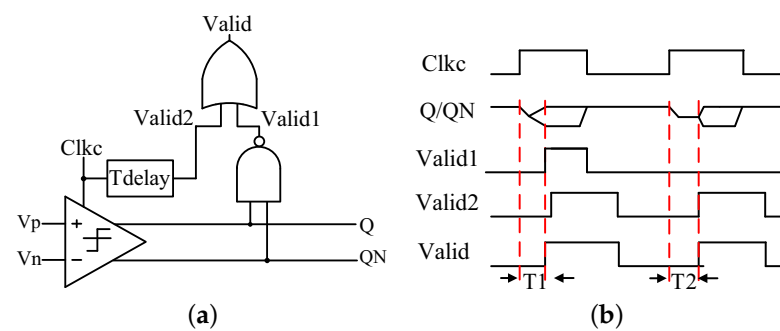**Figure 4.** The timing diagram of the asynchronous control logic involved in first two comparisons.

(a)   **(b)**

Figure 5. The schematic and timing diagram of the timing-protection circuit. (**a**) Schematic. (**b**) Timing diagram.

3.3. Dynamic Comparator

To eliminate kick-back noise and improve the comparison speed, a pre-amplifier is adopted as its first stage, followed by a regenerative latch. The schematic of the high-speed dynamic comparator is shown in Figure 6. As a trade-off, the comparator has higher static power dissipation than most of counterparts without a pre-amplifier [15]. This overhead is affordable, as the power is relatively small at 0.9 V supply. In the reset phase when the *Clkc* is low, the outputs *Q/QN* are charged to the positive supply (AVDD). Next, the comparator enters the regeneration state when *Clkc* goes high. The positive feedback latch composed of M5, M6, M7, and M8 starts to operate, pulling one of the outputs low.
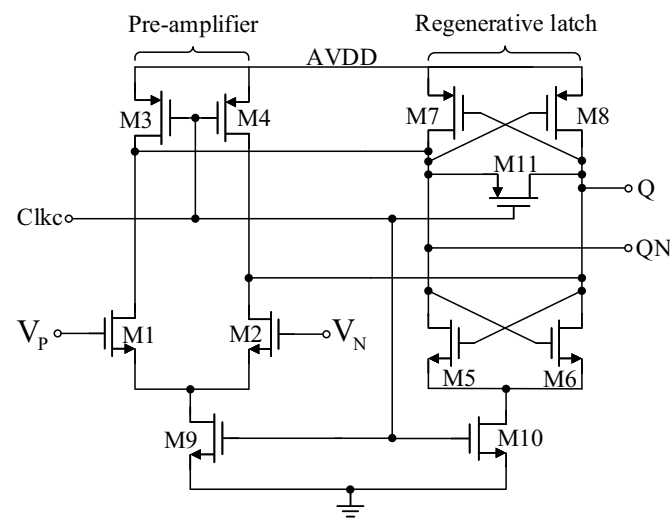
Figure 6. Dynamic comparator schematic.

3.4. Differential CDAC Array

To implement the area-efficient CDAC array with low parasitic capacitance, five-layer low-cost metal-oxide-metal (MOM) finger capacitors are applied in this paper. To minimize the DNL error caused by CDAC array mismatch, the design of the layout is also important. Figure 7 shows the layout of the differential CDAC array. Both plates of the capacitor array are mutually crosswise arranged to meet the overall matching requirement. Meanwhile, each bottom plate is surrounded by the corresponding top plate, as both plates are connected to the reference voltage and input ports of the dynamic comparator, respectively. For the unused capacitors in the CDAC array, they are all connected to a low impedance node to improve the matching.
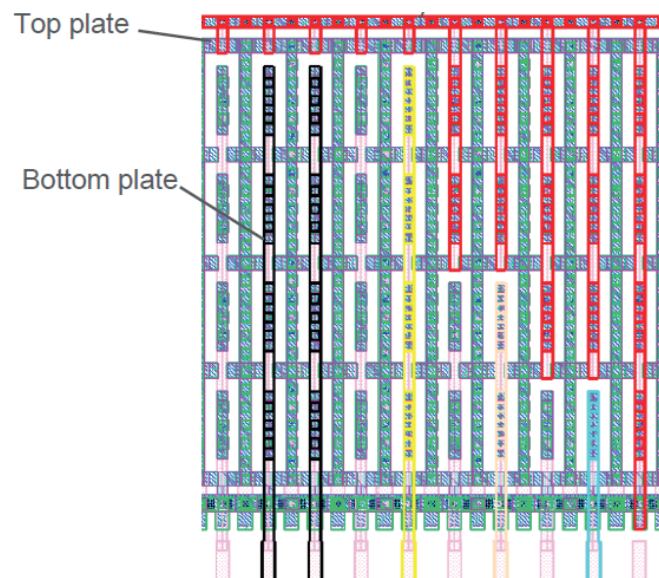

Figure 7. The layout of the differential CDAC array.

4. Measurement Results

The proposed SAR ADC is designed and fabricated in a 28 nm CMOS process. Figure 8 shows the die photo, and the total active area is 200 μm × 130 μm, including the input buffer (0.0028 mm^2) and the voltage reference circuit (0.0065 mm^2). To guarantee the performance of the bias voltage in sub 1 V power supply, the area of the reference has to

be increased slightly. However, benefiting from the advanced process, some areas can be saved, especially in digital circuits.
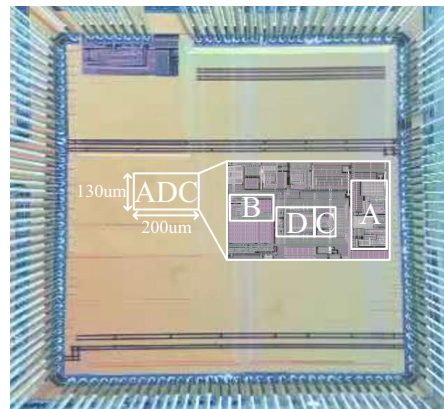

Figure 8. Die photograph. (A) Voltage reference circuit. (B) Input buffer. (C) Dynamic comparator and timing-protection circuit. (D) CDAC array.

Figure 9a,b shows the schematic diagram of the test platform and the chip test board. To obtain clean ADC input signals, a test signal generated by high-precision arbitrary signal generator passes the corresponding bandpass filter. The bandpass filter in which the center frequency is set at a specific frequency has a 3 dB bandwidth of 100 KHz and a stopband rejection of 60 dBc. All results are measured at room temperature. At 100 MS/s, the total power consumption is 1.1 mW with 0.9 V supply voltage, where the voltage reference and the input buffer account for 60% (0.66 mW), and the power consumption of the ADC core is only 0.44 mW.

The FFT spectrum with 1 MHz input at 100 MS/s is shown in Figure 10. The proposed SAR ADC achieves a SNDR of 55.13 dB and SFDR of 61.92 dB; thus, the effective number of bits (ENOB) is 8.86 bits.
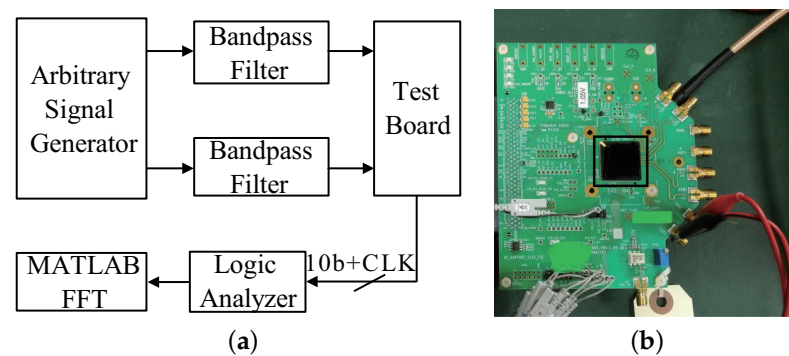

Figure 9. The test platform. (**a**) Schematic. (**b**) Chip test board.

The ENOB of the proposed ADC at −40/27/125 °C and 0.8/0.9/1.0 V supply voltage are post-layout simulated as summarized in Table 1 with five different corners (tt, ff, ss, fnsp, snfp) and 1 MHz input. It can be found that the best ENOB is 9.52 bits at 27 °C and 0.9 V supply voltage under the ff corner, and the worst ENOB is 9.06 bits at −40 °C and 0.8 V supply voltage under the ss corner. Therefore, the ENOB is not much affected by PVT. Figure 11 shows the SFDR and SNDR of the proposed ADC with respect to the input frequency. The SNDR is 51.54 dB and SFDR is 55.12 dB at the Nyquist input, and the ENOB is 8.27 bits. In addition, the *FOM* is 35.6 fJ/conversion-step at the input, defined in (1):

$$FOM = Power/(2^{ENOB} \cdot f_s) \tag{1}$$

where Power and fs are the power consumption and sampling frequency of the SAR ADC, respectively. The main reason for SNDR and SFDR degradation at high input frequency is that a low power supply has more serious influence on the settling of the S/H operation. It is known that bad linearity leads to missing code, which is not accepted in ICS applications.
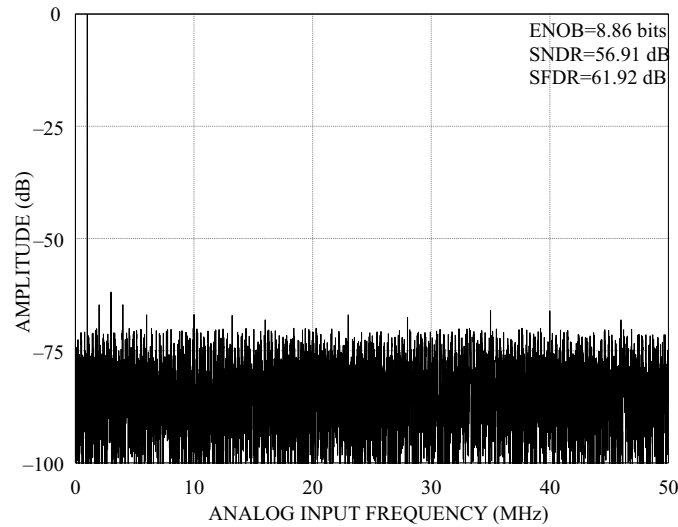

Figure 10. Measured ADC spectrum with 1 MHz input at 100 MS/s.

Figure 12 illustrates that the peak DNL and INL are $+0.37/-0.44$ and $+0.48/-0.63$ LSB, proving that the proposed SAR ADC can achieve good linearity without calibration.
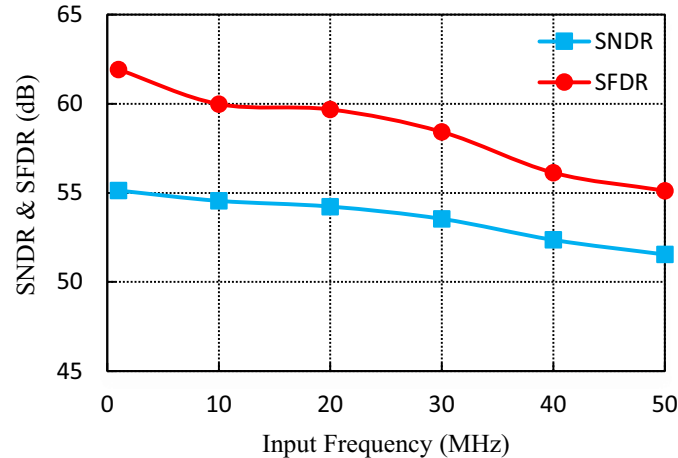

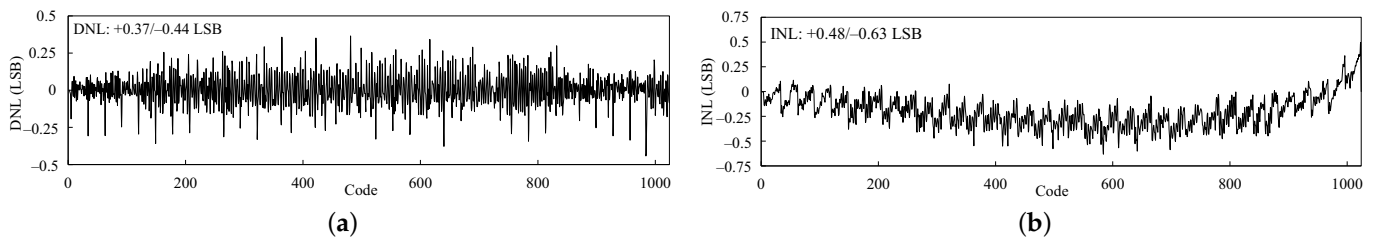**Figure 11.** Measured SFDR and SNDR with respect to the input frequency at 100 MS/s.

Figure 12. Measured DNL and INL at 100 MS/s. (**a**) DNL. (**b**) INL.

Table 1. Post-layout simulation of ENOB of the ADC with process, voltage, temperature (pvt) variations.

Temperature (°C)	Corners	ENOB(bit)@0.8V	ENOB(bit)@0.9V	ENOB(bit)@1.0V
−40	tt	9.09	9.27	9.17
	ff	9.19	9.39	9.32
	ss	9.06	9.16	9.09
	fnsp	9.16	9.35	9.25
	snfp	9.08	9.22	9.14
27	tt	9.24	9.43	9.33
	ff	9.39	9.52	9.48
	ss	9.18	9.32	9.26
	fnsp	9.34	9.47	9.4
	snfp	9.19	9.36	9.31
125	tt	9.15	9.29	9.21
	ff	9.26	9.41	9.33
	ss	9.05	9.21	9.14
	fnsp	9.2	9.35	9.25
	snfp	9.12	9.26	9.16

The performance summary of the proposed ADC and recent SAR ADCs in sub 100 nm technologies is given in Table 2. Although the reference generator consumes much power and area, this work achieves competitive power and area efficiency. Meanwhile, the linearity of the ADC is also good, even better than [3] with calibration. However, owing to operating at a low supply voltage, there is a little sacrifice of SNDR at a high frequency input.

Table 2. Performance summary and comparison of SAR ADCs.

	[16] TCAS-II 2020	[3] TCAS-II 2020	[17] JSSC 2019	[18] ASICON 2019	This Work
Architecture	SAR	SAR	Pipe-SAR	SAR	SAR
Process (nm)	65	40	28	28	28
Supply (V)	1.2	1	1	1.05	0.9
Fs (MS/s)	350	120	500	250	100
Resolution (bit)	8	12	10	10	10
SNDR@Nyq. (dB)	45.7	58.1	56.6	52.4	51.54
ENOB (bit)	7.3	9.36	9.1	8.4	8.27
Power (mW)	2.1 *	1.9	6	3.23	1.1 *
FOM (fJ/c-s)	38.1	24.1	21.8	38.2	35.6
DNL (LSB)	+0.9/−0.6	+0.96/−0.93 [†]	+0.48/−0.32 [†]	+0.96/−0.86	**+0.37/−0.44**
INL (LSB)	+0.7/−0.7	+1.6/−1.08 [†]	+0.67/−0.61 [†]	+1.37/−1.02	**+0.48/−0.63**

* The total power consumption, including voltage reference circuit. [†] The measured DNL and INL after calibration.

5. Conclusions

In this paper, a 28 nm 0.9 V low-power SAR ADC with good linearity is presented. With the combination of partially thermometer-coded and parallel split capacitor, the linearity and power efficiency can be improved. Additionally, a compact timing protection scheme is proposed to enhance the stability. At a 0.9 V supply and 100 MS/s, the proposed SAR ADC has a power consumption of 1.1 mW with an active area of 0.026 mm^2. The maximum DNL and INL are 0.44 LSB and 0.63 LSB without calibration, respectively. The measured results prove that the proposed ADC is suitable for ICS applications.

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