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Design, Application, and Verification of the Novel SEU Tolerant Abacus-Type Layouts

Yi Sun [1,†], Zhi Li [2,†], Ze He [3] and Yaqing Chi [4,*]

[1] China Aerospace Components Engineering Center, China Academy of Space Technology, Beijing 100028, China; zoesun99@126.com
[2] Beijing Institute of Control Engineering, China Academy of Space Technology, Beijing 100190, China; coollizhi@126.com or impcas@163.com
[3] Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China; heze@impcas.ac.cn
[4] College of Computer, National University of Defense Technology, Changsha 410000, China
* Correspondence: yqchi@nudt.edu.cn
† Yi Sun and Zhi Li have contributed equally to this work and should be considered co-first authors.

Abstract: Radiation tolerance improvements for advanced technologies have attracted considerable interests in space application. In this paper, the single event upset (SEU) hardened double interlocked storage cell (DICE) D-type flip-flops (DFFs) with abacus-type time-delay cell are proposed and successfully implemented in our test chips. The layout structures of two kinds of abacus-type time-delay cells are illustrated, and their hardening effectiveness are verified by our simulations and heavy ion irradiations. The systematic heavy ion experimental results show that the applied abacus-type time-delay cells can reduce the SEU cross sections of DICE DFFs significantly, and even the SEU immune is observed for the full "0" data pattern. Besides, an apparent test mode dependency of the abacus-type hardened circuits is also observed. The results indicate that the nanoscale abacus structure may be suitable for space application in harsh radiation environment.

Keywords: D flip-flop; double interlocked storage cell; single event upset

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1. Introduction

The implementation of digital circuits and systems using advanced nanoscale technologies is beneficial to achieve higher density, higher performance, and less power consumption than submicron techniques [1–6]. However, the integrated nanoscale circuits are more susceptible to single event effects due to their reduced critical charges and serious charge sharing in adjacent nodes [3,5–8]. The conventional complementary metal oxide semiconductor (CMOS) circuits applied in nanoscale technologies experience weak radiation tolerance that may put advanced electronic systems in danger [2–10]. To overcome this problem, a few reliable and radiation-hardened units are proposed to protect the nanoscale CMOS circuits in the radiation environments [11–32]. However, the traditional circuit-level and system-level redundancies are not optimistic when being implemented to the nanoscale bulk planar technologies to achieve single event upset (SEU) robustness [2,9–14]. For examples, the Quatro 10 T, Quatro 12 T, 14 T, 18 T, and double interlocked storage cell (DICE) structures seem acceptable for their high critical charges of an upset induced by their multiple redundant nodes, while the level of improvements are not dramatic, and even a tendency of continuously decrease of their SEU thresholds with the shrinking of technologies are clearly characterized by recent work, indicating that merely implementing the SEU tolerance units to replace standard cells seems not enough [13–24]. Therefore, for the nanoscale high-integrated circuits, the effective hardening strategies concerning both the units and peripheral circuits are urgently needed to further improve the SEU tolerance of the existing circuits to satisfy the mission-oriented radiation tolerance. In addition, some of the related work with the proposal of hardened units and re-examination of simulation

data may not be enough to support their future space application, since the actual procedure of ionizations, charge propagations, and impact ranges should be fully evaluated rather than merely based on the circuit-level simulation results [14–20]. Hence, detailed high-linear energy transfer (LET) heavy ion irradiation experiments are also necessary to investigate the SEU mechanisms of nanoscale devices and verify the effectiveness of the designed circuits, which are indispensable for the procedure of hardening design.

In this paper, the novel abacus-type time-delay cells are applied to the D-type flip-flops (DFFs) chains to replace the standard time-delay circuits, and all of the specially designed DFF chains are fabricated using an advanced 40 nm planar technology. The proposed abacus-type time-delay cells are aimed at achieving high SEU response robustness. In addition, a series of heavy ion irradiation experiments are carried out to verify the effectiveness of the abacus-type circuits and evaluate their appropriateness for space applications. The rest of the paper is organized as follows: Section 2 of this paper details the designed DFF chains including the layouts with diverse hardness techniques. The irradiation setups are described in Section 3. Section 4 presents the heavy-ion irradiation results and related discussions. Finally, in Section 5, we give the conclusions.

2. Circuits Design

The test chip contains three DFF chains including a standard DICE DFF chain without time-delay cells, a DICE DFF chain with Abacus-C time-delay cells, and a DICE DFF chain with Abacus-R time-delay cells. The capacity of each DFF chain is 4000 bits. The DICE structures are widely used in DFF designs for its high soft error tolerance. Thus, the DICE hardened DFFs implemented in our designed test chip are used to reduce the SEU sensitivity of the body of DFF and highlight the influence of the different time-delay cells. The diagram of the DICE DFF with the time-delay cell is given in Figure 1. The general layout structure of the time-delay cell consists of even inverters, which layout is shown in Figure 2. In our work, two novel abacus-type time-delay cells Abacus-C and Abacus-R are proposed and employed into the DICE DFF chains to further reduce the SEU cross sections of the DICE DFFs. The basic Abacus-type inverters used in the time-delay cells are shown in Figure 3, and the well and substrate contacts are also implemented. Then, the 3D mixed-mode based on the TCAD tools are performed to investigate the SEU sensitivity of abacus structure. The drain current-gate voltage (I_d-V_g) curves for both PMOS and NMOS in the inverter are calibrated with the I-V data from the commercial 40 nm process design kits. In addition, all of the simulations are performed for normal incidence with nominal supply voltages (V_{dd} = 1.1 V). The charge tracks are generated by a heavy-ion Gaussian charge distribution model under the condition of LET = 100 MeV·cm^2/mg. The pulse width is LET dependent, and the high LET (100 MeV·cm^2/mg) is used to help us to decide the delay time of circuits to achieve a high radiation tolerance. The 50 nm track radius and 0.5 ps rise time are employed in pulse width simulations, according to the actual characteristics of ions. The simulation results for the standard cell and abacus cell with and without the well and substrate contacts are shown in Figure 4. The obvious mitigation of pulse width of the 40 nm transistors can be found based on the comparisons of TCAD simulation results. Hence, we applied the abacus-hardened structure presented in Figure 3 into the time-delay module of the DFF cells.

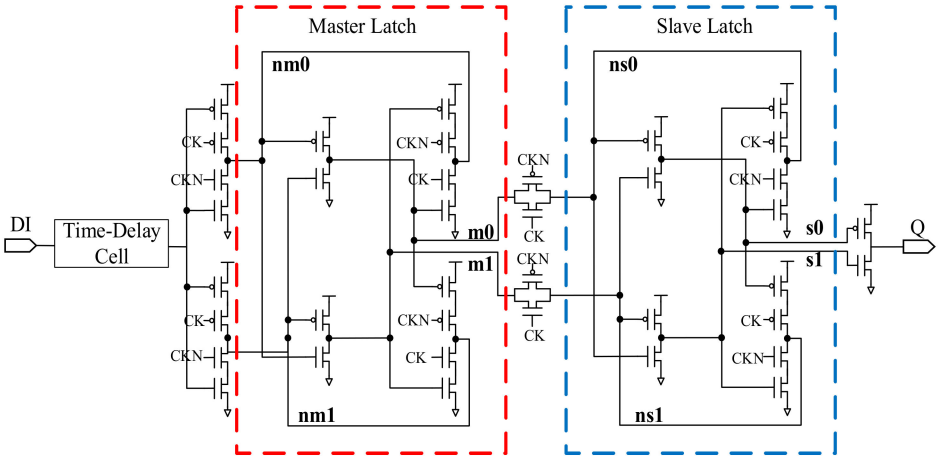

Figure 1. Basic structure of the DICE DFF.

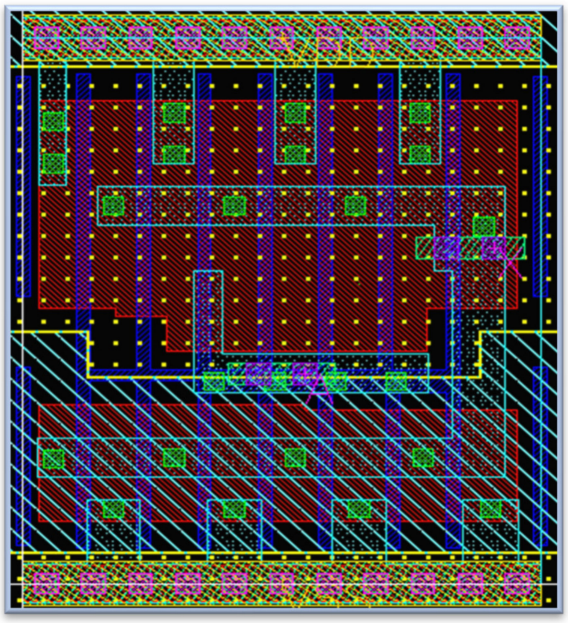

Figure 2. The general layout of the inverters of the time-delay cell.

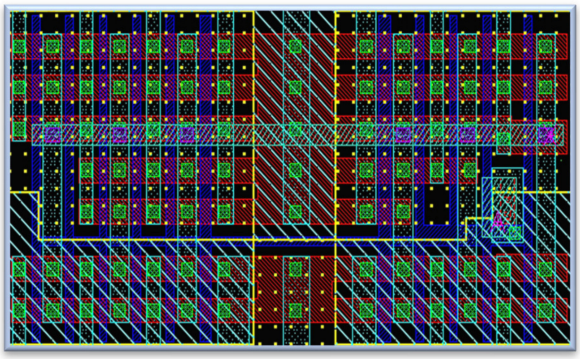

Figure 3. The layout of abacus-type inverters of the time-delay cell.

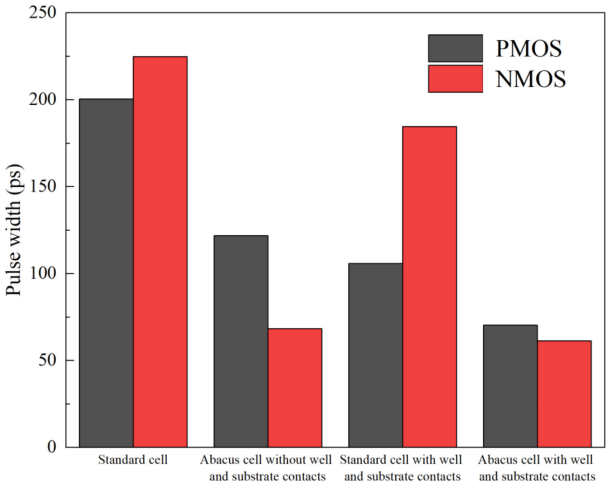

Figure 4. Pulse width simulations for the unhardened and abacus-hardened PMOS and NMOS (*LET* = 100 MeV·cm^2/mg, V_{dd} = 1.1 V).

Compared with the basic time-delay cells, the abacus-type time-delay cells have benefits for both the stability of circuits and mitigation of ions induced single event transients in time-delay circuits. The Abacus-C time-delay cell consists of cascaded six inverters (four inverters at the two ends are used to drive the signals, and the two inverters with large gate area in the middle are used to improve the capacitance of the circuit nodes to get the signal delay), where the size of the gates in the middle two common inverters are six times than in the four Abacus-type inverters of the both ends as Figure 5 shows, which realizes large capacitors and increase the delay time. The channel length (L) for the NMOS and PMOS transistors of the four Abacus-type inverters in Abacus-C cell is 40 nm. The Abacus-R time-delay cell consists of cascaded two inverters, a 26 k Ohm resistance, and other two inverters as Figure 6 shows. It utilized the inverter (INV)-26 k Ohm resistance (R)-INV structure. The 26 k Ohm resistance is made of two cascaded gate blocks with 8 μm-length and 0.4 μm-width for each block in our design. The L of the transistors employed in the Abacus-R cell is 40 nm. The determination for the value of R of Abacus-R and the structure of Abacus-C is based on the circuit-level simulation results by SPICE tools. It is investigated that the delay module of Abacus-R and Abacus-C is around 240 ps, which is on the basis of the pulse width induced by the transient in an inverter of 40 nm technology. Both the extra resistances and capacitors are very useful to reduce the radiation induced transients and increase the critical charges for the upset of the circuits. Thus, the SEU cross sections for our abacus circuits ought to be decreased, because of the mitigated transients and effective isolations between sensitive transistors.

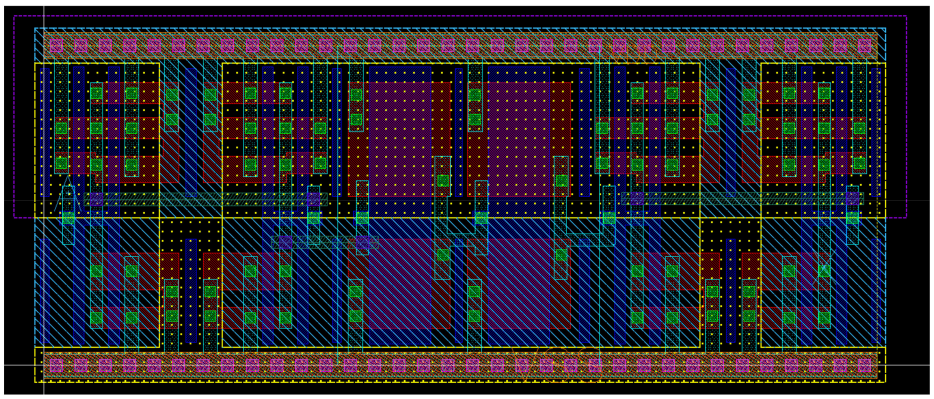

Figure 5. The layout of the proposed Abacus-C time-delay cell.

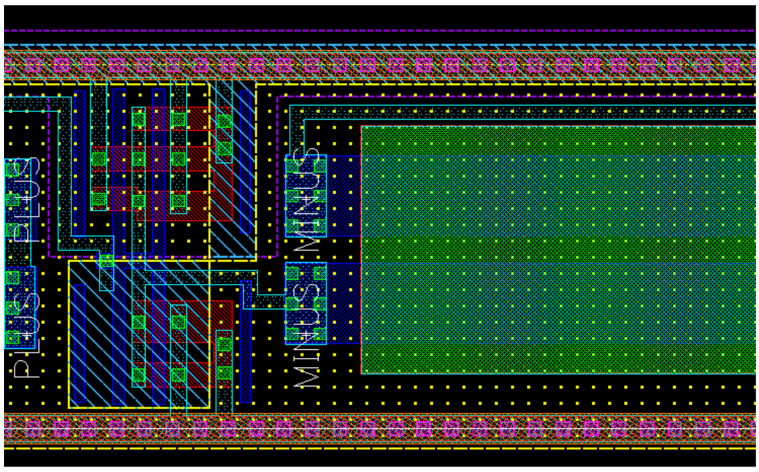

Figure 6. The left part of the layout of the proposed Abacus-R time-delay cell.

For our test chip, the data input, output, and clock ports are included in each DFF chain. The clock signals are set to one during the static irradiation test, while the clock signals continuously change at 40 MHz during the dynamic test. All the DFF cells are fabricated based on the advanced 40 nm planar technology with high-k gate dielectric. Besides, the isolation of the transistors is realized by the shallow trench isolation (STI) technique.

3. Experimental Setup

The test system with independent daughterboard and motherboard is presented in Figure 7. The full "1" and full "0" data patterns are used in the experiments, and all of the test modes are realized by a controllable readback frequency with error information presenting in a real time.

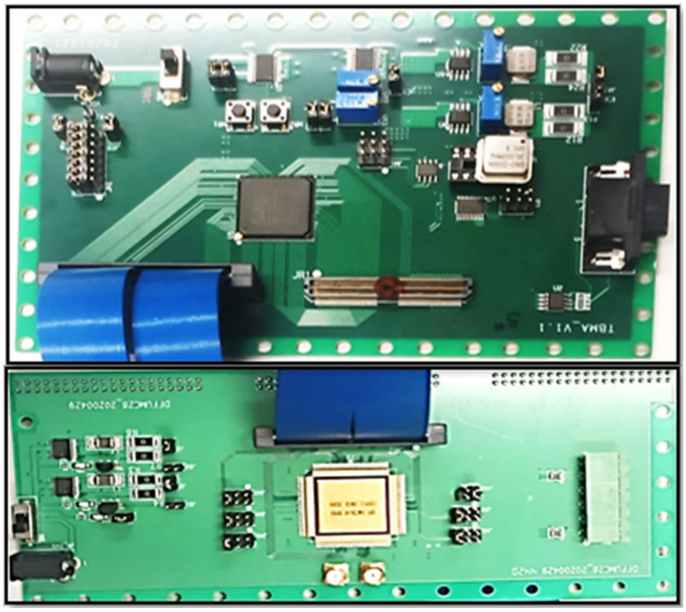

Figure 7. The designed SEU test system for DFF chip.

The heavy ion irradiation tests are conducted at Heavy Ion Research Facility in Lanzhou (HIRFL), in the Institute of Modern Physics, Chinese Academy of Sciences. At HIRFL, the air layer is used as energy degraders to adjust beam energy, and the tests are carried out in air with the flux of incident ions controlled at 10^4 ions·cm^{-2}·s^{-1}. The ^{181}Ta ions are used in our irradiation test due to their high ionization ability, and the detailed parameters of each ion are shown in Table 1. Besides, the 0° to 45° variations of tilt angle (θ)

are also performed to verify the actual radiation tolerance of the novel abacus-type modules. In tilt-angle irradiation, the X-direction (along-cell irradiation) and Y-direction (cross-cell irradiation) are also classified. Thus, the effective LET values can be calculated by:

$$LET_{eff} = \frac{LET_0}{\cos X \cos Y} \quad (1)$$

where the LET_{eff} means the effective LET for the ions at an angle of θ (X°, Y°), and the LET_0 denotes the initial LET of the incident ^{181}Ta at the surface of the sensitive regions.

Table 1. The parameters of ^{181}Ta ions and irradiation conditions.

Energies (MeV)	Ranges (μm)	Tilt (°)	Effective LET (MeV·cm^2/mg)	Modes
1695.3	99.2	(0, 0)	78.3	Dynamic
1695.3	99.2	(0, 0)	78.3	Static
1623.8	95.3	(0, 45)	111.7	Static
1623.8	95.3	(45, 45)	158.0	Static
1668.8	97.8	(30, 0)	90.8	Static

Due to the rotation of incident angles, a coefficient for the effective fluence (F_{eff}) of ions in sensitive regions is required for the tilt incidence, which is related to the beam fluences (F) counted by detectors.

$$F_{eff} = F \cos X \cos Y \quad (2)$$

where the F_{eff} represents the effective fluence, and the F indicates the beam fluences counted by detector.

4. Irradiation Results and Analysis

The SEU cross sections (σ) is calculated by the formula:

$$\sigma = \frac{\sum_j j \times N_j}{F \times N \times \cos X \times \cos Y} \; j = 1, 2, 3, \ldots \quad (3)$$

where the N_j is the number of multiple event upsets (MEU) involving j-bit errors, and N is the total bits of each DFF chain. In our experiments, no multiple event upset (MEU) is observed, because the interval of DFFs is around 18 μm, which is so far that the deposited charges cannot cover two or more DFF cells to induce the MEU.

The SEU cross-sections for different data patterns and test modes are characterized, and the evaluation results are shown in Figure 8. The downward-pointing arrows are used to mark the limited value of no SEU event. Based on the heavy ion irradiation results, it is found that the dramatic improvements for the SEU tolerance of both the Abacus-R and Abacus-C chains are investigated, when compared with the standard DICE hardened DFFs. An obvious SEU dependence on data patterns is clearly observed. Besides, for the dynamic mode, the SEU cross sections of full "1" data present one order of magnitude higher than the SEU cross sections of full "0" data, and for the static mode, an SEU immune is measured for the full "0" data of the abacus hardened circuits. It is indicated that the influence of peripheral circuits on upset occurrence can lead the discrepancy of SEU cross sections between the static mode and dynamic mode. In dynamic mode, the SEU cross section results are higher than that in static conditions due to the additional impacts of the transients in peripheral circuits. The circuits are susceptible to both the reset and clock signals in dynamic test, leading to the substantial increase of SEU cross sections. Hence, the hardened circuits are suitable to be fully examined in the static with high-LET ions irradiation. It is because that, during the static mode, data are stored before the irradiation and read out after the irradiation, which can exclude some of the impacts of the additional perturbation of transients in peripheral clock ports and reflect the actual extent of SEU

sensitivities. Therefore, for the SEU hardened circuits, the differences of SEU cross sections between the static and dynamic modes are non-negligible.

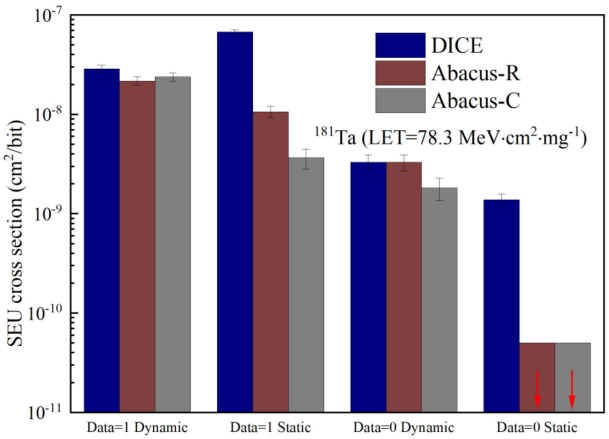

Figure 8. SEU cross section results for different data patterns and test modes.

Besides, for the hardening circuits, the SEU may flip the logic state of a latch but cannot result in an error output of this flip-flop, which depends on the robust of hardening effectiveness and the position of hardening units and presents different tolerance for full "1" or full "0" data patterns. It is determined by the working modes of the slave and master DFF cell, which have different sensitivity-node distributions under different data patterns. Hence, the SEU cross sections of full "1" and full "0" indicate the size of sensitive area and inherent radiation tolerance of slave DFF and master DFF cells. The SPICE simulations are applied to get the SEU sensitivities of all the nodes in the DICE DFFs (Figure 1) by injecting the current pulse into the circuit nodes. The nodes connected to the off-state transistors are possible to upset in radiation environments. The double-exponential current pulses, shown in the following formula, are inserted into the circuit nodes to investigate the circuit responses:

$$I(t) = I_{peak}\left[e^{-\frac{t-t2}{\tau 2}} - e^{-\frac{t-t1}{\tau 1}}\right] \quad (4)$$

where the I_{peak} is the maximum current to be approached, $t1$ indicates the onset time of rise in current, $t2$ indicates the onset time of fall in current, $\tau 1$ is the parameter of rise time, and the $\tau 2$ is the parameter of fall time. The parameters are calibrated by TCAD tools, where the $\tau 1$ and $\tau 2$ are 2 ps and 10 ps, respectively, and the value of $t2 - t1$ is 15 ps. And the simulation results are shown in Table 2. Both the simulation and heavy ion test results show that the nodes of nm0 and nm1 are more sensitive than the m0 and m1 ones. The critical charges of nm0 and nm1 are around 5.2 fC, while the m0 and m1 can keep the data unchanged if the LET values are >100 MeV·cm^2/mg. The upset conditions in Table 2 corresponds to the state of data "1". Therefore, the full "1" data is more likely to upset than the full "0" data for the designed DICE DFFs.

Table 2. Critical Charge of the Sensitive Nodes in the Master Latch of the DICE-DFF.

Node	Striking Position	Critical Charge
nm0 or nm1	off-state PMOS	5.2 fC
nm0 or nm1	off-state NMOS	No Upset
m0 or m1	off-state PMOS	No Upset
m0 or m1	off-state NMOS	No Upset

The occurrence of SEU is determined by the disturbance of ion induced high-density-charge deposition and diffusion in circuits. Since the ^{181}Ta ions used in the irradiation have a high LET value, high-density charges are deposited in circuits and diffused to a long distance under the electric field, and be collected by multiple adjacent transistors,

leading the hardening layouts to lose efficacy. The Monte Carlo simulation using the Geant4 tool is presented to further explain the radial ionization profiles of irradiated ions, as shown in Figure 9. Charge deposition in the active regions of circuits may lead the SEU occurred. While the charge depositions are varying from the radial distances. Thus, it is suitable to calculate the radial ionization profiles of experimental heavy ions by Monte Carlo method with Geant4 toolkit. The energy deposition in the sensitive regions of circuits is different with different radial distance of ions. The average charge densities versus the track radius are calculated and presented in Figure 9, and the mechanisms of the high-LET ^{181}Ta ions induced failures are also illustrated in this figure. If the off-state NMOS and PMOS transistors in DFF cell are regarded as sensitive nodes, the high-density charges cover a large number of sensitive nodes for the 40 nm planar technology, and the impact area can be extended when the tilt-angle incidence is implemented during the irradiation test. Therefore, to make the influence more notable, the tilt irradiations are utilized to further investigate the radiation tolerances and failure rates of the hardened circuits in more serious radiation environments, and the relevant results are given in Figures 10 and 11. For the full "0" data, no upset is measured for all of the irradiation conditions. While for the full "1" data, the increased SEU sensitivities are verified during the tilt conditions, especially for the joint change of tilt angles. It is found that four or more times higher SEU cross-sections for the (45°, 45°) tilt angle are measured when compared with the vertical irradiation. Though the SEU cross sections are affected by the irradiation conditions, i.e., the increased effective LET values in tilt irradiations have significant contributions on SEU cross-sections, the improvements of SEU tolerance for the abacus-hardened circuits are still significant.

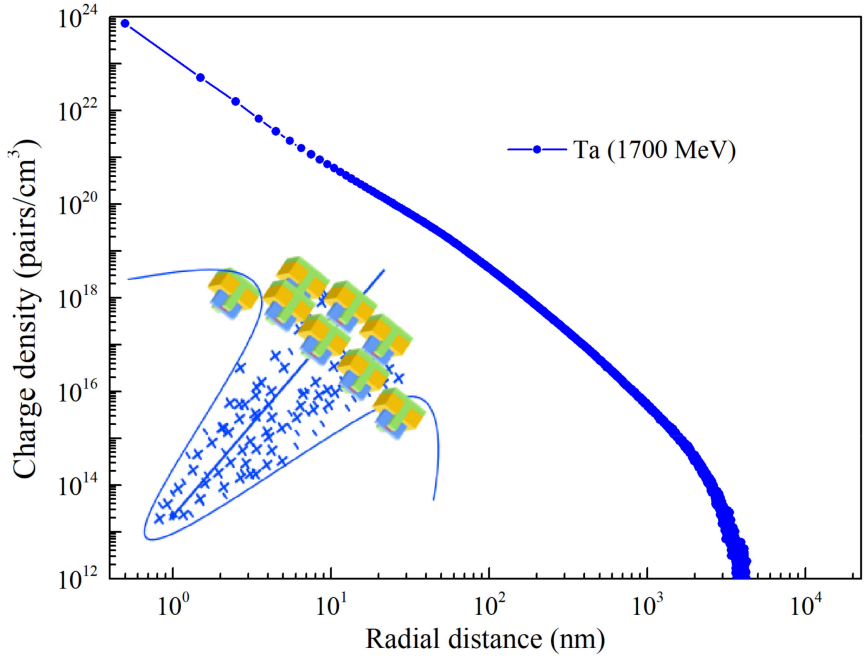

Figure 9. The concentration of electron-hole pairs in device generated by the ionization of ^{181}Ta ions vs. the radial distance.

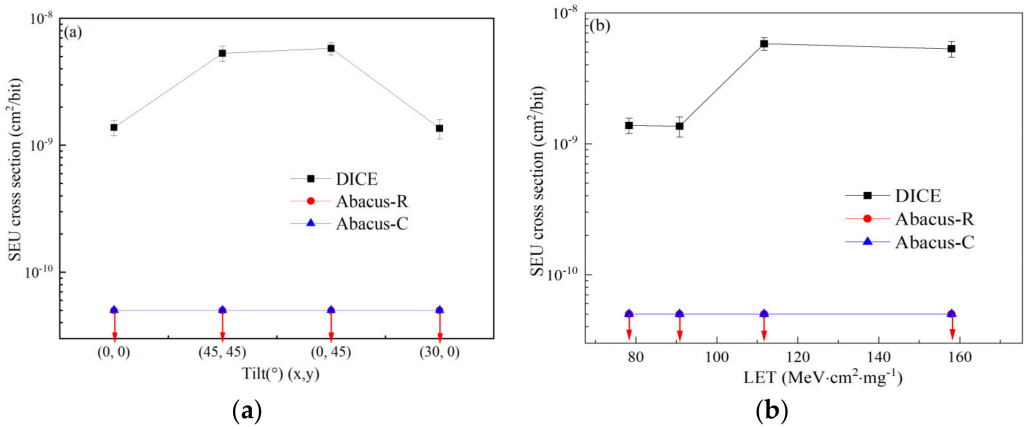

Figure 10. SEU cross section results for full "0" data under (**a**) different irradiation tilts, and (**b**) different LET values.

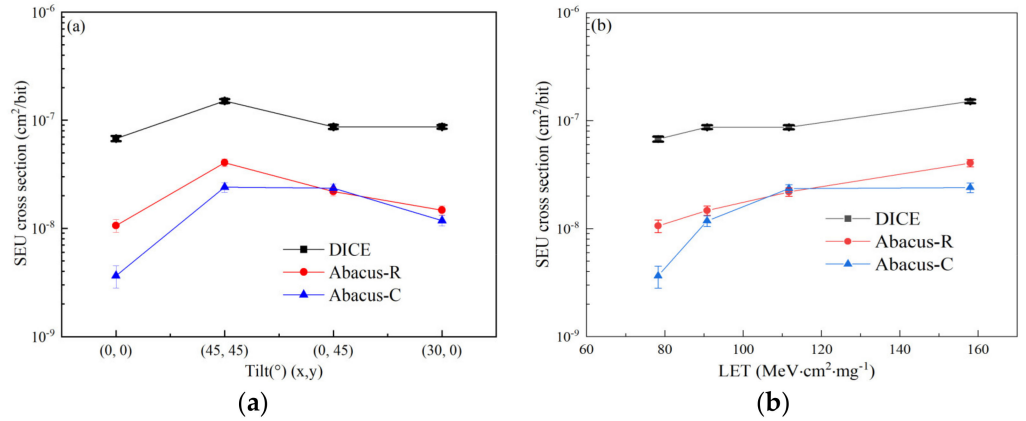

Figure 11. SEU cross section results for full "1" data under (**a**) different irradiation tilts, and (**b**) different LET values.

5. Conclusions

In this paper, the radiation response of our proposed DFFs with novel abacus-type time-delay cells manufactured by 40 nm planar technology are investigated, and plenty of interesting results are observed in our specially arranged heavy ion irradiation experiments. Benefiting from the changed area and location of the sensitive nodes in layouts, the abacus-type time-delay cell possessed a superior radiation resistance, reducing the SEU cross sections in a considerable degree, though the LET value of heavy ions is high. Our systematic vertical and tilt-angle irradiations confirm that the degree of SEU rate elimination is closely related to the working modes and data patterns. The improved SEU tolerance of the abacus-type circuits indicates that more charge diffusion and deposition in the sensitive nodes of peripheral time-delay circuits are needed to trigger an upset in these hardened circuits. Even without the additional reinforcement, the abacus-hardened module is appropriate for application in harsh radiation environments to further improve the SEU tolerance of the cell-hardened circuits. Moreover, the novel abacus-type layouts are also useful to drive the complex clock and reset networks to achieve high-reliable electronic systems in the future.

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