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Low Switching Frequency Operation Control of Line Voltage Cascade Triple Converter

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Abstract: With the increasing power level of wind power generation system, the traditional topology of power converters can no longer meets the demand of high-power wind power generation systems due to the limitation of device performance. The line voltage cascade type multiple PWM converter (LVC-VSC) is a kind of converter that uses the traditional two-level and six-switch voltage source converter as the basic component unit, and each unit is combined with the line voltage cascade method. This type of converter is suitable for medium-voltage and high-power applications such as wind power generation and metallurgical drives because of its easy modularization, strong scalability and low number of isolated power supplies required. However, for medium-voltage and high-power applications, the switching frequency of power devices in the converter is low, usually limited to a few hundred hertz. The traditional modulation method of line voltage cascade converter has a large number of redundant states, and simply reducing the carrier ratio will cause serious degradation of control performance and system instability. To address this problem, this paper proposes a modulation strategy and a corresponding control method for low switching frequency. The modulation strategy is based on the vector relationship of finite switching states, and the optimal switching sequence is selected according to the modulation system by removing redundant states, thus ensuring the application of different modulation sequences under different modulation depths and ensuring the current quality on the basis of the minimum switching frequency, which effectively solves the control problems at low switching frequency. The experimental results show the correctness and effectiveness of the proposed modulation strategy and control method.

Keywords: triple line voltage cascade converter; low switching frequency; switching sequence; modulation depth

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1. Introduction

With the increasing power level of wind power generation systems, a series of multiple, multilevel converter topologies have been proposed by scholars to meet the application requirements of medium-voltage and high-power applications. The converters currently applicable to high-voltage level occasions can be divided into the following two categories: single DC-power inverters such as diode clamp type and capacitor clamp type; multiple DC-power inverters such as cascaded H-bridge type and cascaded three-phase bridge type [1–7]. The latter is the most widely used due to its advantages such as easy modularity and expandability [8–10]. Compared to cascaded H-bridge type inverters, cascaded three-phase bridge type inverters require fewer switching devices and DC-side capacitors (or independent power supplies), thus reducing system costs, while in terms of control, three-phase system control methods can be well applied to the system [11–15]. Therefore, line-voltage cascaded three-phase bridge inverters have good prospects for medium-voltage and high-power applications. In this paper, we take wind power generation as the application background and triple LVC-VSC as the net-side converter to carry out the research work. Figure 1 shows the main circuit topology of the triple structure applied in the wind power grid-connected system as the net-side converter [16]:

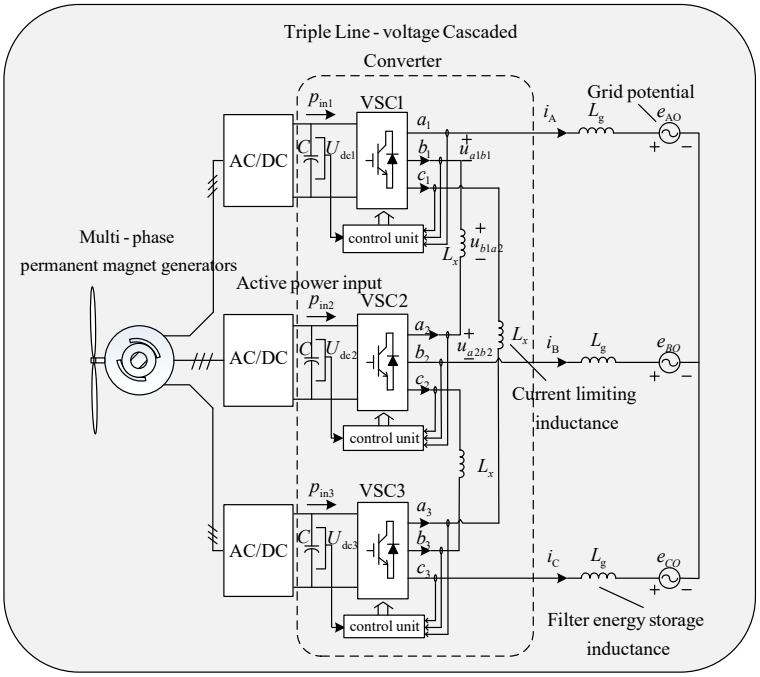


Figure 1. Schematic diagram of triple line voltage cascade type multiple PWM converter (LVC-VSC) main circuit and control system.

In the figure, the energy generated by the motor is transmitted to the power grid through an AC–DC–AC conversion. The Triple LVC-VSC operates as a grid-side converter, L_X is the current limiting inductance between power units, L_g is the grid-side filtering and energy storage inductance, and C is the DC busbar capacitance.

The traditional modulation strategy of this topology is carrier phase shifted SVPWM modulation. This modulation strategy does not consider some unnecessary switching states, resulting in low switching utilization, mainly including redundant switching states and switching states causing circulating current. The former will increase the switching frequency, while the latter will cause current shock and power loss, which will seriously affect the service life of the whole system [17–19]. At present, to address this issue, some scholars' improvement goal is the combination of three groups of modulation waves or switching signals of carrier phase-shifting. Although some redundant states are removed and the waveform quality is improved to a certain extent, it does not completely solve the inherent problems caused by the complex state of carrier phase-shifting switching [20–23]. In addition, the inter-module circulation problem is studied. The literature [24] screened a theoretical infinite current inductor with a finite switching state. Each switching state corresponds to a voltage vector. After removing the redundant states, 19 voltage vectors are obtained, including 18 effective voltage vectors and 1 zero voltage vector. Each voltage vector corresponds to a plurality of switching states, thus forming a set of switching states. The switching frequency is reduced by preferential selection of them.

However, for the screened voltage vectors, only simple single vector modulation can not ensure good output performance at low switching frequency operating conditions. On the contrary, it is necessary to improve the switching frequency to make up for the deficiency of single vector modulation, which is contrary to the concept of low switching frequency in a high power level. In this paper, we reprogram the voltage space vector diagram in the ideal switching state. On this basis, the modulation vector is synthesized by using the selection principle of the nearest three vectors. Finally, in the low modulation depth area, the switching frequency is reduced to less than half of the carrier frequency; in the high modulation depth area, the switching frequency is reduced to about one third of the carrier frequency. By analyzing the current harmonics caused by several sequences from the perspective of the switching stage, the optimal modulation sequence is found

for different modulation depths, which ensures both low switching frequency and current quality. Finally, it is simulated and experimentally verified in low switching frequency operating conditions.

2. Conventional Carrier Phase Shift Modulation Strategy

The structure of triple LVC-VSC as a network-side rectifier is shown in Figure 2, which consists of three two-level voltage source converters (VSC) combined by line voltage cascade. According to its structural characteristics, the traditional two-level SVPWM modulation strategy can be combined with carrier phase shift technology to obtain a modulation strategy suitable for this topology—carrier phase shift SVPWM modulation strategy.

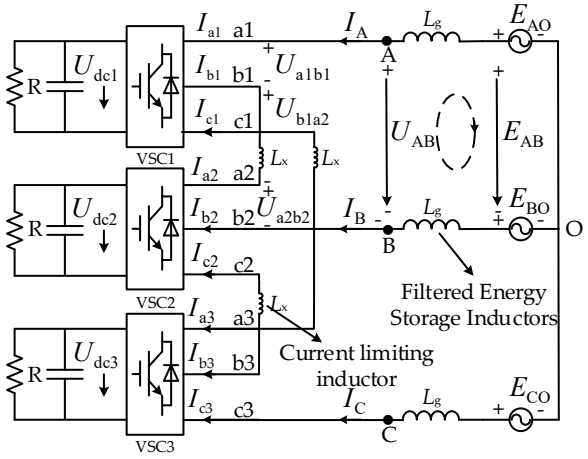


Figure 2. Diagram of triple LVC-VSC operating in rectifier status.

In Figure 2, U_{b1a2}, U_{a1b1}, and U_{a2b2} are the current-limiting inductor voltages between unit 1 and unit 2 modules, the phase A and B line voltages of unit 1, and the phase A and B line voltages of unit 2, respectively. U_{AB} is the entire triple structure A and B phase line voltage, and E_{AB} is the electric potential value between phases A and B of the grid. u_{dc1}, u_{dc2} and u_{dc3} are the DC bus voltage values for cell 1, cell 2, and cell 3, respectively.

The specific modulation method is as follows: the triple LVC-VSC uses three SVPWM calculation units, each corresponding to a space vector map coordinate system with an axis length of $2*U_{av}/3$, where U_{av} is the average value of the three sets of DC bus voltages. The modulated voltage output from the controller is compared with the three sets of carriers to obtain the switching signal and act on the converter. The three sets of VSC module carriers have the following correspondence in phase, the initial phase of the second set of carriers lags the first set of carriers by 1/3 carrier period, the initial phase of the third set of carriers lags the second set of carriers by 1/3 carrier period, and the relationship between the three sets of carriers and the modulating waveform is shown in Figure 3.

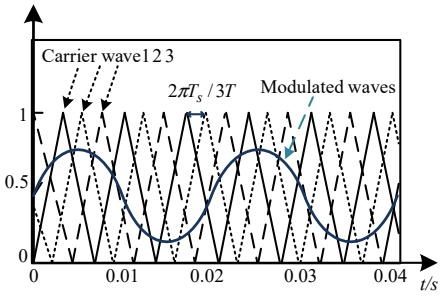


Figure 3. The relationship between modulation wave and three sets of carrier phase in carrier phase shifting modulation.

The three sets of output drive signals correspond to the switching tubes of each VSC, and the specific relationship is shown in Figure 4.

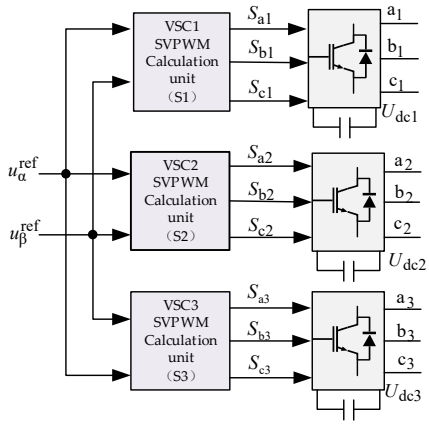


Figure 4. Correspondence of carrier phase shift switching signals.

In the figure, $u_\alpha^{ref}, u_\beta^{ref}$ is the modulated voltage output from the closed-loop controller in the stationary coordinate system component, and S_{mi} is the switching signal output from the modulation unit (m indicates phase a, phase b or phase c; i indicates unit 1, unit 2 or unit 3).

The whole control system adopts the integrated control method, so the equivalent circuit model of the triple structure needs to be established. According to the loop formed by unit 1 and unit 2 in Figure 2, the following expression can be derived:

$$\begin{cases} U_{AB} = U_{a1b1} + U_{a2b2} + U_{b1a2} = j\omega L_g(I_A - I_B) + E_{AB} \\ U_{BC} = U_{b2c2} + U_{b3c3} + U_{c2b3} = j\omega L_g(I_B - I_C) + E_{BC} \\ U_{CA} = U_{c3a3} + U_{c1a1} + U_{a3c1} = j\omega L_g(I_C - I_A) + E_{CA} \end{cases} \quad (1)$$

U_{c2b3}, U_{b2c2}, and U_{b3c3} are the current-limiting inductance voltages between unit 2 and unit 3 modules, the B and C phase line voltages of unit 2, the B and C phase line voltages of unit 3, respectively. E_{BC} is the electric potential value between Grid B-phase and C-phase. U_{a3c1}, U_{c3a3} and U_{c1a1} are the current-limiting inductance voltages between unit 3 and unit 1 modules, the C and A phase line voltages of unit 3, the C and A phase line voltages of unit 1, and E_{CA} is the electric potential value between Grid C-phase and A-phase.

When the transmitted power is balanced, the DC bus voltages of each VSC module are equal, which is known by symmetry:

$$\begin{cases} U_{a1b1} = U_{a2b2} = U_{a3c3} \\ U_{b1c1} = U_{b2c2} = U_{b3a3} \\ U_{c1a1} = U_{c2a2} = U_{c3a3} \end{cases} \quad (2)$$

According to Equation (2), Equation (1) can be rewritten as follows:

$$\begin{cases} U_{A'B'} = U_{AB} - j\omega L_{gx}(I_A - I_B) \\ U_{B'C'} = U_{BC} - j\omega L_{gx}(I_B - I_C) \\ U_{C'A'} = U_{CA} - j\omega L_{gx}(I_C - I_A) \end{cases} \quad (3)$$

$U_{A'B'}, U_{B'C'}, U_{C'A'}$ is the equivalent AC side line voltage vector, and its values are:

$$\begin{cases} U_{A'B'} = U_{a1b1} + U_{a2b2} \\ U_{B'C'} = U_{b2c2} + U_{b3c3} \\ U_{C'A'} = U_{c3a3} + U_{c1a1} \end{cases} \quad (4)$$

L_{gx} is the inductance of the current-limiting inductor L_x after equating to the three-phase AC side and superimposing with the filter inductor L_g, whose value is:

$$L_{gx} = L_g + L_x/3 \tag{5}$$

From Equations (2) and (4), we can conclude that the equivalent AC side line voltage amplitude is equal to two times the AC side line voltage amplitude of each VSC, and since the AC side line voltage amplitude of each VSC is equal to its DC bus voltage value, the line voltage amplitude after equivalence is two times the DC bus voltage amplitude of each module, i.e.:

$$U_{eq} = 2U_{av} = 2\frac{(U_{dc1} + U_{dc2} + U_{dc3})}{3} \tag{6}$$

The overall capacitance value can be obtained according to the power conservation principle as:

$$C_{eq} = C/2 \tag{7}$$

Based on the above analysis, the equivalent circuit model can be obtained as shown in Figure 5:

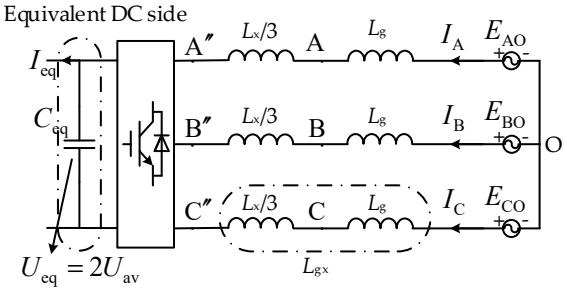


Figure 5. Triple equivalent circuit model under transmission power balance.

The equivalent circuit model can be used to instantiate the design of the converter. Taking the medium-voltage power level as an example, the entire converter needs to achieve a DC output of 1200 V. In the triple topology, a single VSC unit with an output of 600 V can meet the power requirements. Therefore, taking into full consideration the overall power level of this experimental system, the FGA40N120D IGBT is selected as the basic power device with a VSC power device with a withstand voltage value of 1200 V and a maximum collector current of 40 A current. At the same time, the power unit drive module needs to be designed, and the M57962AL driver chip is selected to build the drive circuit of the system in combination with the selected IGBT model, and a logic protection circuit consisting of a logic gate chip is added to the drive circuit to prevent the upper and lower bridge arms from conducting in the same phase. In addition, the main circuit on the AC side requires a filter inductor and a current limiting inductor. The selection of the filter inductor requires that the voltage drop on it does not exceed 3% to 5% of the peak AC line voltage when the converter is operating.

For the conventional carrier phase-shifted SVPWM modulation method, there is a strong coupling effect between the individual VSC modules in some switching states, and based on the equivalence model, only the external equivalence is established, and the internal electrical connections cannot be analyzed in the equivalence model. Since the conventional modulation algorithm does not have the necessary constraints on the switching states, it contains a large number of redundant states [24], which causes unnecessary switching losses and current shocks and becomes a problem that cannot be avoided by the conventional modulation algorithm. Therefore, the circuit between cascaded modules needs to be analyzed to avoid non-ideal switching states and to improve the modulation algorithm.

3. Nearest Three-Vector Modulation Strategy Based on Ideal Switching State Model

3.1. Ideal Vector Switching State Selection

The screening principles are: no circulating current, no short circuit, and minimum number of adjacent vector switches.

There are more line voltage cascaded inverter switch combination states, and they will be respectively represented by three digits (X1 X2 X3), where X1, X2, X3 are all arbitrary numbers between 0 and 7, a total of $8^3 = 512$ combinations. Respectively, representing the switch state corresponding to the three-phase upper bridge arm switch tube of unit 1, unit 2, unit 3, each number and the two-level voltage source inverter switch state relationship as shown in Table 1. For example, (X1 X2 X3) = (1 2 3) means that the three-phase upper bridge arm switch states of unit 1 is 001; the three-phase upper bridge arm switch states of unit 2 is 010; the three-phase upper bridge arm switch states of unit 3 is 011.

Table 1. Corresponding switch states of single VSC.

Number	0	1	2	3	4	5	6	7
State	000	001	010	011	100	101	110	111

The equivalent circuits for different switching states is analyzed and then filtered to obtain the desired ideal switching states with no circulating current and no short circuit. Taking (444) as an example, the switching state of each unit is 100, and its path is shown in the left figure in Figure 6, and the right figure is the equivalent model of the path in this state.

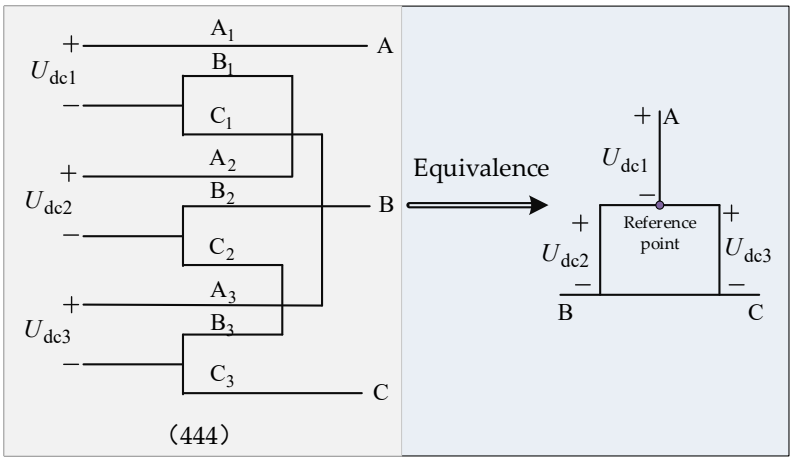


Figure 6. Path diagram and equivalent circuit model under switching state (444).

The other switching states are analyzed as above, and Figure 7 shows the screened equivalent circuit connection diagram that meets the conditions. Below the equivalent circuit are the constraint states of this kind of circuit. A total of 96 switching states are screened and are classified into the following six groups, where ⊙ denotes the "same", "or" logical. If the logic is 1, port 3 and port 4 in Figure 7a are connected to the negative side of the power supply, and port 1 and port 2 in Figure 7b are connected to the positive side of the power supply, and if the logic is 0, neither of the above two groups of ports is connected. S_{ij} indicates the on state of the switch tube of the upper bridge arm of phase j in the ith VSC cell: 1 indicates the on state and 0 indicates the off state.

Take a switch state of group a as an example: as can be seen from Figure 7, at this time the constraint is $S_{1B} = S_{1C} = 0$; $S_{2A} = S_{3A} = 1$; $S_{2C} \odot S_{3B} = 1$, the remaining states S_{1A}, S_{2B}, S_{3C} state and the circuit connection mode correspondence is as shown in Table 2.

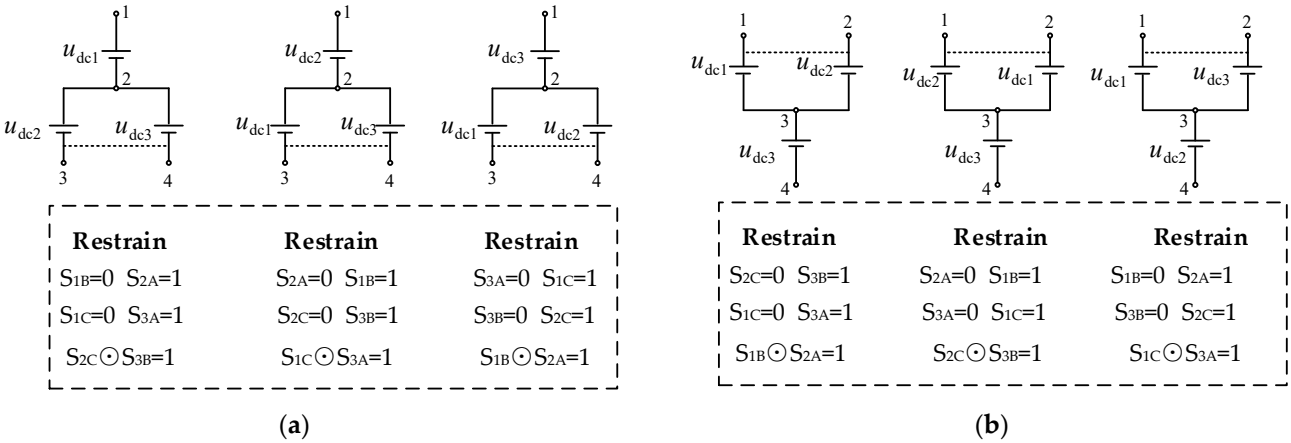


Figure 7. Each group of switch combinations and their constraint states. (**a**) First three sets of switching constraints; (**b**) Rear three sets of switching constraints.

Table 2. Corresponding relationship between switch state and three-phase output.

	State = 1	State = 0
S_{1A}	A connection port 1	A connection port 2
S_{2B}	B connection port 3	B connection port 2
S_{3C}	C connection port 4	C connection port 2

A new voltage space vector diagram can be obtained based on the above switching states, as shown in Figure 8.

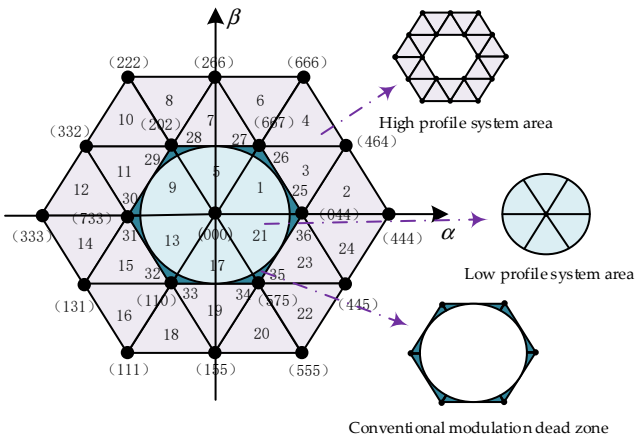


Figure 8. Triple 19 vector voltage space vector diagram and sector division.

It contains 18 effective voltage vectors, which can be divided into large, medium and small vectors according to their length, the length of large vector is $4*U_{dc}/3$; the length of medium vector is 2*sqrt(3)* U_{dc} /3; the length of small vector is $2*U_{dc}$ /3. Each vector corresponds to multiple switching states. To ensure the minimum number of switching times when adjacent vectors are switched, 20 switching states are selected, of which 18 correspond to effective vectors and two correspond to zero vectors.

3.2. Sector Division of Three-Vector Modulation Strategy and Vector Selection

In this paper, the voltage space vector diagram is divided into 36 sectors. In Figure 8, the whole voltage space vector diagram can be divided into the above three areas ac-

cording to different modulation depths, and the following is the calculation formula of modulation depth.

$$m = \frac{V_s}{U_{max}} = \frac{\sqrt{3}V_s}{2U_{dc}} = \frac{\sqrt{3v_d^2 + 3v_q^2}}{2U_{dc}} \tag{8}$$

Low modulation depth area: $m \leq 0.5$;
High modulation depth area: $0.5 \leq m \leq 0.577$;
Traditional modulation dead area: $m \geq 0.577$.

The sector distribution of each area is shown in the figure where m is the modulation depth, V_s is the modulating voltage, U_{max} is the maximum output voltage of the trivialized system, and V_d, V_q is the modulating voltage V_s component in the dq coordinate system.

When the vector is located in the low modulation regime and high modulation regime, the basic voltage vector is selected and vector synthesized according to the nearest three vectors principle, which can be calculated from the number of switching tube actions during vector switching in the space vector diagram, and the vector selected by this principle can reduce the switching frequency to 1/3 of the carrier frequency in the high modulation regime; and reduce the switching frequency to 1/2 of the carrier frequency in the low modulation regime. When the vector is located in the traditional modulation dead zone, the target vector cannot be synthesized based on the nearest three vectors method, and the vector needs to be reselected, then the nearest medium vector can be used to replace the smaller vector which is farther away to ensure the lowest switching frequency while synthesizing the vector. Take sector 25 as an example, since (000), (044) and (667) cannot synthesize the target vector, then (464) is selected to replace (667) to complete the vector synthesis.

3.3. Vector Action Time and Duty Cycle Calculation

Similar to the traditional two-level SVPWM modulation algorithm, the modulating voltage is synthesized using the principle of volt-second balance, taking the first sector as an example: when the modulating voltage vector is located in the first sector, the three vectors selected by the principle of the nearest three vectors are (044), (667) and (777), and the zero vector is selected based on the minimum number of switches, Figure 9 shows the volt-second balance synthesized voltage vector diagram.

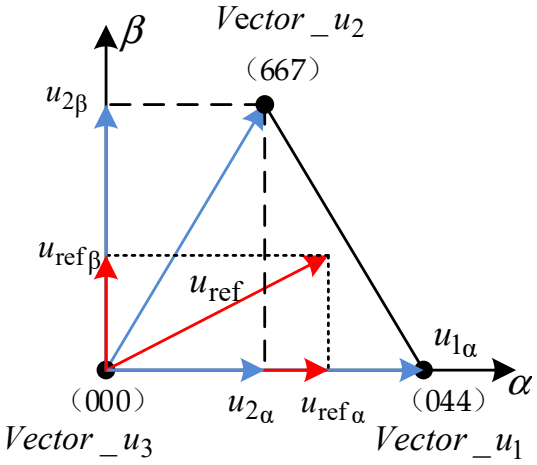


Figure 9. First sector modulation voltage synthesis vector diagram.

*V*ector_u_1, *V*ector_u_2, *V*ector_u_3 are the three selected vectors, $u_{1\alpha}$, $u_{2\alpha}$ are vector 1 and vector 2 in α-axis component, $u_{1\beta}$, $u_{2\beta}$ are vector 1 and vector 2 in β-axis component, u_{ref}, $u_{ref\alpha}$, $u_{ref\beta}$ are modulating voltage and modulating voltage in α-axis and β-axis component, respectively.

The principle of volt-second balance is that in a control cycle, the principle of average equivalence is used so that the total effect of the three vectors is equal to the effect of the modulating vector action, and the following equation can be obtained.

$$\begin{cases} u_{\text{ref}\alpha} = u_{1\alpha} * D_1 + u_{2\alpha} * D_2 \\ u_{\text{ref}\beta} = u_{1\beta} * D_1 + u_{2\beta} * D_2 \\ D_3 = 1 - D_1 - D_2 \\ D_1 = T_1 / T_{\text{s\_control}} \\ D_2 = T_2 / T_{\text{s\_control}} \\ D_3 = T_3 / T_{\text{s\_control}} \end{cases} \tag{9}$$

where T_1, T_2, T_3 corresponds to the action time of vector 1, vector 2 and vector 3 in one control cycle, respectively. Ts_control is the control cycle, and D_1, D_2 and D_3 are the duty cycles of the three vectors in a single control cycle.

The modulation method combined with the integrated control method based on the equivalent circuit model of Figure 5 constitutes the entire closed-loop control system of this paper, as shown in Figure 10.

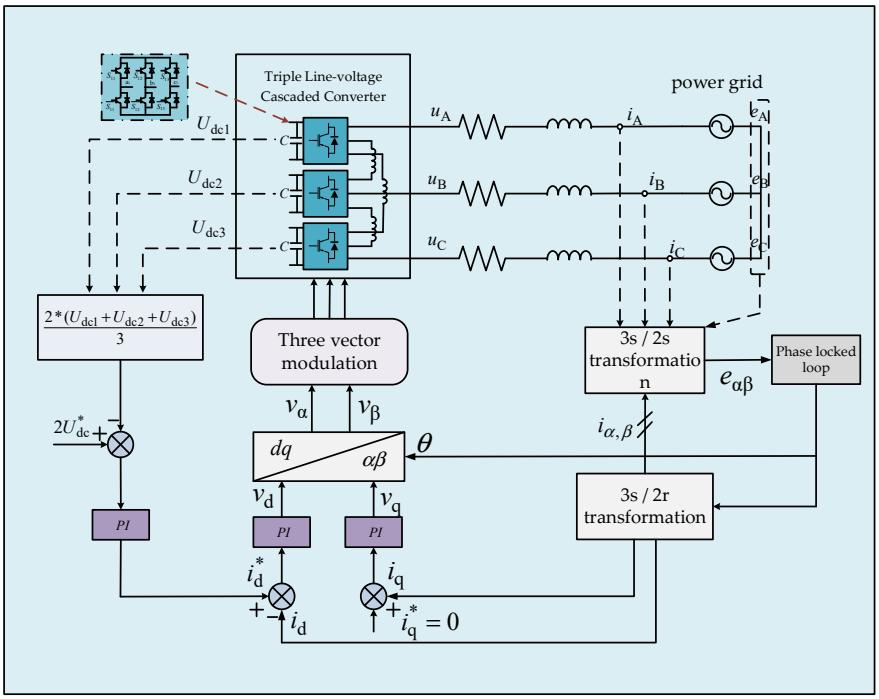


Figure 10. Triple double closed loop control block diagram.

4. Vector Action Sequence and Current Fluctuation Suppression

4.1. Analysis of Current Fluctuations within a Single Control Cycle

Analysis of the causes of the formation of current fluctuations: vector synthesis are based on the average equivalent of vector action in a control cycle, but at a certain point the output is still a single vector, and the modulation vector will form a voltage difference, which reflected in the current is the current fluctuations, the following is a quantitative analysis of current fluctuations [25], the voltage difference:

$$v^*(t) = v(t) - v_{\text{Ts}}(t) \tag{10}$$

$v(t)$: The basic voltage vector selected at the current time;$v_{\text{Ts}}(t)$: Modulation voltage value.

The single-phase equivalent model of the power converter at the grid side can be approximated as shown in Figure 11.

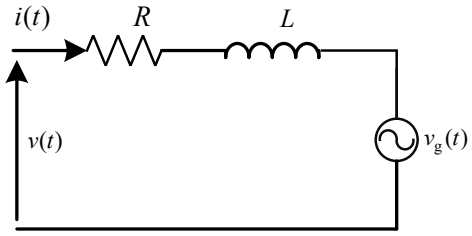


Figure 11. Single phase equivalent model.

Then:

$$v^*(t) = v(t) - v_{\mathrm{Ts}}(t) = R * [i(t) - i_{\mathrm{Ts}}(t)] + L * [\frac{di(t)}{dt} - \frac{\Delta i(t)}{T_s}] + [v_g(t) - \overline{v}_g(t)] \quad (11)$$

The first and last terms are negligible, and Equation (11) can be simplified as follows:

$$v^*(t) = L * [\frac{di(t)}{dt} - \frac{\Delta i(t)}{T_s}] \quad (12)$$

Further discretization can be obtained:

$$\Delta\widetilde{i}(t) = \frac{1}{L} * \int v^*(t)dt + \frac{t}{T_s} * \Delta i(t) \quad (13)$$

$\Delta\widetilde{i}(t)$: Total current variation;
$\frac{1}{L} * \int v^*(t)dt$: the variation of harmonic current;
$t/T_s * \Delta i(t)$: Fundamental current variation.

It can be seen that the offset direction of the fundamental current can be determined according to the positive and negative of the voltage error [25].

4.2. Vector Action Sequence and Current Fluctuation

From the above way of analyzing harmonics, it can be seen that only the current fluctuation in one control cycle is considered, because on most occasions, the current fluctuation in a single cycle and the current fluctuation in the whole electric cycle are approximately the same, while on some special occasions, the two are not approximately equal.

This section summarizes several factors influencing the switching-level current harmonics throughout the electrical cycle.

(1) Within a single control cycle

The choice of the fundamental voltage vector, which influences the magnitude of the voltage error and is the most direct influencing factor.

(2) During adjacent control cycles

The current offset when the vector at the end of the previous control cycle is switched to the initial vector of the current control cycle; the current offset when the vector at the end of the current control cycle is switched to the initial vector of the next control cycle.

(3) When adjacent sectors are switched

Current offset when the last vector of the previous sector is switched to the first vector of the current sector; current offset when the last vector of the current sector is switched to the first vector of the next sector.

For the traditional two-level modulation strategy, the symmetrical waveform such as five-segment, seven-segment, etc. is often used, and the characteristic of this waveform is that the first vector and last vector are zero vectors within a single control cycle, so that the influence factor 2 and influence factor 3 do not need to be considered, at this time it can be said that the minimum current fluctuation in a single control cycle is basically the same as the minimum current fluctuation in the whole electric cycle.

For the modulation strategy described in this paper, in order to take full advantage of the minimum number of switching times when adjacent vectors are switched, the three-vector sequential waveform is used instead of the traditional five- stage and seven-stage

waveform, the latter reduces the current fluctuation to a certain extent, but will greatly increase the switching frequency, which is contrary to the requirement of low switching frequency in medium and high power applications.

The working condition studied in this paper is a low-switching frequency operating condition, where the carrier ratio is usually within 10, and the influence factors 2 and 3 must be fully considered. In the higher regulation depth in particular, there are 12 sectors, and the sectors where the voltage vectors of adjacent control cycles are located are not the same. Therefore, the current fluctuations of adjacent control cycles should be fully considered when selecting the vector action sequence while ensuring a lower switching frequency. Ultimately, the optimal selection of the vector action sequence can solve the difficult problem of high current quality at low switching frequency for high-power transmission. The following is an example of A-phase fluctuation at low switching frequency operating conditions, and summarizes the ideal fluctuation mode of sequential waveform generation with minimum current offset in a single control cycle and minimum current offset in the whole electric cycle at low switching frequency.

4.2.1. Harmonic Analysis and Sequence Optimization within a Single Control Cycle

The following is an example of the A-phase fluctuation in the first sector, summarizing the ideal fluctuation mode under the sequence of vector action corresponding to the minimum current offset in a single control cycle in the low modulation depth, and the following figure indicates the relationship of each voltage vector in the first sector.

In Figure 12, V_c is the modulating voltage vector, V_A is the component of the modulating voltage on phase A, vector 1, vector 2 in phase A projection are $2^*U_{dc}/3$, $U_{dc}/3$, respectively. Therefore, there are two position relationships between the three as shown in Figure 13, the following corresponding to the optimal vector sequence in a single control cycle for each position relationship. (*U* for upward offset; *D* for downward offset).

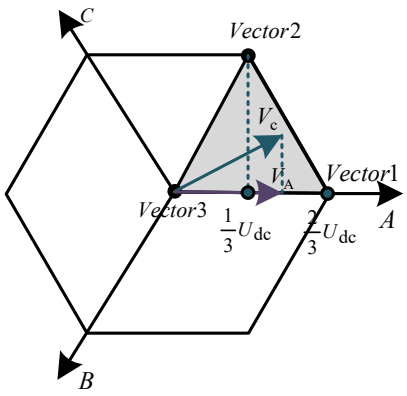


Figure 12. The first sector vector is projected in phase *A*.

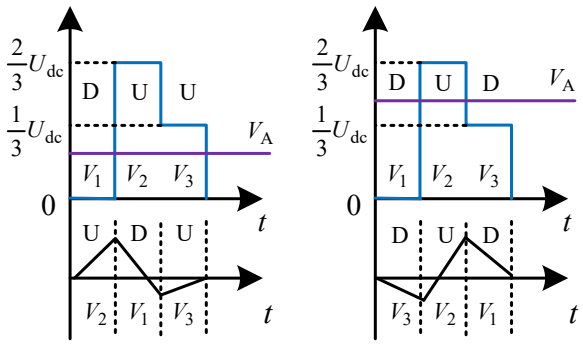


Figure 13. Ideal current offset mode of single control cycle.

V_1, V_2, V_3 is the basic voltage vector. Combined with the current offset regularity derived in Section 3.1, it can be seen that the vector sends waves in the order of $V_2V_1V_3$ or $V_3V_2V_1$ to minimize the amount of current fluctuation in that control cycle.

4.2.2. Analysis of Current Fluctuations throughout the Electrical Cycle and Sequence Optimization

At this time, the modulating voltage is located in the high modulation depth area, for example, within one electrical cycle, the modulating voltage will pass through 12 sectors. Taking into account the current fluctuations when switching sectors, the following law is analyzed in this process: Because there are three basic voltage vectors acting in one control cycle, the vectors will necessarily be shifted three times. That is, the following two situations will occur.

Case 1. shifted down twice and shifted up once.

Case 2. shifted down once and shifted up twice.

During the counterclockwise rotation of the vector, if the vector is shifted up once and down twice during the current control cycle, then the adjacent control cycle must be shifted down once and up twice. In order to ensure minimal fluctuations throughout the electrical cycle, it was finally found to be optimal for the fundamental current to be offset in the following manner.

UDD-UUD-UDD——UDD-UUD or DUU-DDU-DUU——DUU-DDU

The following Figure 14 is a graph of the current fluctuations when the vector is located in the high modulation regime area offset in the above manner.

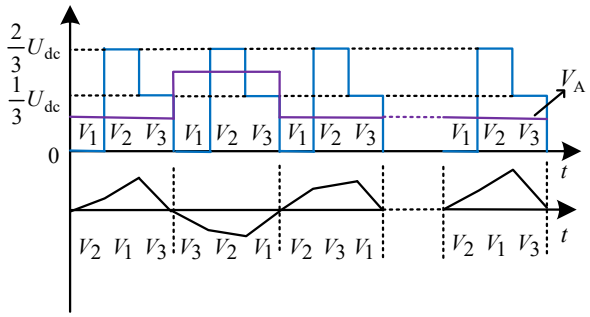


Figure 14. Ideal current offset mode of electric cycle.

Since the control accuracy of the algorithm is for one control cycle and it is not possible to control the entire electrical cycle directly, the above ideal offset approach can only be used as an evaluation criterion. According to the symmetry principle, the order of vector action in each sector is fixed and its does not change with time. By numbering each sector vector counterclockwise V_1, V_2, V_3 according to Figure 12, the final fixed order has the following six as shown in Table 3:

Table 3. Trivector switching sequence.

Number	N_1	N_2	N_3	N_4	N_5	N_6
Order	$V_1V_2V_3$	$V_1V_3V_2$	$V_2V_1V_3$	$V_2V_3V_1$	$V_3V_1V_2$	$V_3V_2V_1$

It is filtered by the evaluation criteria analyzed above and Equation (13), and the final analysis shows that the current offset under the action sequence of N_1 is closest to the ideal case and is not affected by the modulation depth, and finally the simulation is verified under two operating conditions respectively, which proves the correctness of the theory.

Working condition 1: DC bus voltage: 320 V; electrical frequency: 100 Hz; control frequency: 2 KHz; switching frequency: 800 Hz; regulation: 0.765 (high); carrier wave ratio: 8.

Working condition 2: DC bus voltage: 540 V; electrical frequency: 100 Hz; control frequency: 2 KHz; switching frequency: 900 Hz; regulation system: 0.454 (low); carrier wave ratio: 9.

Simulation of the minimum fluctuation of a single control cycle under two operating conditions was also done for comparison with the above, as follows.

From the comparison of THD values in Figures 15 and 16, the simulation results, it can be seen that the vector action order of N_1 = 123 is optimal, mainly because the vector action order of N_1 = 123 is counterclockwise, which is consistent with the vector rotation direction, and has period symmetry, which can satisfy the whole electric cycle harmonic minimum regularity. At the same time, it can be seen from Figure 17 that the optimal single control cycle is not consistent with the optimal whole electric cycle under the low switching frequency operating conditions.

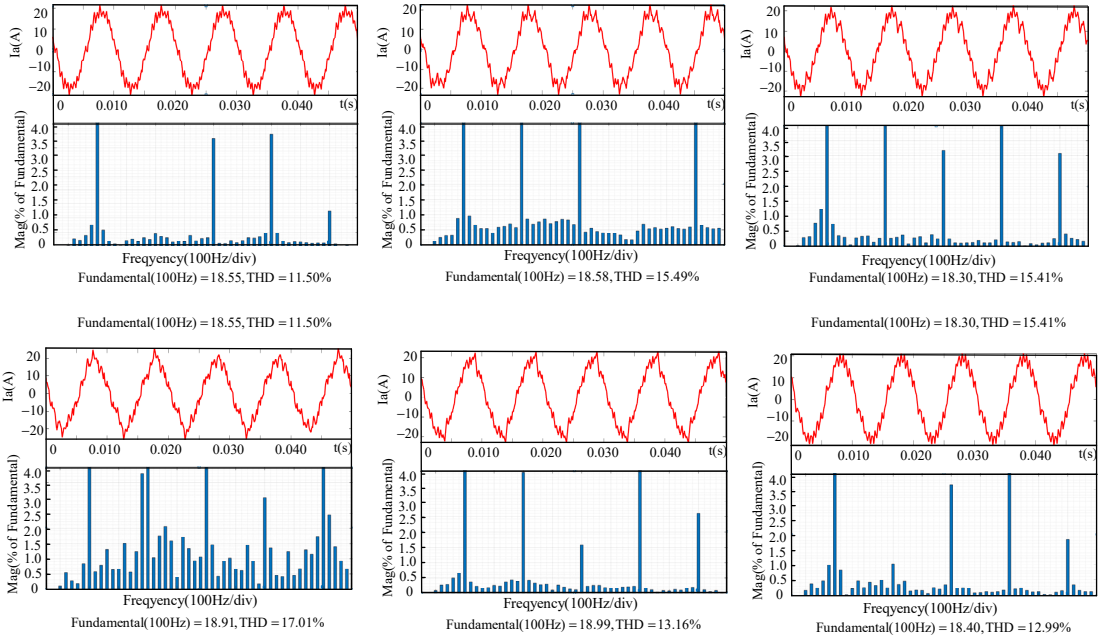


Figure 15. Analysis of three-phase current and THD under different sequences under condition 1.

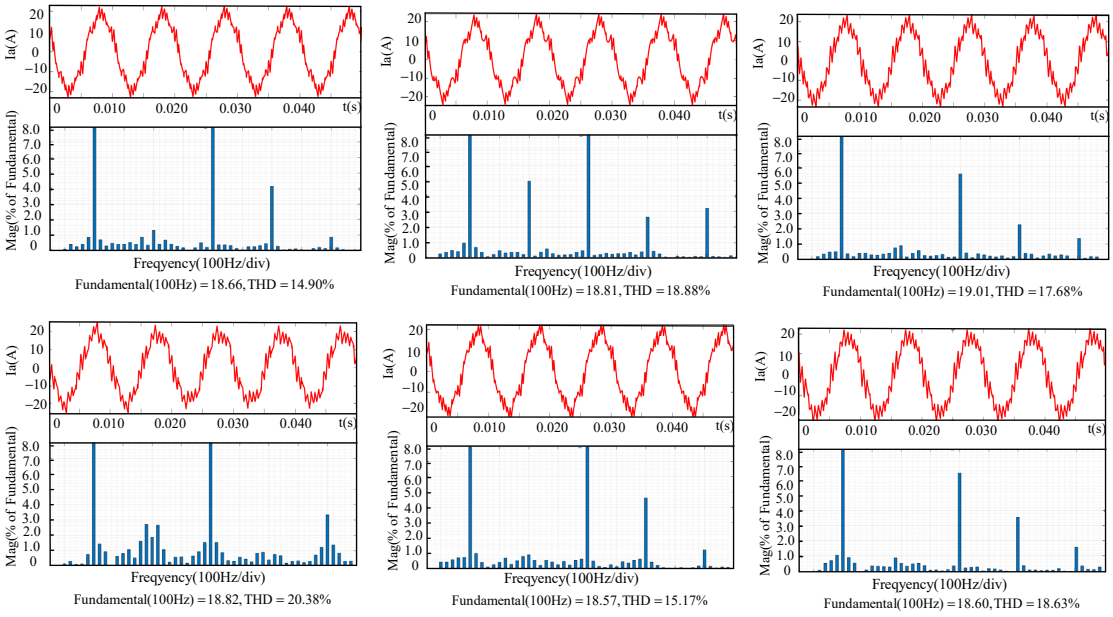


Figure 16. Analysis of three-phase current and THD under different sequences under condition 2.

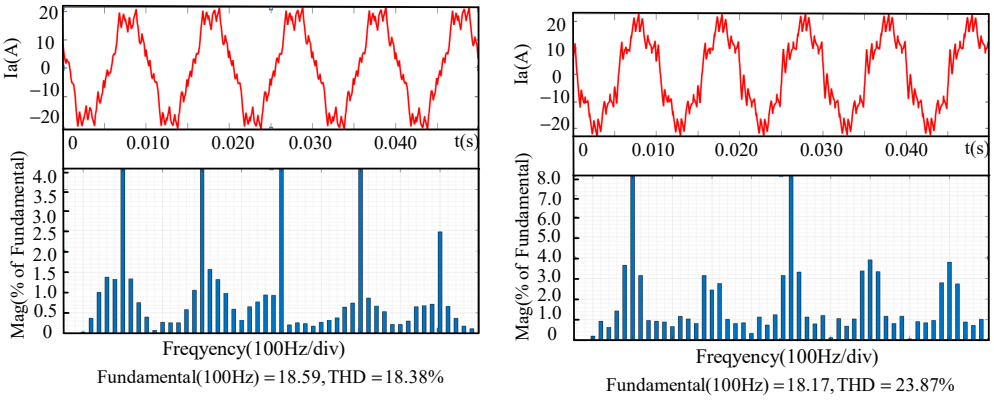


Figure 17. Harmonic optimal three-phase current and THD analysis of single control cycle under different working conditions.

5. Experimental Results Analysis

5.1. Introduction to the Experimental Platform

In order to verify the correctness and effectiveness of the above theoretical analysis, the proposed trivialized LVC-VSC control strategy was experimentally verified. A complete set of experimental platform was built as shown in Figure 18.

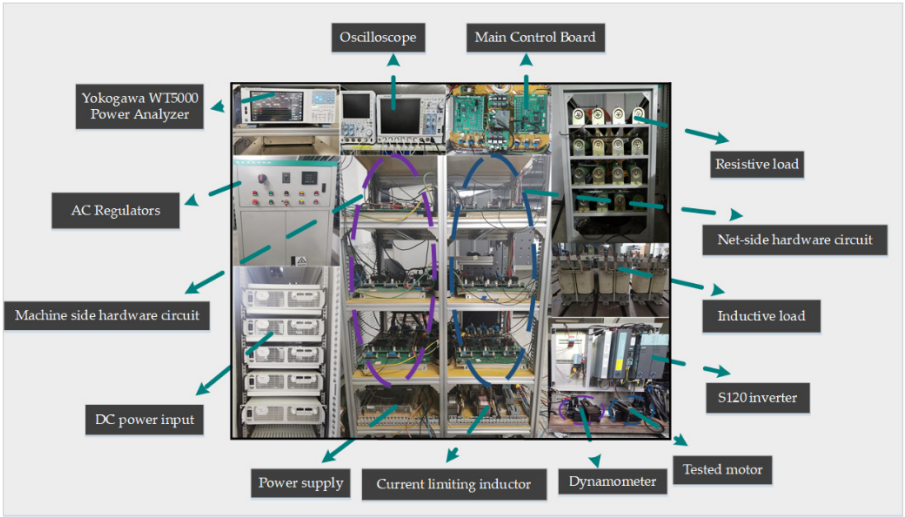


Figure 18. System physical drawing.

Based on the experimental platform shown above, the overall control circuit was designed, the following diagram illustrates each control unit of the entire system, as shown in the Figure 19.

The experimental algorithm is completed based on dual controller chips, the dsp28335 chip and Altera's FPGA chip (EP1C6Q240C8), the control algorithm and a small amount of modulation algorithm is completed through the DSP, most of the modulation algorithm is completed through the FPGA, the specific details are shown in the Figure 19.

The basic experimental parameters are shown in Table 4.

Table 4. Experimental parameters.

Parameter Name	Parameter Value
AC side filter inductor L_g/mH	4.2
Current limiting inductor L_x/mH	2
DC side capacitance C/uF	2350
Switching frequency f/Hz	300–500

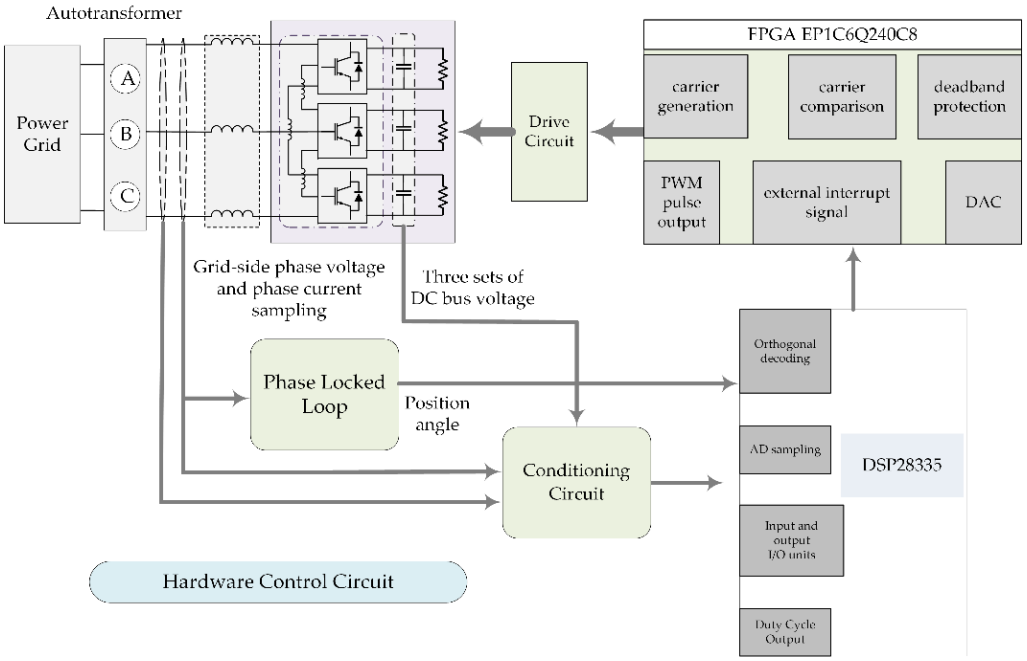


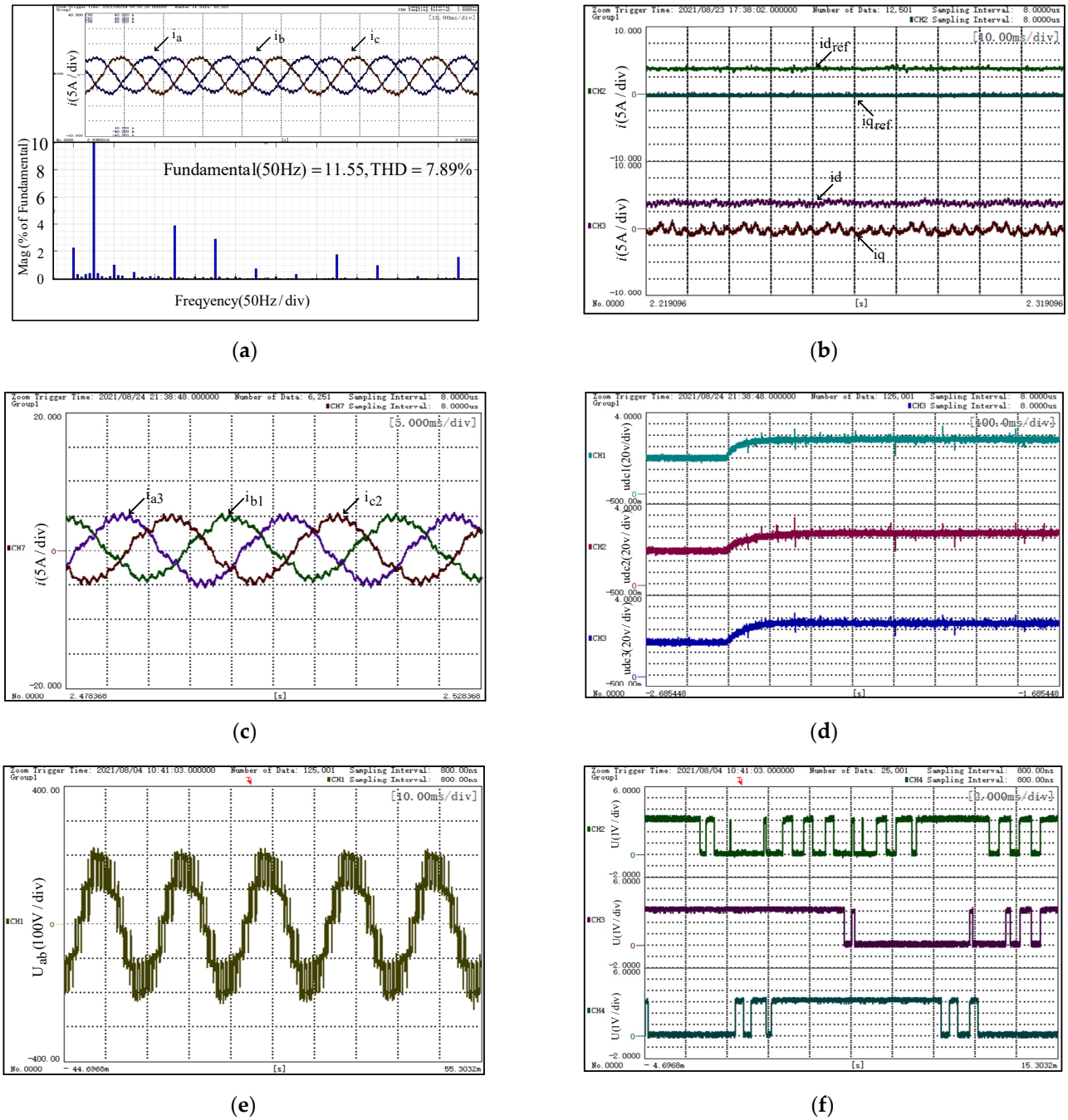
Figure 19. System main circuit and control circuit design block diagram.

5.2. Double Closed-Loop Experiments with Different Modulation Depth

5.2.1. Experimental Validation under a High Modulation Depth

The DC-side load was 30 ohms, and the AC-side power supply outputs three-phase AC power through the AC regulator. At first, the rectifier was operated in the uncontrolled rectification state, and the diode connected in parallel with the IGBT was used to charge the DC side to 60 V. After that, the tube was turned on for controlled rectification, and the given DC bus voltage was set to 100 V. The following are the voltage and current waveforms in the experiment. The three plots on the left side correspond to the network-side three-phase currents, current-limiting inductor currents and network-side line voltage values; the three plots on the right side correspond to the dq-axis currents, the three sets of DC bus voltages and the given, and the individual VSC unit switching signals.

This experiment used four times sampling to reduce the control delay on the basis of improving the dynamic performance of the system, considering the algorithm execution time, the number of samples was set to four, that is, 4 k sampling frequency, 1 k carrier frequency. The modulation system was calculated by Equation (8) as 0.6, at which time the switching frequency was reduced to about 1/3 of the carrier frequency, and the switching frequency in Figure 20f is 330 Hz indicating that the experiment matches the theory. The carrier ratio was the switching frequency fs/electric frequency fr equal to 6.6, and it can be seen from Figure 20a that the three-phase current THD value is 7.89% under the low switching frequency operating conditions, which indicates that the modulation strategy is not only applicable to the low switching frequency operating conditions but also can ensure the better inverter output performance. Figure 20b,d also illustrate the feasibility of this paper's algorithm again in terms of the tracking performance of steady-state current and steady-state voltage. Figure 20c shows the current-limiting inductor current during the experiment with good symmetry of the three phases. Figure 20e shows the net-side line voltage. Combined with the switching signal of a single two-level VSC in Figure 20f, it can be seen that with the modulation algorithm described in this paper, a certain two-phase switching tube is clamped for a long time during an electrical cycle, making the average switching frequency very low, but allowing the whole system to achieve a good output performance with a high frequency of level changes in the output line voltage.



(**a**) (**b**)

(**c**) (**d**)

(**e**) (**f**)

Figure 20. Double closed loop experimental waveform under high modulation depth. (**a**) Network-side three-phase current. (**b**) dq axis feedback current and feed. (**c**) Current limiting inductor current. (**d**) Three sets of DC bus voltage, (**e**) Net-side line voltage value $u_{ab.}$ (**f**) VSC1 Three-phase upper bridge arm switching signal.

5.2.2. Experimental Verification under Low Modulation Depth

The experimental process is similar to the high modulation depth, where the DC bus voltage is first charged to 60 V, and then the DC bus voltage is raised to 170 V by controlled rectification. The following are the voltage and current waveforms under this condition:

From Formula (8) the regulation depth is calculated as 0.338, and at this time the switching frequency is reduced to about 1/2 of the carrier frequency. Figure 21f in the switching frequency of 500 Hz shows that the experiment and the theory coincide. The carrier ratio is the switching frequency fs/electric frequency fr equal to 10, and the value of the three-phase current THD is 6.61% under the low switching frequency operating conditions

as shown in Figure 21a, which can still ensure a good inverter output performance under this modulation depth. Figure 21b,d also illustrate the feasibility of the algorithm in this paper in terms of the tracking performance of steady-state current and steady-state voltage. Figure 21c shows the current-limiting inductor current during the experiment with good symmetry of the three phases. Figure 21e shows the net-side line voltage, and combined with the switching signal of a single two-level VSC in Figure 21f, it can be seen that with the modulation algorithm described in this paper under this regulation system, a certain two-phase switching tube is also in the clamped state for a long time during an electrical cycle, which makes the average switching frequency low, and although the inverter output level is two-level at this time, it can still ensure a good output performance.

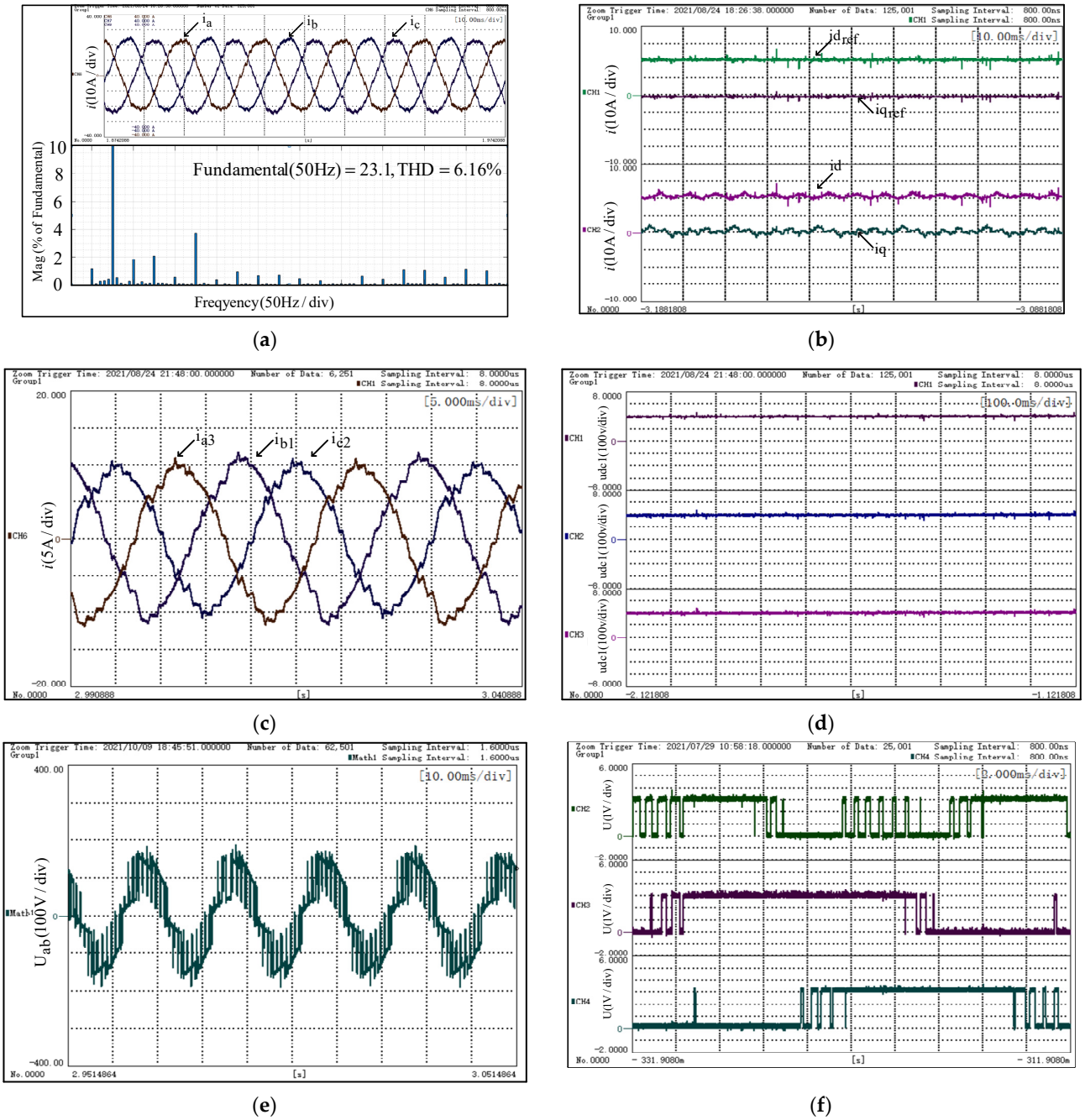


Figure 21. Double closed loop experimental waveform under low modulation depth. (**a**) Network-side three-phase current. (**b**) dq axis feedback current and feed. (**c**) Current limiting inductor current. (**d**) Three sets of DC bus voltage. (**e**) Net-side line voltage value uab. (**f**) VSC1 Three-phase upper bridge arm switching signal.

In summary, under this modulation strategy, the system can achieve low switching frequency operation in both high and low modulation regimes, and can ensure good current quality, and the theoretical analysis is consistent with the experimental results.

5.2.3. Efficiency Experiments in Different Modulation Areas

The above two sets of experiments show that the modulation strategy can achieve better results in terms of switching frequency and current quality. The following experiments will prove that the whole system can operate with high efficiency during the experimental process. The following describes the efficiency experiments of the converter operating in high and low modulation areas and at different power levels respectively, and analyzes the efficiency of the converter and the efficiency of the whole system from two perspectives.

The experimental conditions are basically the same as the experiments in the above section, DC bus voltage is still given as 100 V and 170 V, except that the power point is changed by varying the load resistance, and the resistance value is selected in the range of 20 ohms to 80 ohms, with 10 ohms as an interval, while the efficiency values corresponding to different power points are observed with a power analyzer. Due to the specificity of the triple topology, there are three groups of DC loads, and the power analyzer can only measure the efficiency of one group, therefore, it is necessary to perform power analysis for each of the three VSC units, and the final system output power is the sum of the three power groups, the following is the measured power curve in different modulation areas as shown in Figure 22:

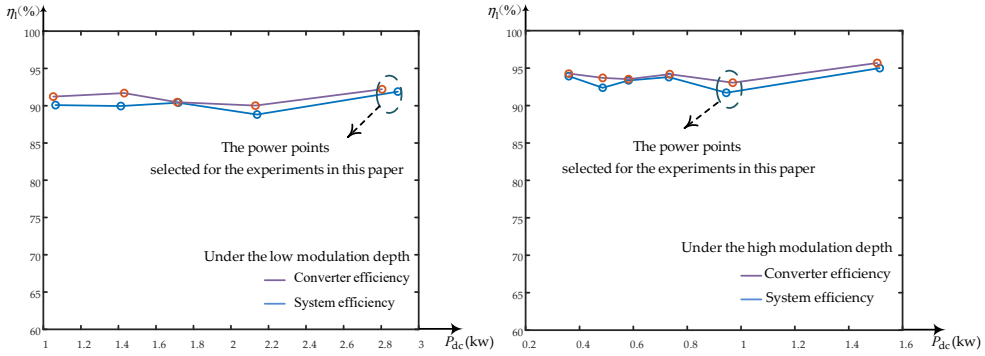


Figure 22. Efficiency curves in different modulation areas.

The efficiency experimental results of the above two modulation system areas show that, although the converter inevitably generates some reactive power and switching losses during operation, both the efficiency of the converter and the efficiency of the whole system can still be maintained above 90%, which again illustrates the correctness and effectiveness of the modulation strategy described in this paper from the side.

6. Conclusions

Triple line voltage cascade converter is suitable for medium and high voltage high power transmission field, while the traditional carrier phase shifting SVPWM has many problems: such as more redundant switching states, more narrow pulses in the switching circuit; when the carrier ratio is low, the converter AC side current harmonics increase abruptly. For medium-voltage and high-power applications, the control system carrier ratio is generally low due to the limitation of device switching characteristics, and the traditional carrier shifted phase SVPWM modulation strategy cannot meet the application requirements. For the above problems, a new modulation strategy and control algorithm were proposed in this paper, the optimal wave generation sequence was established, and the good AC output performance of the triplex converter could be guaranteed under the low switching frequency limitation. The theoretical analysis and experimental verification of the proposed algorithm were carried out under different operating conditions by means

of simulation and experimentally, and the correctness and effectiveness of the method were illustrated.

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