

Article

Wideband Rectangular Waveguide to Substrate Integrated Waveguide (SIW) E-Plane T-Junction

Roberto Vincenti Gatti , Riccardo Rossi  and Marco Dionigi 

Department of Engineering, University of Perugia, Via G. Duranti 93, 06125 Perugia, Italy; riccardo.rossi4@studenti.unipg.it (R.R.); marco.dionigi@unipg.it (M.D.)

* Correspondence: roberto.vincentigatti@unipg.it

Abstract: A broadband rectangular waveguide to substrate integrated waveguide power divider for hybrid beam forming networks is presented. Rectangular waveguide symmetric E-plane irises are used to realize a multi-section matching network. A hybrid circuit and full-wave design procedure are described and adopted to synthesize three matching networks with one, two, and three irises, progressively increasing the bandwidth and exceeding the state of the art in the last two cases. Three proof-of-concept prototypes are manufactured and tested to validate the design procedure. Good agreement between simulated and measured performance confirms the validity of the proposed solution.

Keywords: rectangular waveguide; substrate integrated waveguide; power divider; T-junction; low-cost manufacturing



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1. Introduction

Most modern microwave radar and communication systems require wideband high-gain antennas, which in many cases consist of large planar arrays. Low profile and light weight are indeed appealing features of such antennas [1], though the choice of proper technology for the implementation of the beam-forming network (BFN) is critical, as it determines the insertion loss associated with long routing paths. One approach to reducing such loss and at the same time to increase the antenna bandwidth consists in subarraying, that is, dividing the planar arrays into smaller sections, fed by a low-loss BFN based on air-filled rectangular waveguides (RWGs), substrate integrated waveguides (SIWs) or grounded coplanar waveguides (GCPWs).

SIW is a well-known technology [2,3] exhibiting a number of advantages, such as hermeticity, low profile, low insertion loss, ease of integration with other planar structures, light weight, low cost, and compatibility with standard printed circuit board (PCB) manufacturing techniques.

However, the presence of a dielectric substrate implies a higher insertion loss, especially at high frequencies. For these reasons, the air-filled RWG is still of great interest in high-performance systems. In addition to this, the robustness of RWGs makes this technology more appropriate for non-standard 3D feeding structures.

As a consequence, a viable approach for the implementation of high-performance flat antennas is based on hybrid SIW-RWG slot arrays, where the radiating section and the BFN are designed using SIW and RWG technologies, respectively. The connection of these two waveguiding structures requires the design of proper junctions.

Since modern microwave systems are often required to operate on wide bandwidths, a typical design can be represented by a SIW slot array where the single subarrays are center-fed by an RWG feeding network. This choice provides the largest bandwidth by reducing the number of series-fed slots. Therefore, it is necessary to couple microwave power between the RWG and the SIW using a hybrid E-plane T-junction. This consists of a RWG input section connecting two SIW output branches at a right angle.

Power dividers of this kind have already been studied in the literature and, since they all require a coupling aperture etched on the SIW bottom plate, bandwidth is often limited due to the slot resonant behavior. Therefore, a number of techniques have been investigated to broaden the impedance bandwidth with respect to a traditional straight structure without matching elements. In Reference [4], the SIW is locally enlarged at the junction to attenuate higher order modes and a 20-dB return loss bandwidth of 12.57% is obtained. The RWG and the SIW are slot-coupled and matched with a guiding post in [5], though bandwidth is limited to 2.35%. In Reference [6], an aperture is realized on the SIW and coupled with a radiating patch printed on an additional layer to excite the RWG. This device exhibits a bandwidth of 2.79%, which can be broadened by increasing the patch layer substrate thickness. Two dielectric layers are also employed in [7], where two SIW cavities with two H-shaped slots are designed to achieve a bandwidth of 35.66%.

This paper presents a novel RWG-to-SIW E-plane T-junction with an integrated RWG matching network based on capacitive irises. Return loss bandwidth is broadened according to the number of irises introduced and a maximum bandwidth of 40.93% is obtained. All full-wave simulations are performed with the commercial software CST Microwave Studio. Three proof-of-concept prototypes are manufactured with low-cost stereolithography (SLA) technology and electroplating. The design is validated with experimental results.

2. Power Divider Design

The power divider in Figure 1 is obtained by coupling a standard WR-75 waveguide and a SIW through an H-shaped slot etched in the SIW bottom ground plane. The SIW top ground plane is removed to show the coupling slot location. RWG input is labeled as port 1, while the SIW outputs as ports 2 and 3.

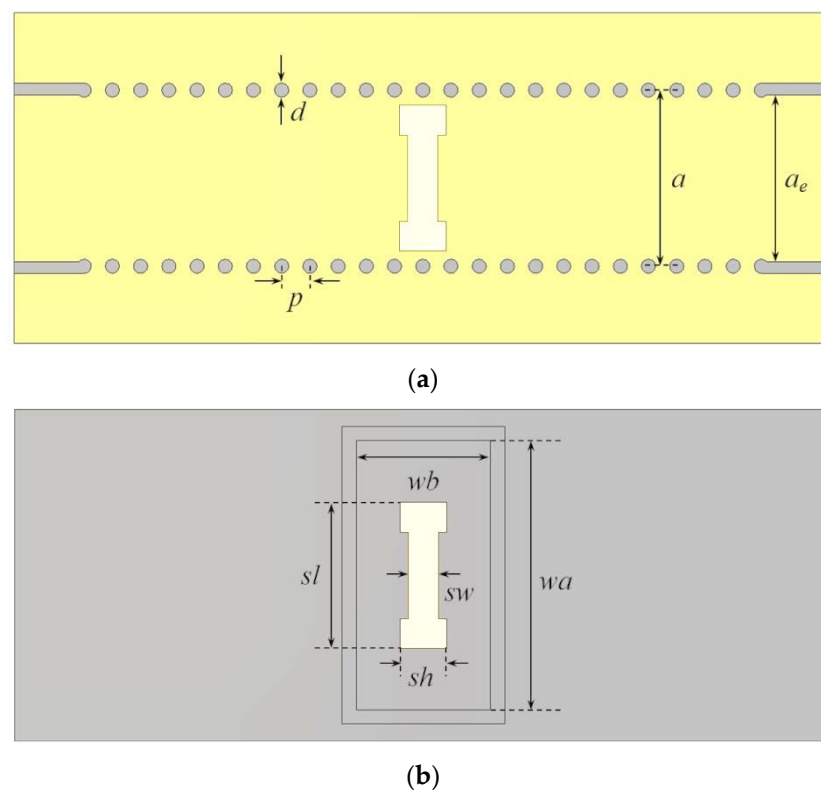


Figure 1. Cont.

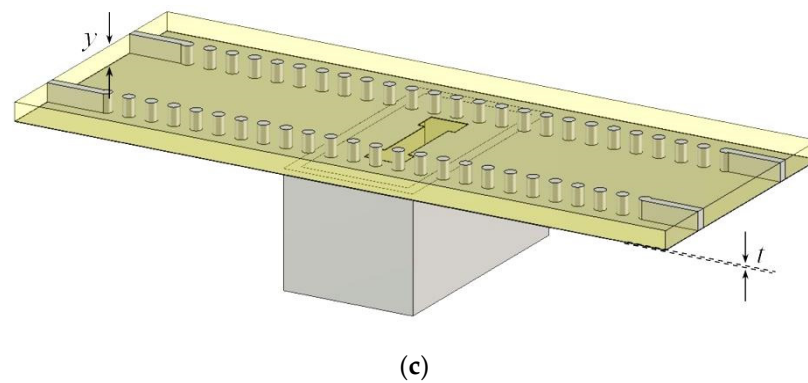


Figure 1. Unmatched RWG-to-SIW power divider: (a) Top view, (b) Bottom view, (c) 3D view.

Similarly to [8,9], the SIW is modeled as a dielectric-filled RWG with equivalent width a_e and same height. The slot dimensions are selected so as to guarantee an input port matching of at least 3 dB in the absence of matching elements. A 2:1 via hole pitch-to-diameter ratio is chosen for reliable manufacturing. Rogers RT5880 substrate, with a dielectric constant $\epsilon_r = 2.2$ and $\tan\delta = 0.001$, is adopted to minimize dielectric losses. Other substrate parameters are the height $y = 1.575$ mm and the metal thickness $t = 17$ μm , though this parameter is increased to 45 μm in the design to account for the via hole metallization process. The design center frequency is set to 12.5 GHz and simulation bandwidth is between 10 and 15 GHz, which is the typical operating frequency range for a WR-75 waveguide. The power divider geometrical parameters and initial scattering parameter are reported in Table 1 and Figure 2, respectively. For reasons of symmetry, scattering parameter S_{31} is omitted.

Table 1. Unmatched RWG-to-SIW power divider geometrical parameters.

Parameter	Description	Value (mm)
a	SIW width	12.500
a_e	Equivalent RWG width	11.865
d	Via hole diameter	1.000
p	Via hole pitch	2.000
y	Substrate height	1.575
t	Metal thickness	0.045
sl	Slot length (vertical)	10.350
sh	Slot length (horizontal)	3.300
sw	Slot width	2.100
wa	RWG width	19.050
wb	RWG height	9.525

The poor return loss performance clearly makes this device unsuitable for hybrid BFNs to be utilized in large planar arrays. This is due to the fact that the equivalent load connected to the RWG is characterized by a very low impedance, which tends to a short circuit as the substrate height becomes smaller.

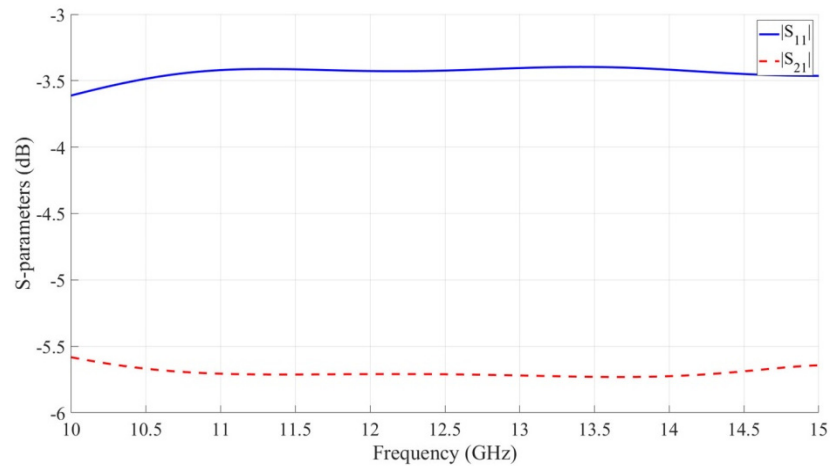


Figure 2. Unmatched RWG-to-SIW power divider simulated scattering parameters.

In the RWG a multi-section impedance matching network is realized by a number of symmetric E-plane irises. In this way, a direct connection between the RWG and the SIW is possible with no need for additional printed circuit elements, thus making this solution particularly convenient.

A constant width $w = 1$ mm is set for all irises with blending radius $br = 1.25$ mm for a low-cost computer numerical control (CNC) machining, as illustrated in Figure 3.

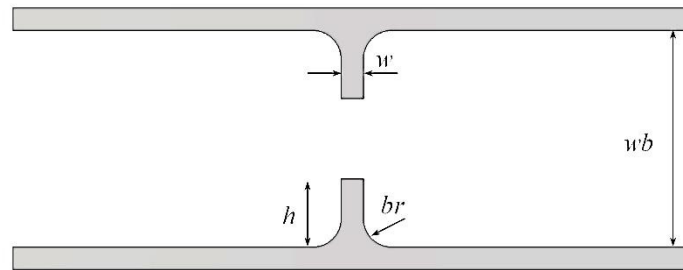


Figure 3. RWG symmetric E-plane iris (E-plane cross-sectional view).

The single iris is modeled with an accurate two-parameter equivalent circuit obtained through a number of full-wave simulations, providing a reliable representation of the iris scattering parameters over an extended bandwidth with respect to the traditional shunt capacitance model [10,11]. The adopted equivalent circuit, consisting of a shunt LC resonator and two symmetrical transmission lines, is shown in Figure 4.

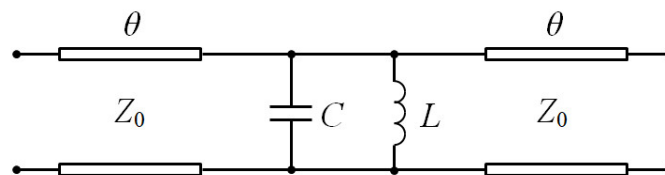


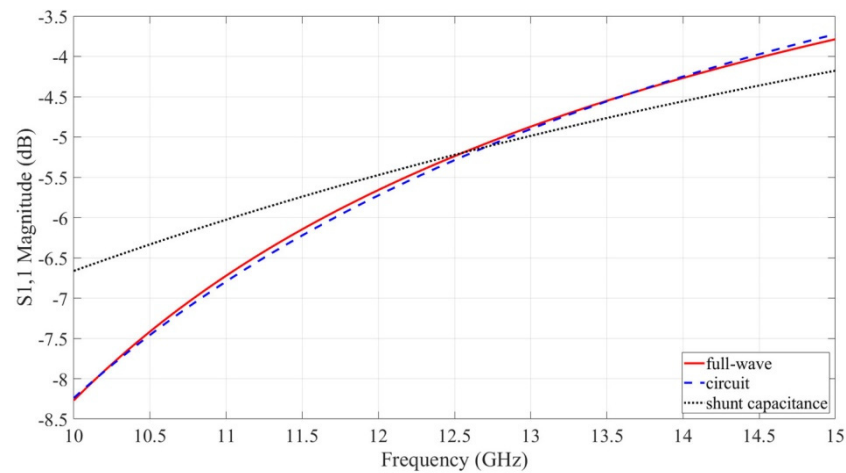
Figure 4. RWG symmetric E-plane iris equivalent circuit.

The transmission line characteristic impedance Z_0 is normalized, while the electrical length θ allows for a fine-tuning of the transmission coefficient phase. The model only depends on the iris height h , which is swept from 0.5 mm to 4.5 mm with a step of 0.5 mm. For each of the nine simulated configurations, a wideband scattering parameters fitting is performed, acting on the three circuit element values C , L , and θ , as in [12]. The fitting procedure results are listed in Table 2.

Table 2. Equivalent circuit parameters for each iris configuration.

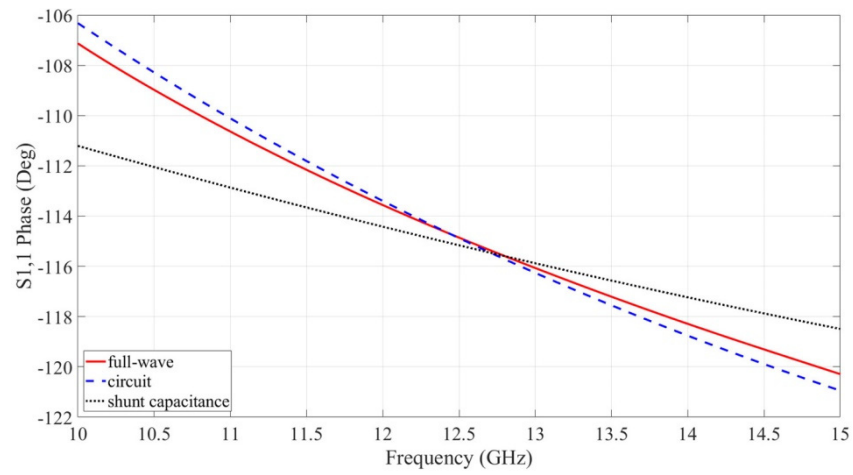
Iris Height (mm)	C (pF)	L (pH)	θ (deg)
0.50	1.776	314.162	−0.512
1.00	3.838	165.103	−1.526
1.50	6.438	100.696	−2.192
2.00	10.131	63.611	−2.765
2.50	14.894	44.643	−3.374
3.00	22.089	29.057	−4.039
3.50	31.240	22.417	−4.537
4.00	49.427	14.315	−5.198
4.50	110.015	6.473	−5.883

To highlight the effectiveness of the proposed equivalent circuit with respect to the standard shunt capacitance model, full-wave and circuit scattering parameters for a generic iris geometry are compared in Figure 5, resulting in a very good agreement over a 40% fractional bandwidth (FBW).

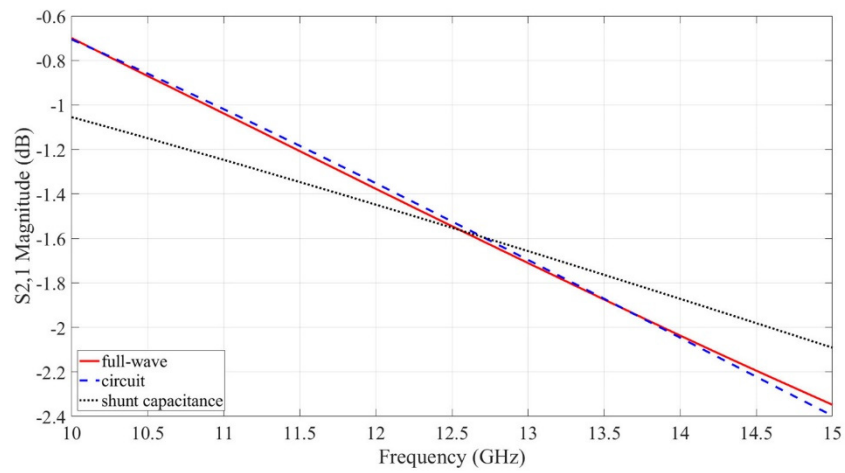


(a)

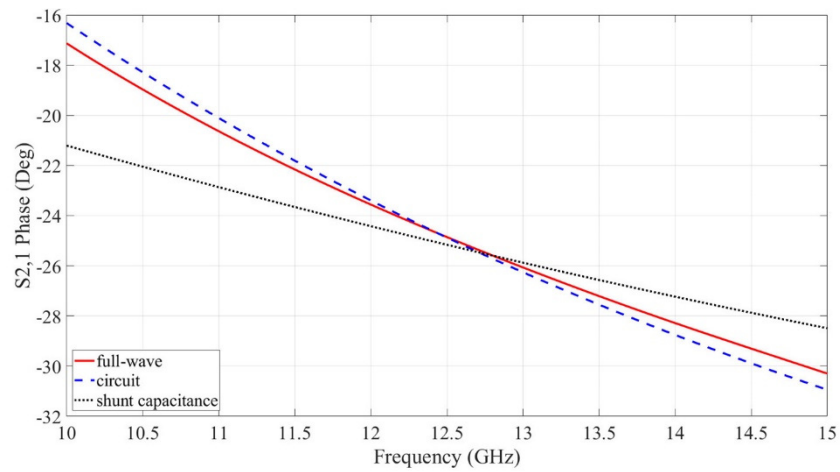
Figure 5. Cont.



(b)



(c)



(d)

Figure 5. RWG symmetric E-plane iris scattering parameters for $h = 3.0$ mm: (a) $|S_{11}|$, (b) $\angle S_{11}$, (c) $|S_{21}|$, (d) $\angle S_{21}$.

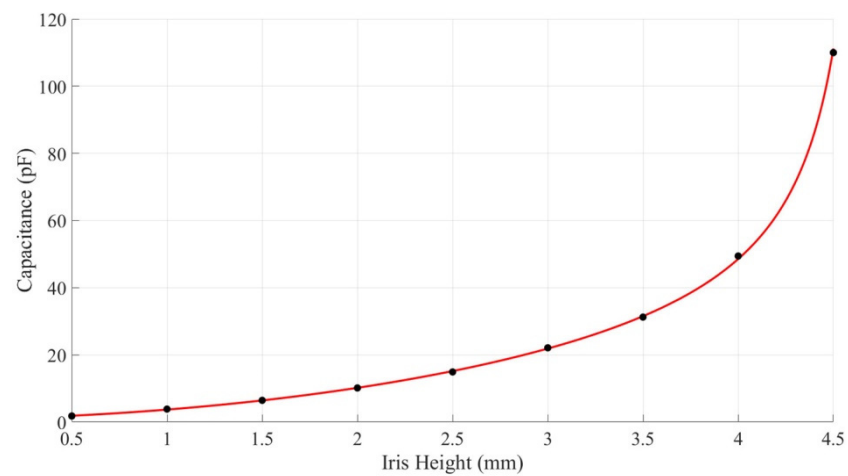
To obtain an accurate model for any value of the iris height in the considered range, a least-squares interpolation is performed, adopting the following fitting functions for C , L and θ :

$$C(h) = \frac{c_3 h^3 + c_2 h^2 + c_1 h + c_0}{h - wb/2} \quad (1)$$

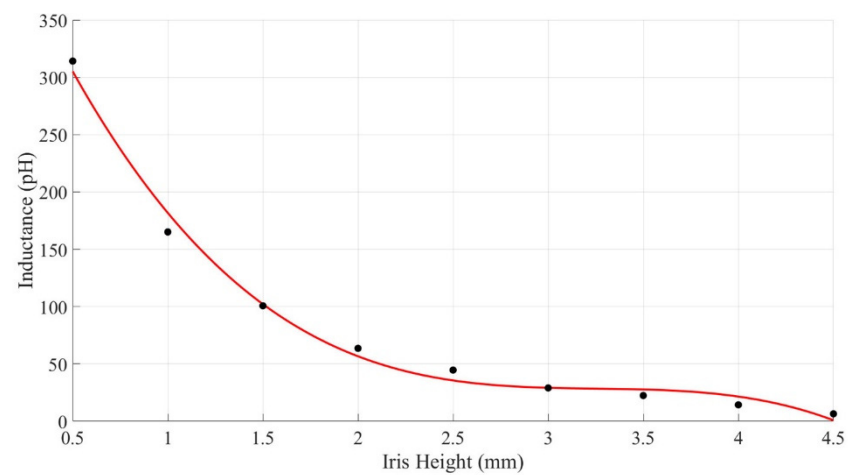
$$L(h) = l_3 h^3 + l_2 h^2 + l_1 h + l_0 \quad (2)$$

$$\theta(h) = t_3 h^3 + t_2 h^2 + t_1 h + t_0 \quad (3)$$

Third order polynomials are selected as a trade-off between interpolation accuracy and computational cost, with the only exception of Equation (1), which is a rational function with first-degree denominator to properly describe the case of an iris with $h = wb/2$. The obtained interpolating functions and the associated coefficients are shown in Figure 6 and Table 3, respectively.

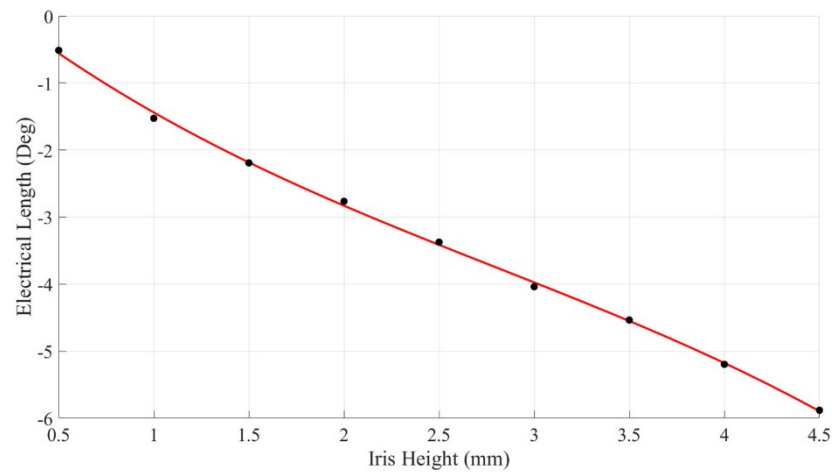


(a)



(b)

Figure 6. Cont.



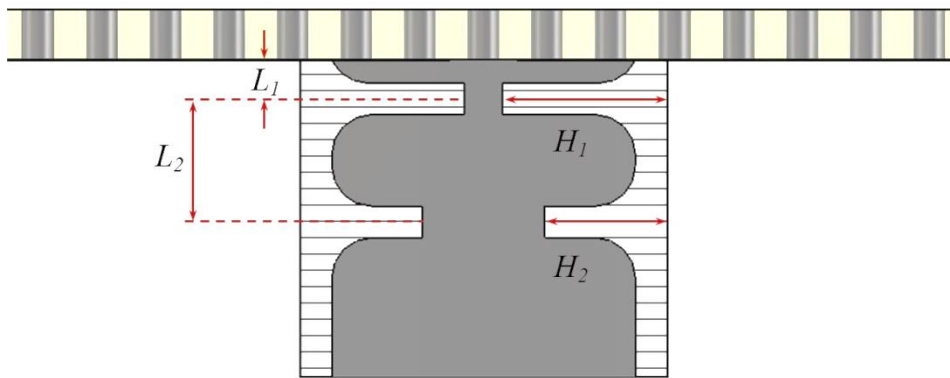
(c)

Figure 6. Circuit parameters fitting values (black dots) and interpolating functions (solid line): (a) C , (b) L , (c) θ .

Table 3. Interpolation coefficients for the circuit elements C , L , and θ .

Interpolation Coefficients			
c_3	c_2	c_1	c_0
1.364	-6.294	-4.894	-4.044
l_3	l_2	l_1	l_0
-12.950	126.500	-413.900	482.100
t_3	t_2	t_1	t_0
-0.051	0.428	-2.319	0.503

A preliminary design of the multi-section matching network at the RWG-to-SIW T-junction input can now be performed. With the aim of maximizing the 20-dB return loss bandwidth, three different designs are carried out with the above-mentioned circuit modeling, employing one, two, and three irises, respectively. The power divider in the case of a two-iris matching network is shown in Figure 7a, and its equivalent circuit is given in Figure 7b. The transmission lines are dimensioned to model the RWG sections in between each iris, with $Z_0 = 1$ and electrical lengths $\theta_i = \beta L_i$, where β is the propagation constant [10,11] and L_i are the sections physical lengths.



(a)

Figure 7. Cont.

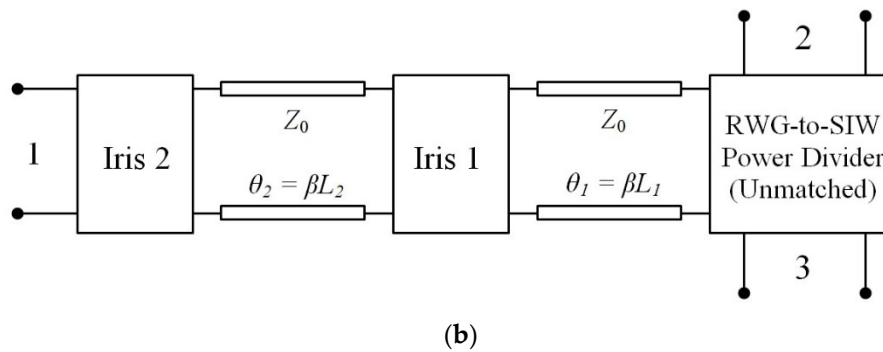


Figure 7. RWG-to-SIW power divider with two-section matching network: (a) Physical realization (E-plane cross-sectional view), (b) Equivalent circuit.

It is worth mentioning that the proposed design approach allows a quasi-instantaneous first dimensioning of the waveguide circuit, though its accuracy is limited by the fact that only the fundamental mode is considered in the model. A full-wave verification is therefore necessary. The synthesized geometries are provided in Table 4, while circuit-analysis and full-wave simulation scattering parameters are compared in Figure 8.

Table 4. RWG-to-SIW power dividers geometrical parameters.

Parameter	Description	Design 1 Value (mm)	Design 2 Value (mm)	Design 3 Value (mm)
H_1	First iris height	3.393	3.907	4.050
H_2	Second iris height	-	2.525	3.318
H_3	Third iris height	-	-	1.931
L_1	First iris distance	2.360	1.793	1.565
L_2	Second iris distance	-	4.661	3.836
L_3	Third iris distance	-	-	5.654

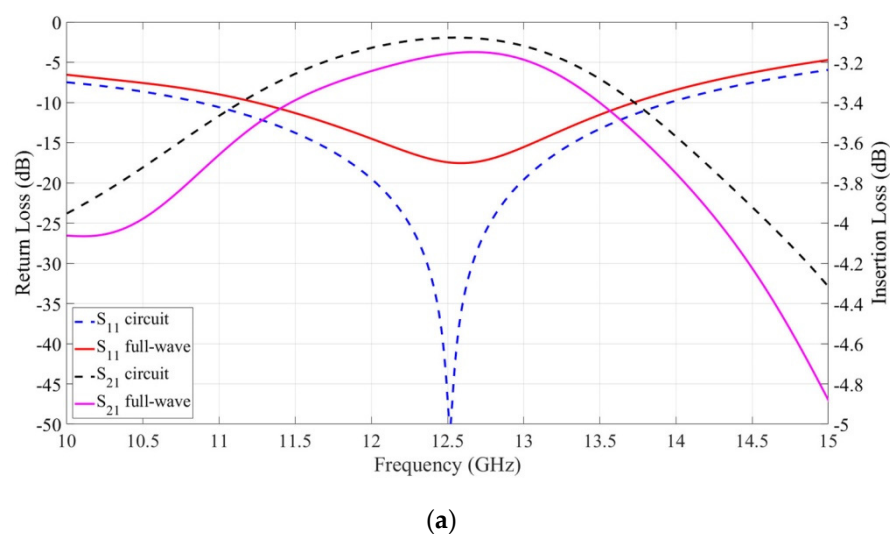


Figure 8. Cont.

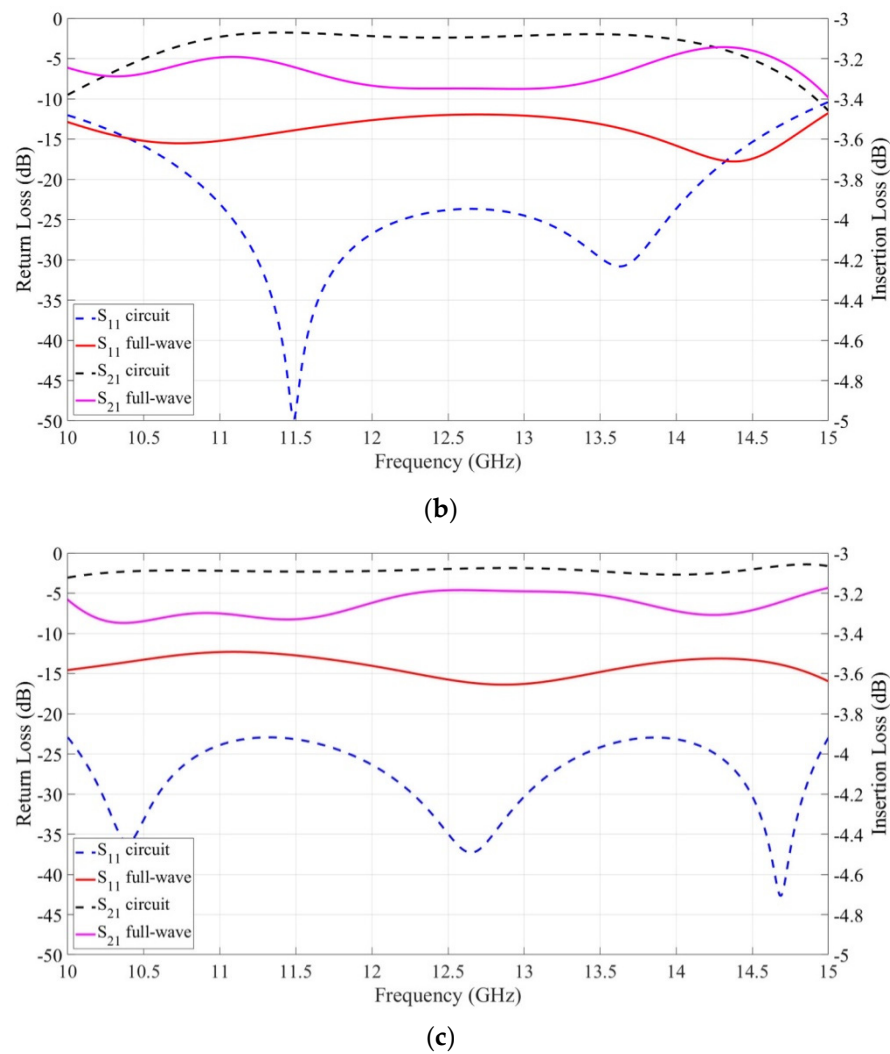
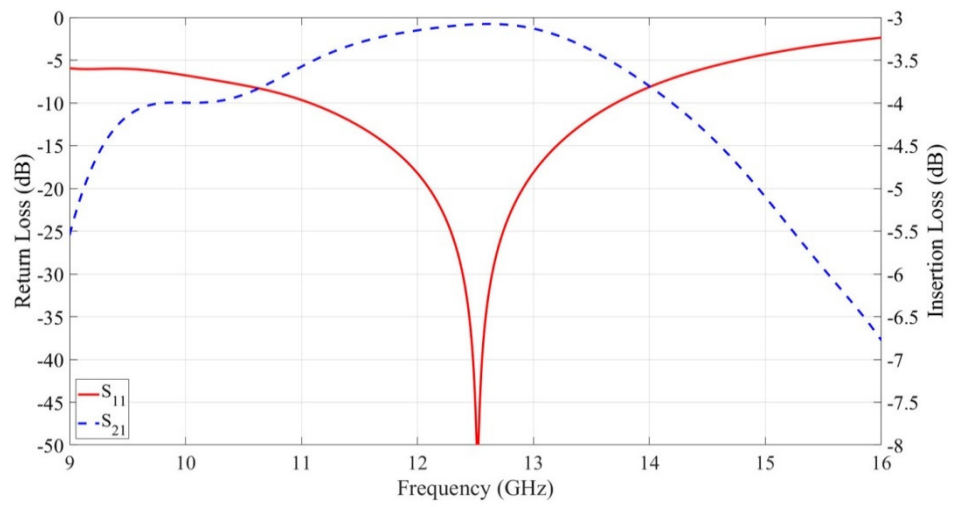


Figure 8. RWG-to-SIW power dividers: Comparison between circuit and full-wave analysis: (a) One-section matching network, (b) Two-section matching network, (c) Three-section matching network.

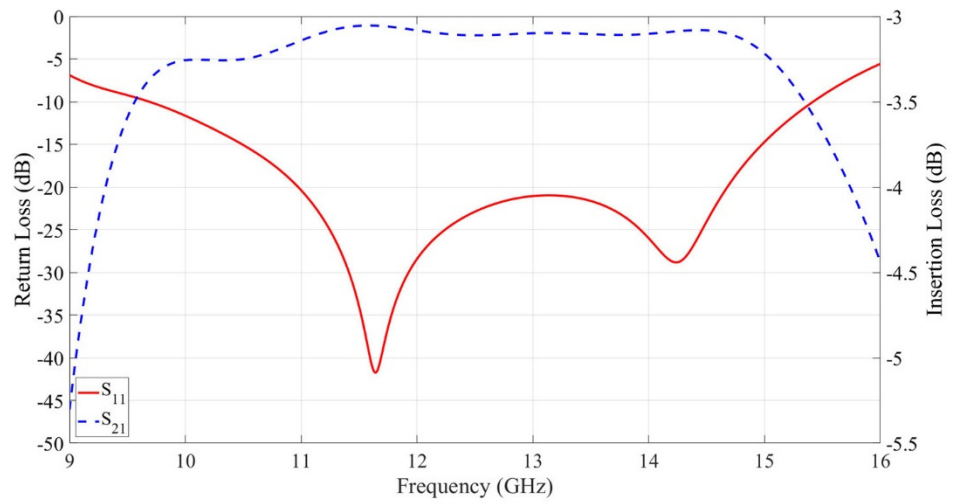
As expected, full-wave results show some deviations from circuit simulations, and further full-wave optimization is needed. For all cases, however, convergence is reached in a few iterations with a local optimization. The final geometrical parameters and simulated performance are shown in Table 5 and Figure 9, respectively. Fractional bandwidths of 6.48%, 28.89%, and 40.93% are obtained in the three cases. Insertion loss is always better than 0.17 dB in the operative frequency ranges.

Table 5. Optimized RWG-to-SIW power dividers geometrical parameters.

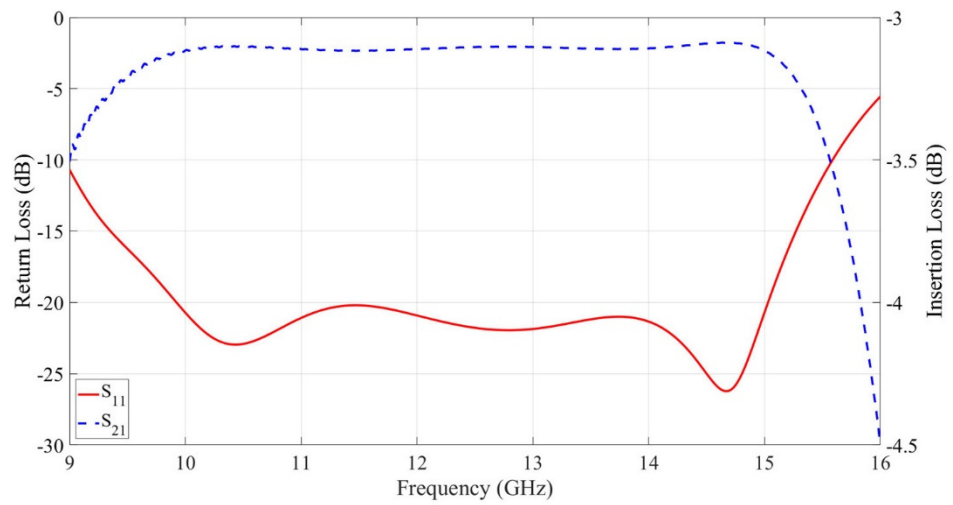
Parameter	Description	Design 1 Value (mm)	Design 2 Value (mm)	Design 3 Value (mm)
H_1	First iris height	3.647	4.160	4.212
H_2	Second iris height	-	2.837	3.414
H_3	Third iris height	-	-	1.667
L_1	First iris distance	2.064	1.209	1.237
L_2	Second iris distance	-	3.887	3.494
L_3	Third iris distance	-	-	5.674



(a)



(b)



(c)

Figure 9. Optimized RWG-to-SIW power dividers simulated scattering parameters: (a) One-section matching network, (b) Two-section matching network, (c) Three-section matching network.

It is worth noting that the three-section RWG-to-SIW power divider exhibits a 5-GHz bandwidth around 12.5 GHz with a total thickness of just 11.5 mm ($L_1 + L_2 + L_3 + w/2$), thus making this solution extremely compact.

To assess the effectiveness of the proposed solutions, a comparison with referenced works [4–7] is presented in Table 6. The SIW height y (i.e., the substrate thickness) is related to the cutoff wavelength $\lambda_c = 2a_e\sqrt{\epsilon_r}$ as follows:

$$r = \frac{y}{\lambda_c} \quad (4)$$

Table 6. Comparison with state-of-the-art solutions.

Reference	[4]	[5]	[6]	[7]	This Work (1)	This Work (2)	This Work (3)
f_0 (GHz)	78.60	29.85	12.53	32.25	12.50	12.83	12.48
ϵ_r	2.20	3.55	2.20	2.20	2.20	2.20	2.20
a (mm)	2.24	4.80	11.00	4.80	12.50	12.50	12.50
y (mm)	0.787	0.787	1.000	0.787	1.575	1.575	1.575
a_e (mm)	2.00	4.54	10.36	4.60	11.87	11.87	11.87
λ_c (mm)	5.93	17.11	30.73	13.65	35.21	35.21	35.21
r (%)	13.26	4.60	3.25	5.76	4.47	4.47	4.47
$BW_{20\text{dB}}$ (MHz)	9880	701	350	11,500	810	3707	5108
FBW (%)	12.57	2.35	2.79	35.66	6.48	28.89	40.93
F	0.95	0.51	0.86	6.18	1.45	6.45	9.15
F/F [7]	0.15	0.08	0.14	1.00	0.23	1.04	1.48

The achievable bandwidth is observed to be linearly dependent on the ratio r . For this reason, in order to perform a fair comparison between the various state-of-the-art solutions, the fractional bandwidth performance is normalized by introducing a merit factor F defined as:

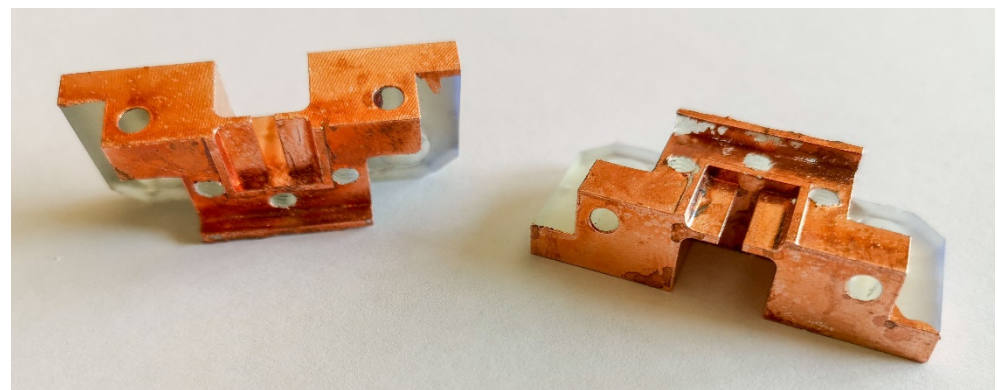
$$F = \frac{FBW}{r} \quad (5)$$

Table 6 refers to simulated results only, so that biasing due to manufacturing errors in fabricated prototypes is not considered. In order to highlight an actual bandwidth improvement, each merit factor is related to the highest state-of-the-art merit factor, corresponding to reference [7].

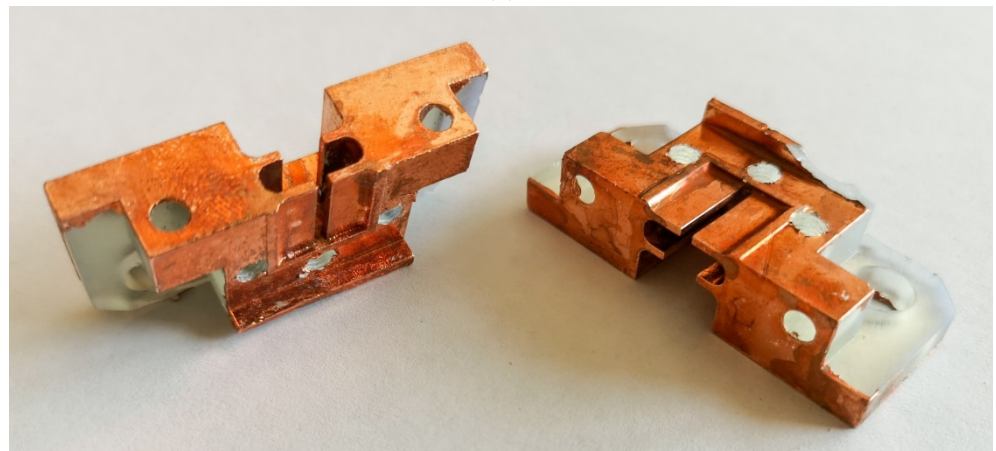
The third design proposed in this work exhibits the best overall performance, exceeding the state of the art by almost 15% in terms of FBW and 50% in terms of F . With this respect, however, also the second design achieves a remarkable merit factor.

3. Power Divider Manufacturing and Test

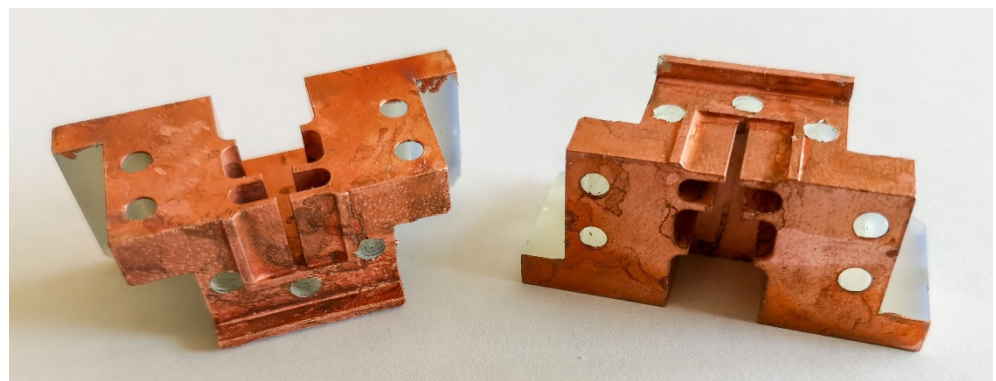
The three power dividers are prototyped to validate simulation results. The three RWG multi-section matching networks are manufactured with a Formlabs Form 2 SLA printer and metalized with a two-step process consisting of silver painting followed by electrolytic copper deposition. The open waveguide sections are shown in Figure 10 to visualize internal details.



(a)



(b)



(c)

Figure 10. Waveguide multi-section matching networks: (a) One section, (b) Two sections, (c) Three sections.

In particular, each structure is divided into two symmetrical halves so as to ease the silver paint deposition. The two parts and a separate copper rod are immersed in a commercial copper sulfide solution. Electroplating takes place when the cathode of a DC power supply is connected through copper wires to the inner surfaces of the two split waveguides, while the anode is connected to the copper rod. A 100 mA current guarantees a uniform copper deposition, limiting defects such as spikes and unwanted surface roughness. Screws are used to guarantee good electrical contact between the two parts. The adopted manufacturing process, detailed in [13], minimizes cost and prototyping time, while ensuring good performance, as already verified in [14–16]. The SIW is manufactured with standard PCB technology and joint to a mechanical supporting structure integrating the RWG section by means of six mounting screws. A wideband

SIW-to-GCPW transition is designed according to [17]. The transition geometry, simulated performance, and geometrical parameters are reported in Figure 11 and Table 7, respectively. GCPW feeding sections for the two output ports are preferred over microstrip lines due to a reduced radiation loss and a limited influence on the RWG structure. Two Southwest Microwave 2.92-mm jack (female) end-launch solder-less connectors model 1092-03A-5 are employed to feed the GCPW lines.

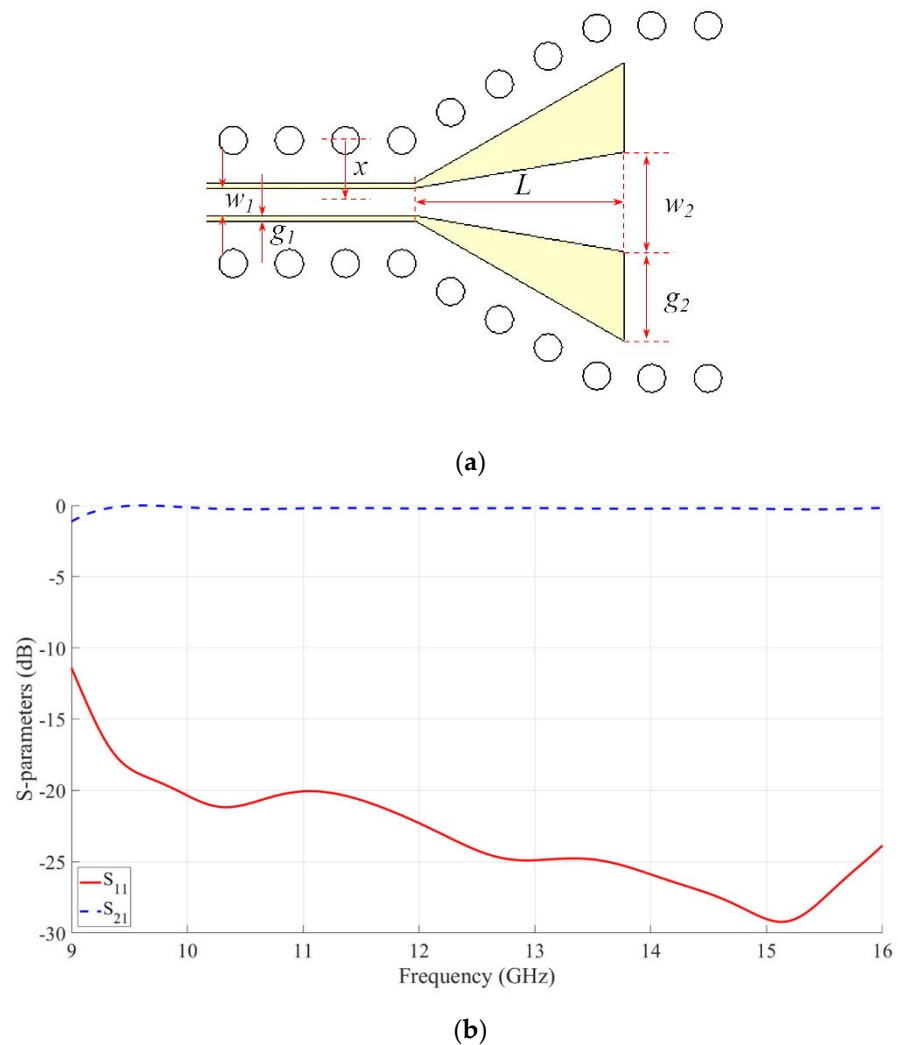


Figure 11. SIW-to-GCPW transition: (a) Geometry, (b) Simulated scattering parameters.

Table 7. SIW-to-GCPW transition geometrical parameters.

Parameter	Description	Value (mm)
w_1	GCPW initial width	1.000
w_2	GCPW final width	3.530
g_1	GCPW initial gap	0.180
g_2	GCPW final gap	3.157
L	Taper length	7.387
x	Line-via distance	2.180

The RWG input port is connected to a commercial coaxial-to-WR-75 transition, whose scattering parameters are reported in Figure 12 in a back-to-back configuration to verify its input matching in the frequency range of interest. The assembled prototype is shown in Figure 13. In particular, a 3D-printed rigid plate on top of the SIW circuit is clearly visible.

This element is introduced to uniformly distribute the pressure on the PCB in order to further improve the electrical contact with the RWG section.

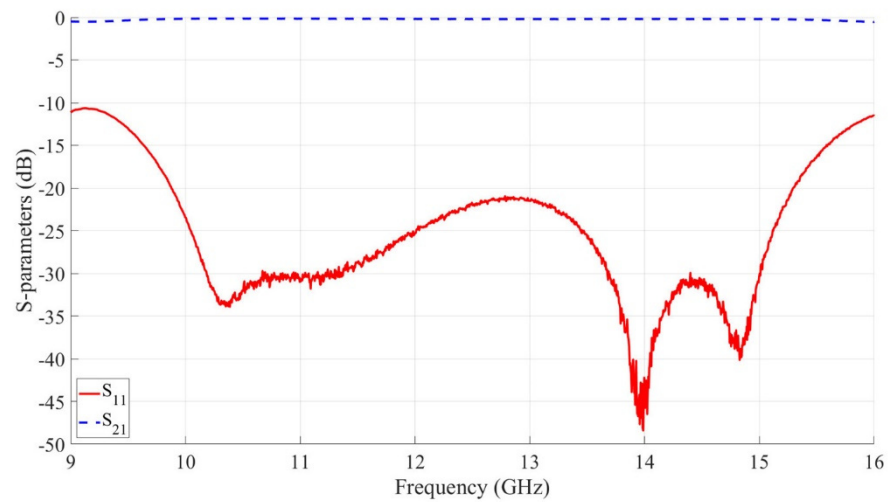


Figure 12. Coaxial-to-WR-75 transition measured scattering parameters (back-to-back configuration).

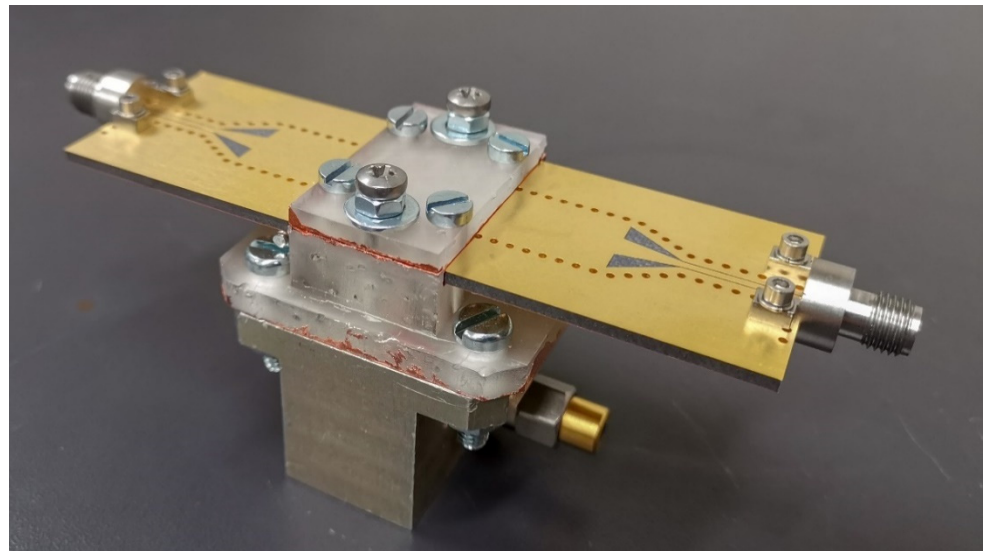
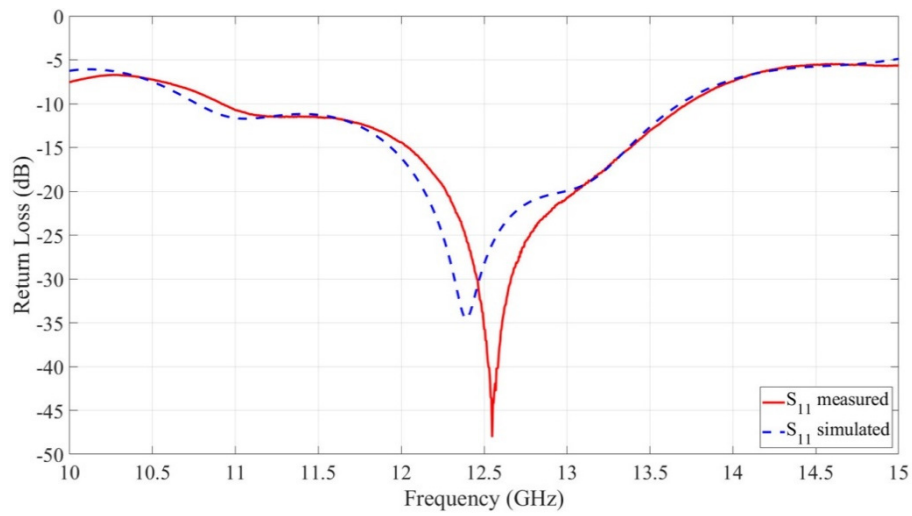
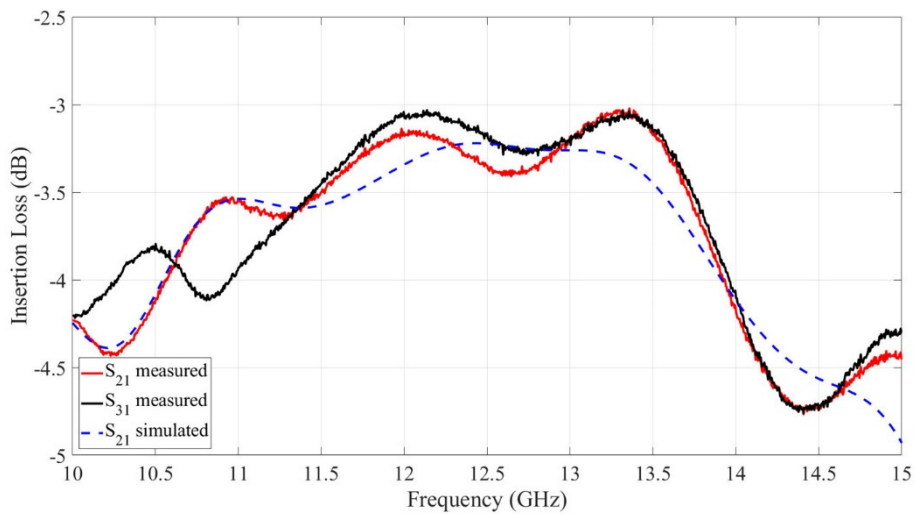


Figure 13. RWG-to-SIW power divider prototype.

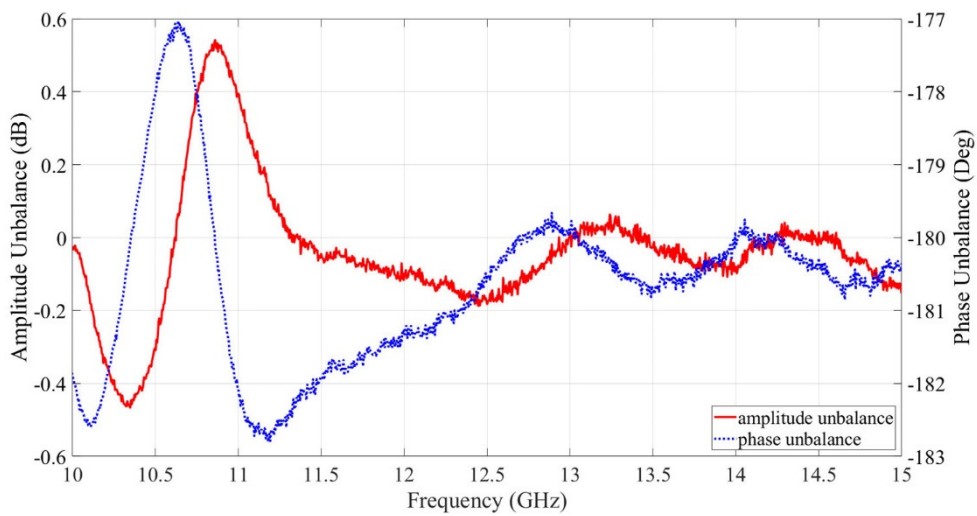
The three power dividers are tested with an Agilent N5230A vector network analyzer using the Short-Open-Load-Through (SOLT) calibration technique. Measured scattering parameters are reported in Figures 14–16 and compared to simulated results, the latter including GCPW-to-SIW transition sections. Physical properties of copper conductivity and surface roughness are taken into account in the simulation. In particular, an estimated metallic roughness of the order of $5\ \mu\text{m}$ contributes to deteriorating copper conductivity. Similarly to [18], the effects of the coaxial connectors are de-embedded. According to measured data provided by the manufacturer, an estimated insertion loss of 0.4 dB at 10 GHz and 0.5 dB at 15 GHz is considered.



(a)

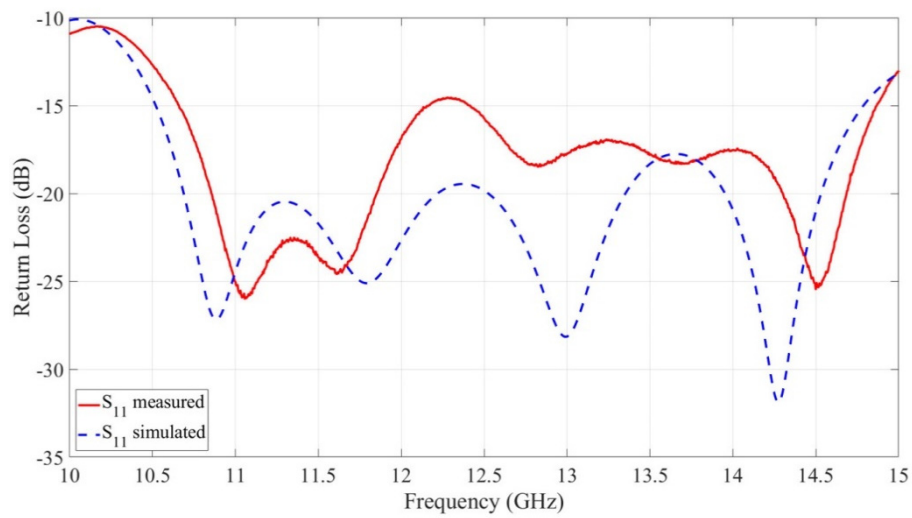


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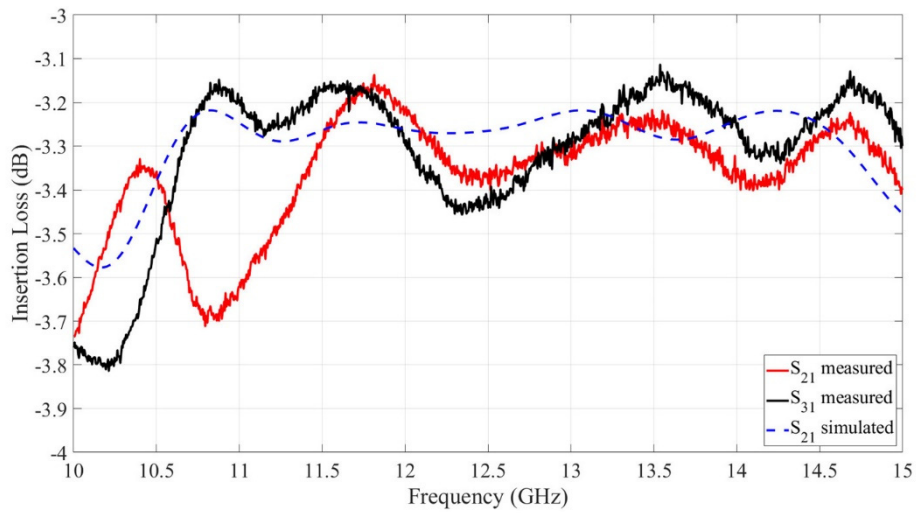


(c)

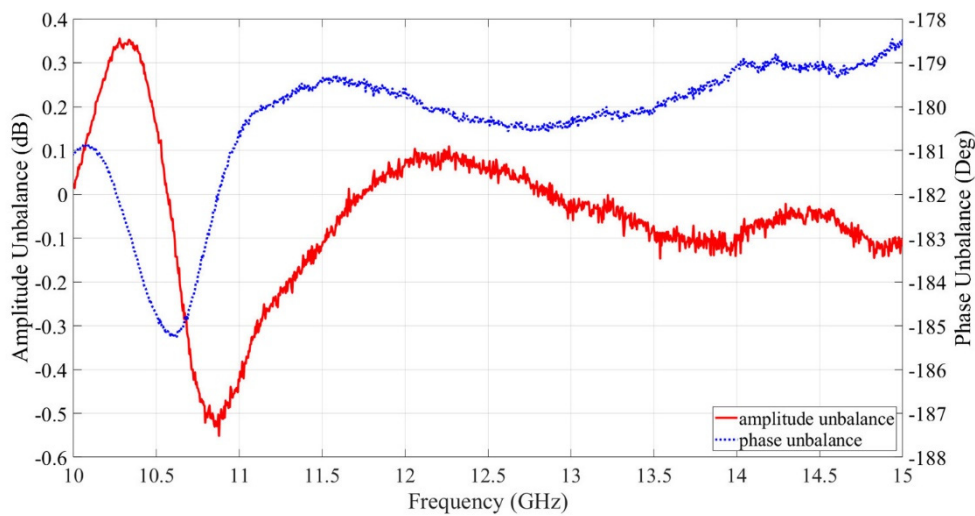
Figure 14. One-section RWG-to-SIW power divider measured results: (a) S_{11} , (b) S_{21} , (c) Amplitude and phase unbalance.



(a)



(b)



(c)

Figure 15. Two-section RWG-to-SIW power divider measured results: (a) S_{11} , (b) S_{21} , (c) Amplitude and phase unbalance.

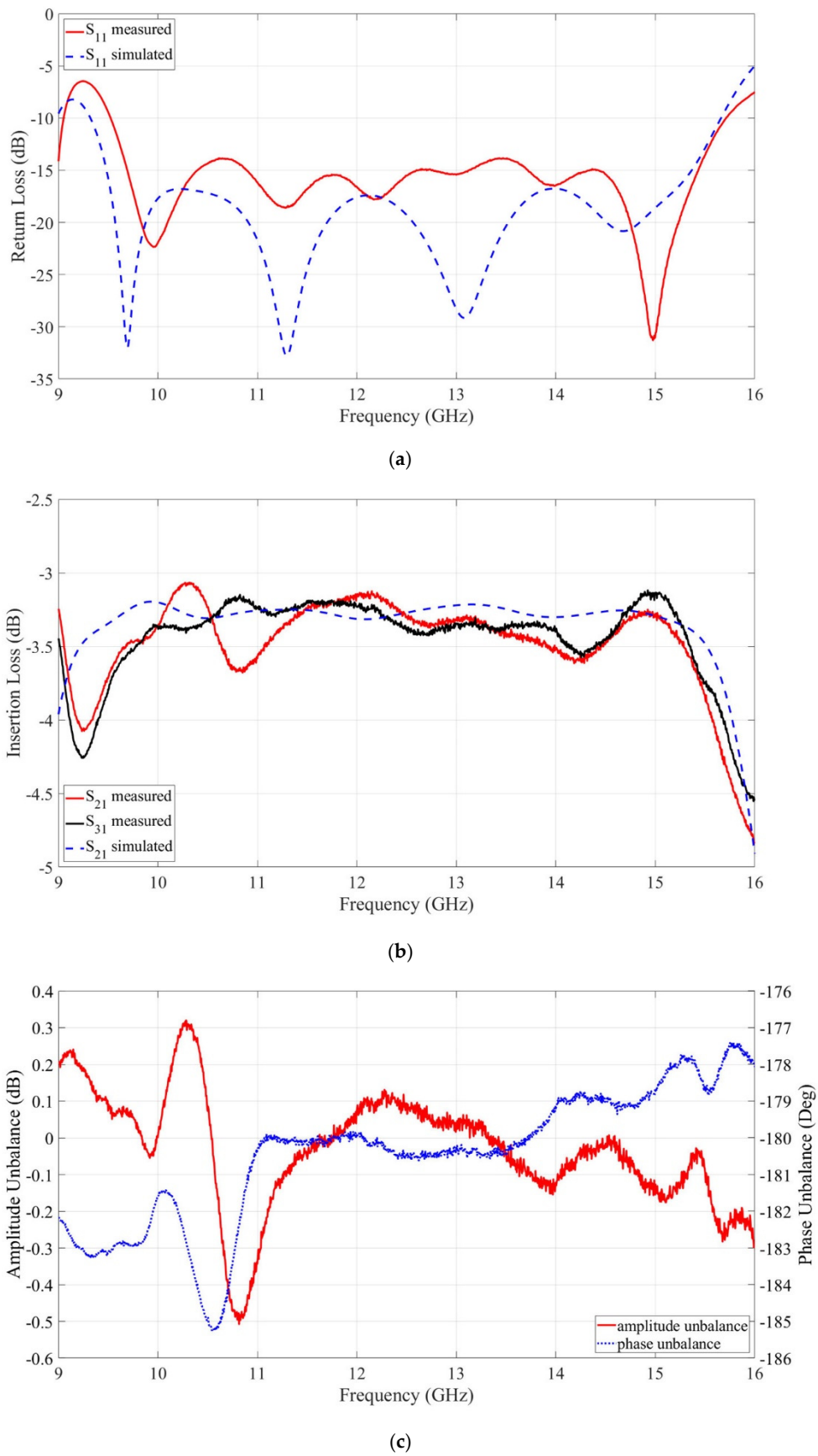


Figure 16. Three-section RWG-to-SIW power divider measured results: (a) S_{11} , (b) S_{21} , (c) Amplitude and phase unbalance.

Measured results show an overall good agreement with simulations, though small frequency shifts toward higher frequencies, differences in the return loss levels, and increased insertion loss can be observed. Deviations from simulated results are mainly caused by the additive manufacturing 0.1-mm fabrication tolerance, as well as misalignment errors and plastic deformation in the assembly. It is worth mentioning that simulation results derive from an electromagnetic design, which accounts for the effects of the SIW-to-GCPW output transitions but excludes the contributions from the coaxial-to-WR-75 input transition, which is assumed negligible with respect to the validation of the manufactured devices. Small differences in the insertion loss are to be imputed to a suboptimal electrical contact between the SIW and RWG sections as well as to the manufacturing tolerance. Nevertheless, very small amplitude and phase unbalances can be noticed in the frequency ranges of interest, as shown in Figures 14c, 15c and 16c. Industrial-grade manufacturing with aluminum CNC machining would indeed lead to an excellent agreement between simulations and measurements, though considerably increasing costs and prototyping time. In conclusion, the adopted in-house fabrication process is considered a good compromise to validate the performance for the three proof-of-concept prototypes and adequate to demonstrate the feasibility and effectiveness of the proposed solution.

4. Conclusions

This work presents a broadband RWG-to-SIW E-plane T-junction, a key device in all hybrid RWG-SIW architectures for phased arrays antennas. Despite the choice of a low-profile SIW substrate, wideband performance has been obtained thanks to a multi-section RWG matching network consisting of a number of symmetric E-plane irises. An equivalent circuit has been extracted to describe the capacitive iris performance over an extended frequency range, considerably improving the traditional single-parameter model and significantly reducing the computational cost of the matching network design when compared to a pure full-wave procedure. Simulated 20-dB return loss fractional bandwidths of 6.48%, 28.89%, and 40.93% have been achieved, respectively, for the one-iris, two-iris, and three-iris versions for a SIW height equal to 4.5% of the cutoff wavelength. Such performance is comparable or exceeds the state of the art. Three proof-of-concept prototypes have been fabricated with PCB and additive manufacturing technologies. Good agreement between simulations and measurements validates the design procedure.

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