electronics

MDPI

Article

Reference Power Supply Connection Scheme for Low-Power CMOS Image Sensors Based on Incremental Sigma-Delta Converters

Luis Miguel Carvalho Freitas [1,2,*] and Fernando Morgado-Dias [2]

[1] AMS Sensors Portugal, Madeira Tecnopolo 2, 9020-105 Funchal, Portugal
[2] ITI/LARSyS/Madeira Interactive Technologies Institute, University of Madeira, Caminho da Penteada, 9020-105 Funchal, Portugal; morgado@uma.pt
* Correspondence: miguel.freitas@ams.com

Abstract: Modern Complementary Metal-Oxide-Semiconductor (CMOS) image sensors, aimed to target low-noise and fast digital outputs, are fundamentally based on column-parallel structures, jointly designed with oversampling column converters. The typical choice for the employed column converters is the incremental sigma-delta structures, which intrinsically perform the correlated multiple sampling, creating an averaging effect over the system thermal noise when used in conjunction with 4T-pinned pixels. However, these types of column converters are known to be power-hungry, especially if the imaging device needs to target high frame rate levels as well. In this sense, the aim of this paper was to address the excess of power dissipation problem that arises from image sensors while employing oversampling high-order incremental converters, by means of using a different connection scheme to supply and to drive the required reference signals across the image sensor on-chip column converters. The proposed connection scheme revealed to be fully functional with no unwanted artifacts in the imager output response, allowing it to avoid 20% to 50% of the power dissipation, relative to the classical on-chip references generation and driving method. Furthermore, this solution allows for a much less complicated and less crowded printed circuit board (PCB) system.

Keywords: CMS; ADC; low-power; CMOS; low-noise; high frame-rate; CIS; image sensors

Citation: Carvalho Freitas, L.M.; Morgado-Dias, F. Reference Power Supply Connection Scheme for Low-Power CMOS Image Sensors Based on Incremental Sigma-Delta Converters. *Electronics* **2021**, *10*, 299. https://doi.org/electronics10030299

Academic Editor: Kamal EI-Sankary
Received: 22 December 2020
Accepted: 21 January 2021
Published: 27 January 2021

1. Introduction

Recent developments with regards to the optimization of the column readout circuits, in parallel with the improvements on the pixel design, namely sensors using pinned-pixels, in-pixel amplification, and pixel-process optimization, have led to the appearance of a new class of CMOS image sensors (CIS) that can detect and manage light at extremely low levels of illumination. Some of them are even capable of detecting photons and are usually called quanta image sensors (QIS). Additionally, there are also devices that not only target low-noise imaging but also target high frame rate (FR) specification. The joint low-noise and high FR specifications lead to CIS devices capable of fitting in almost any scientific and industrial application, making them valuable pieces of hardware for the later mentioned applications, due to the design difficulties that occurs precisely from combining the low-noise and high-speed features in the same imager.

However, to obtain a truly competitive and remarkable device for high-end applications, the sensor resolution and the power consumption need to be reduced and added to the equation. By adding the spatial resolution issue to the subject, it is still possible to end with a competitive and scalable imaging concept, at virtually any target resolution; such a CIS development requires one to adopt a completely different design approach, namely the design with a 3D-stacking process.

For the 2D flat development (relative to both the low-noise and high FR features) or the 3D stacking design (including a high resolution to both the low-noise and FR features),

the low-noise and high FR features are in conflict with the mandatory requirement of a low-power specification. The FR specification makes the readout circuits exhibit a higher bandwidth, hence requiring a considerable amount of current. Furthermore, high-order incremental sigma-delta (ISD) analog-to-digital converters (ADCs) usually need to be employed to make the imaging devices meet high values of conversions per second [1], therefore being in-line with the expected sensors FR.

Sigma-delta converters are known to be capable of reaching deep converter resolutions, while also being reasonably fast (or simply being fast), depending on the modulator order and the class of the modulator design [1]. In addition to this, they are also suitable for low-noise applications [2] due to their intrinsic nature of shaping circuit noise, enabling low-noise contribution to the system, given their ability to average any input thermal noise signal, by oversampling the input or oversampling any input-referred noise signal. This effect is known as correlated multiple sampling (CMS) when applied in the CIS field and when used together with low-noise 4T-pinned pixels, namely the pixels based on pinned photo-diodes (PPD).

Therefore, there is a cross-dependency function among the required features, since to meet both low-noise and high FR, it interferes or sacrifices the device power consumption [1], which worsens the higher the sensor spatial resolution is. In this sense, it seems logical that without a compromise between all the relevant features, the device will not be of much value for high-end applications, such as in scientific and industrial cases.

The present research project focused on low-noise design, high FR, and high-resolution CIS devices, targeted for a possible future development with a 3D stacked CIS implementation in mind, to target high-end applications such as for industrial and scientific areas. In this sense, this paper deepens the work from the same authors regarding the CIS test chip development [3,4], as well as both its fabrication and characterization work [5,6]. Its development was aimed to meet the proposed goals, such as going through the system verification; it was also designed, however, for testing some system operation variants, by checking their improvements and their future usage, such as the one that this paper addresses.

The rest of the research paper is organized as follows: Section 2 provides background information and Section 3 provides a sufficiently in-depth discussion of the problem being tackled. Section 4 focuses on the proposed low-power solution being adopted in this test chip for a clear verification. Section 5 addresses the proof-of-concept and the outcomes/results of the fabricated imaging device under the proposed low-power connection scheme, presenting a comparison work with the classical default operation results. Finally, conclusions are presented in Section 6.

2. Background

As indicated briefly in Section 1, image sensors that aim to exhibit extreme low-noise outputs at low-light levels need exceptional readout circuit performances, combined with state-of-the-art low-noise pixels. However, both pixel design and/or process optimization are insufficient in reaching extreme levels of image noise in the dark, driving the design effort mainly to the readout circuits' optimization.

It is commonly found in the literature that to achieve a low-noise pixel/column readout circuit, the CMS technique must be employed [7–10]. Combining the CMS operation with Nyquist-rate ADCs is difficult, if not impractical at all, to do. Instead, oversampling converters are preferred, since these intrinsically perform the necessary and desired multiple sampling effect. Figures 1 and 2 show the simplified readout circuit structure path employing an oversampling ISD converter system and depict the pixel operation under the CMS technique. The association of the intrinsic oversampling operation with the multiple sampling processing method is shown in s 1 as well. The sampling period Ts is related with the ADC clock period, while the global double sampling period Tcds is associated with the converter's conversion time, accounting with the required time for the in-pixel charge-transfer process.

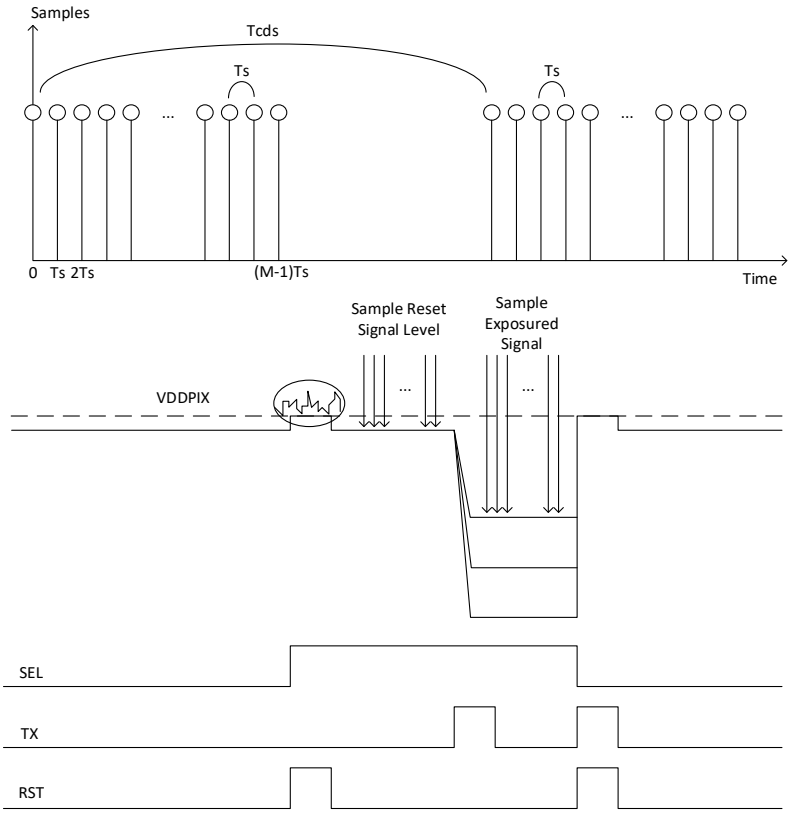

Figure 1. Simplified 4T-pinned pixel correlated multiple sampling (CMS) sampling operation. (**top**) The CMS process from signal processing perspective; (**bottom**) equivalent time domain pixel readout signals and corresponding pixel timing control signals.

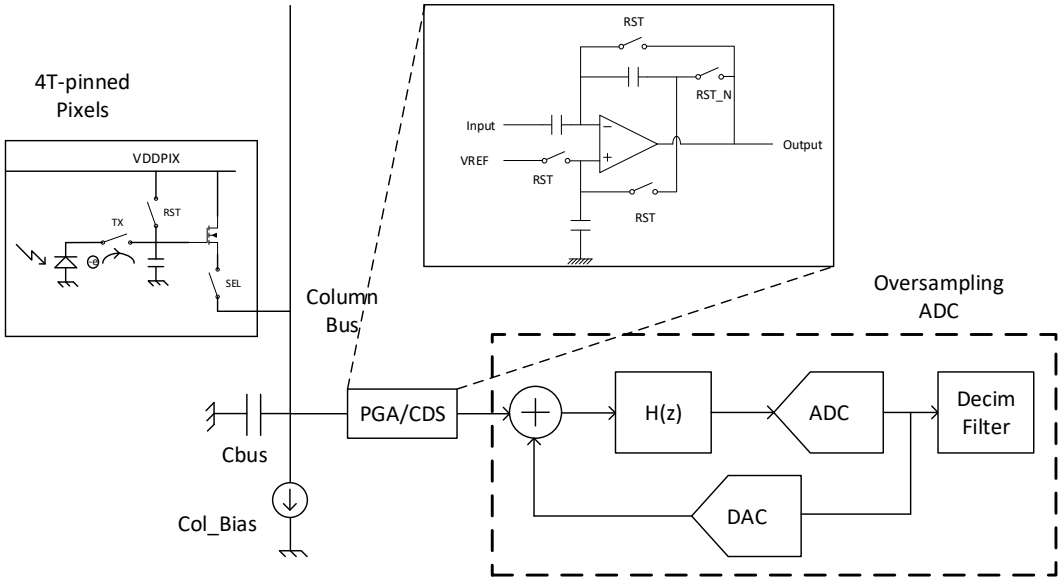

Figure 2. Simplified CMOS image sensors (CIS) entire column readout structure. Additional emphasis to the programmable gain amplifier (PGA)—performing the correlated double sampling (CDS), and to the analog-to-digital converter (ADC) driver circuit implementation—requiring a single-bit built-in digital-to-analog converter (DAC).

The pixels and the readout circuits work as follows: while a specific row of pixels is addressed (with the pixel select—SEL control signal switched-on), first, the pixel reset level (pixel supply-VDDPIX) is readout through the in-pixel source follower (SF). This is

accomplished by issuing the pixel reset-RST control signal. After the reset level is readout, the light-induced signal level can be similarly readout through the column bus, by issuing the TX control signal. The difference between the reset and the light-induced signals, creates the photo-signal information. The photo-signal is then amplified by the PGA/CDS stage (programmable gain amplifier, performing the analog version of the correlated double sampling technique), which in turn the output signal is then converted by the column oversampling signal converters.

The means to take advantage of the multiple sampling effect, while accessing the pixel signals, is to let the oversampling ISD ADC to convert the available steady DC pixel signals (the reset level and the after exposure time: the light-induced signal) while they are available during pixel access time. In this way, the CMS signal operation can take place, allowing less noisy images to be outputted.

The most common experimental low-noise column signal converters employed are the single-bit discrete time (DT) ISD systems. As an example, a 3rd order single-bit DT feed-forward (FF) structure ISD, employed in the test chip fabrication, is depicted in Figure 3. Given their incremental nature, they are similar to the Nyquist-rate operation. It is demonstrated in the literature that they fit reasonably well with column-parallel CMOS imagers [1,11–17].

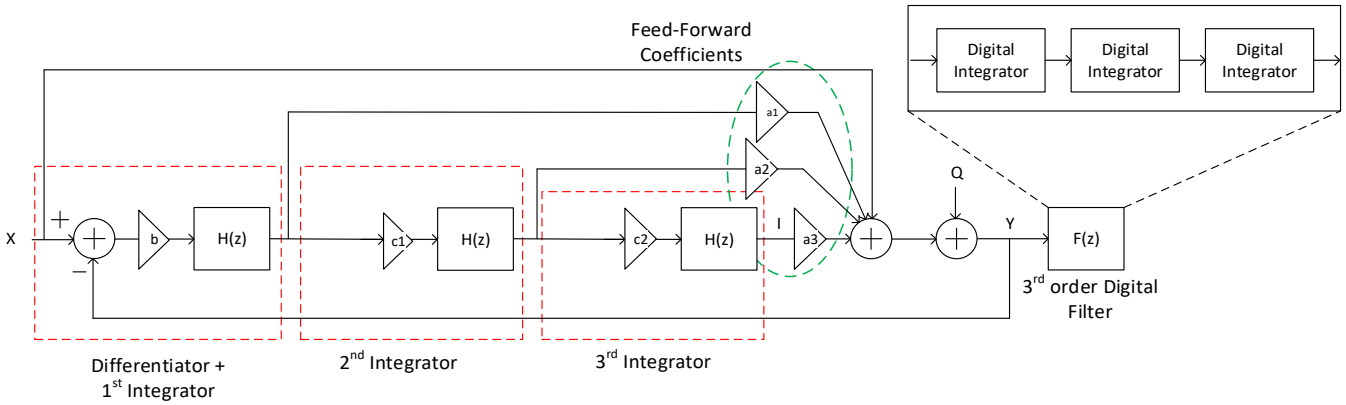

Figure 3. Implemented 3rd order cascade of integrators feed-forward incremental sigma-delta (ISD) column converter system. Additional emphasis to the digital filter implementation, namely three consecutive digital integrators in counting digital data in a row.

The most noteworthy part of such ISD systems is their oversampling characteristic, performing the averaging of the input thermal noise, as Equation (4) suggests. Moreover, ISD ADCs can perform fast conversions when designed with high-order modulators and combined with high-order filters, as Equations (2) and (3) demonstrate.

The issue with their usage lies in getting a stable modulator, and hence having a fully functional ADC system. However, they may be power-hungry systems [5], draining substantial current from the analog supplies. This is of particular importance in case they need to achieve substantially low conversion times; hence, higher-order modulators are required and, therefore, more integrator circuit stages to supply high bandwidth.

Next, the underlying theory is briefly described and how a 3rd order ISD ADC system works in the fabricated test chip CIS. From the time domain circuit analysis, the output of the last integrator can be expressed, after M clock cycles, as [18]:

$$I_{Out}[M] = bc_1c_2 \times X \times \frac{M(M-1)(M-2)}{3!} - bc_1c_2 \times \sum_{k=0}^{M-1}\left(\sum_{j=0}^{k-1}\left(\sum_{i=0}^{j-1}(Y[i] \times Vref)\right)\right) \quad (1)$$

where b, c_1, c_2 are the modulator feedback coefficients that control the modulator loop stability and the converter resolution. Similarly to the former coefficients, and from Figure 3, a_1, a_2, a_3 are the feed-forward coefficients from the converter structure. The loop

coefficients are all equal to 0.34 and the FF coefficients equals 2, 1, and 0.5 for a_1, a_2, a_3, respectively. Further details about the converter operation, its coefficients can be traced in Freitas et al. [5] and in J. Markus et al. [18].

The ratio of the input voltage to the reference voltage is estimated as [18]:

$$\frac{Vin}{Vref} = \frac{3!}{M(M-1)(M-2)} \times \sum_{k=0}^{M-1} \left(\sum_{j=0}^{k-1} \left(\sum_{i=0}^{j-1} (Y[i]) \right) \right) \tag{2}$$

where $Vref$ is the absolute difference from the positive and the negative outer reference signals, centered and equally spaced from the virtual reference ground, and Vin is the time domain representation of the state input variable, X. If the output of the last integrator is supposed to be bounded to the "$PxVref$" product quantity, then the effective quantization step of the ADC can be expressed as follows

$$V_{LSB} = \frac{P}{bc_1c_2} \times \frac{3!}{M(M-1)(M-2)} \times Vref \tag{3}$$

Note that P is the factor that refers to how much of the signal at the last integrator output node, and it is allowed to drift and go beyond the $Vref$ reference level.

For this particular 3rd order system, the thermal noise power averaging effect is expressed by the following [18],

$$\sigma_{OUT}^2 \leq wf \times \frac{\sigma_{IN}^2}{M} \tag{4}$$

whose wf worsening factor equals 9/5 (when compared with the unity reference factor from the first order oversampling converters) and M is the number of clock cycles to run the system, also known as the over sampling ratio (OSR).

3. Problem Description

The excessive power dissipation does not end with the usage of ISD converters by themselves. The issue extends to the column signal drivers, which are responsible to drive the pixel signals and properly set the DC pixel signal levels to the input node of the column ADCs.

These intermediate active driver stages consume approximately the same, if not higher, current compared to the input stage of the ISD modulator. Although these driver stages are not part of the conversion system, which may allow amplification (namely the programmable gain amplifiers-PGAs), they are fundamental element stages to consider, given that they are necessary intermediate stages to make the column ADCs work properly, given the absolute level of the pixel signals.

Furthermore, ISD converter systems require three types of reference signals, which need to be driven by strong and usually on-chip buffers [3]. One reference is seen as the virtual ground for the ADCs, while the other two are the positive and negative outer references required for proper operation, as represented in Equations (1)–(3).

Moreover, the power required for all three reference generation and drivers is in the range of the column readout power dissipation [5], in this case, with 3rd order converter systems. In other words, for every micro-Ampere of current required for the column circuits (PGAs + ADCs), there will be a similar current consumption drained from the analog supply, required for the reference's generation and drivers.

From the reader's perspective, it then becomes clear that the requirements and the needs to address the low-noise feature, the high FR, and the high resolution specifications go in the opposite direction to the chip power dissipation.

Two additional key issues are worth raising now regarding the chip power dissipation and the device's temperature.

A. The first issue, which interferes with the sensor's overall noise performance, has to do with the pixels' dark current. The dark current amplitude is known to be temperature-dependent and increases exponentially with the temperature. Above 40–50 °C, the dark current becomes significant. It is, therefore, expectable that a significant power dissipation will lead to a performance degradation of the noise floor, due to the excessive collected dark exposure time applications, at the expected low-light conditions.
B. The second issue to be raised (prior to enumerating the low-power design options) is the effect of the die working temperature respective to the device's yield. The higher the device working temperature, the greater the chances of the device not complying with the expectations, in terms of functionality or performance playing a significant role in the device yield in the sensor's life expectance, from a commercial perspective.

Lastly, excessive power dissipation, which may be experienced by any device, brings complications to the packaging choice for the CMOS image sensors, making the system not only costly but also bulky, depending on the type of heat-sink or packaging used.

It is precisely to face all these problems that this research was proposed. Before going through the proposed solution, it is necessary to enumerate the typical choices that are used to mitigate the power issue on CIS devices employing ISD converters. The available choices are typically:

- The reduction of the analog voltage supply.
- The reduction of the digital voltage supply.
- A movement to a smaller process node.
- A change from differential output circuits to single-ended output amplifiers.
- The employment of hardware design recycling techniques.
- Off-chip ADCs references generation.

First of all, the choice of an analog voltage supply lower than 3.3 V becomes effective knowing that, for a high-order ADC modulator (for instance, for a 3rd order ISD converter), the current consumption portion of the modulator lies in the range of approximately 55% of the entire per-column readout circuit current consumption (including the digital filter current), yet excluding the partial amount for the references generation consumption.

Taking into account the input ADC driver stage, namely the PGA stage, this portion rises to 75%, reserving the remaining 25% for the per-column digital filtering circuit. Therefore, it becomes evident that, for instance, moving from a 3.3 V analog supply down to a 1.8 V supply, the expected per-column power dissipation reduction drops roughly 45%. The 45% power saving factor becomes global (and not only a per-column power reduction number), taking into consideration the fact that the on-chip ADC references and their strong drivers consume at least the same current as that required for the PGAs and ADC modulators, in this presented test chip development.

However, there is a disadvantage and a strong implication with this choice. It has to do with the expected pixel signal swing at the pixel column bus. Usually, it is expected to be in the order of 1 V, which is translated to 1.22 V at the input node of the ADC (namely the output of the PGA), accounting for the default PGA gain of 1.22, due to the usual signal drop from the pixel SF gain of 0.82. This is done to maintain a unitary system gain. Values above the 1 V signal range at the pixel floating diffusion (FD) node are relatively standard in modern imaging devices. The higher they are, the better. Lower than these values means that the sensor may lack a sensor dynamic range (DR).

Therefore, supplying column analog circuits (PGAs and the ADC modulators) at 1.8 V may create signal limitations on those stages, resulting in a reduction of the available signal room, hence limiting the sensor DR. Although it is challenging to reach a 1.22 V signal swing at a 1.8 V supply, due to the ever-present internal resistor drop (IR-Drop) effect across the columns, it is nevertheless feasible.

Secondly, and similarly to the reduction of the analog voltage supply method, the reduction of the digital supply is a valuable choice for a significant mitigation of the overall power dissipation and the rise of the sensor temperature. The remaining 25% of digital

power dissipation can be reduced to lower levels if the digital supply is also reduced. This option requires one to move to a smaller process node or requires sacrificing the noise margin of the logic gates operation if lowering the digital voltage supply, staying at the same process node design.

The third method that eases some of the design requirements due to circuits exhibiting less temporal noise in the dark is to make the CIS development in a smaller process node, as previously mentioned. This can be considered because transistors exhibit lower flicker (1/f) noise power at an equivalent bias and devices' size conditions than at a bigger process node. Since the overall noise contribution comes from both thermal and flicker noise sources, the chip power dissipation can then be decreased due to the relaxed constraints for the readout circuit's bandwidth, thus reducing the current consumption.

The fourth method available is obtained by reusing the hardware. With this approach there is no need to increase the overall current consumption to achieve a certain value of speed performance and/or functionality [5,14,15,17]. In addition to this, further power improvements can be reached by solely using inverted-based amplifiers, as used by P. Bisiaux et al. [13] or with the cascade common-source amplifier used by Y. Oike et al. [16], rather than using differential input amplifiers (with single-ended output or differential output), saving area and current consumption when compared with the single stage inverted-based amplifiers.

Lastly, a significant contributor choice for reducing the power dissipation of any image device, employing on-chip ISD converters, is to supply the ADCs reference signals from the outside world, namely with an off-chip. Either the on-chip or the off-chip generation are common solutions. On the one hand, the advantage of the on-chip references lies in the fact that these signals do not have to pass through the chip pads and go through their respective bond wire inductances. Additionally, this avoids suffering from possible disturbances from digital signals toggling in the chip IO ring. On the other hand, the advantage of generating the references off-chip lies in the PCB system that holds the chip. Not only does this originate smaller chip power dissipation but it also reduces chip complexity and moves some of the on-chip circuits' responsibility to the off-chip.

Apart from all the previously mentioned ways to reduce power consumption and to avoid excessive temperature rise, it appears that there is another way to further reduce the image sensor power dissipation, possibly improving the sensor noise floor and the dynamic-range, as well as the device yield, the current consumption, and consequently the battery life in the case of battery powered applications. The proposed means is described in Section 4.

4. Proposed Low-Power References Supply Cost-Effective Solution

The proposed low-power solution is described in this section and is depicted in Figures 4 and 5. The concept uses the fact that the references are "brought" from outside the silicon, similarly to the last power reduction option addressed earlier in Section 3. The difference is that there is no need for external regulators ICs for the proposed off-chip references generation option, except the regulator ICs for two power supply domains, namely the analog and the digital supplies.

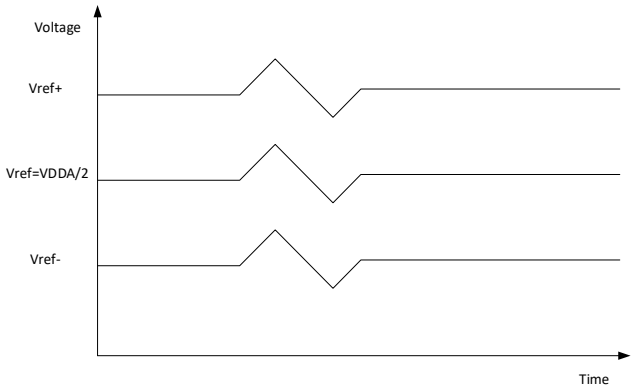

Figure 4. Expected behavior of the group of references with the proper capacitive decoupling effect.

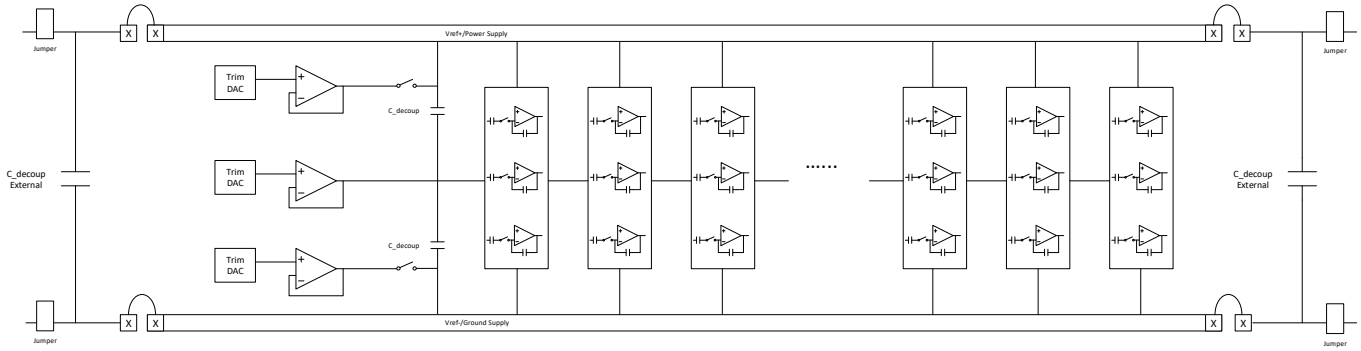

Figure 5. Proposed simplified low-power scheme, with low (Vref−) and high (Vref+) references wire connections.

Instead of simply moving their generation to the off-chip, through the usage of on-board DAC ICs or voltage regulators ICs (keeping the PCB system costly, crowded, and complex), two of the three references (namely the outer references) can be tied to the ground node and to the supply node of the board, respectively, leaving the "virtual ground" reference to be handled.

This strategy can be employed, given that from the highest outer reference, current is always supplied, while from the lowest outer reference, current is always sunk. This issue is precisely the feature of the power supply nodes, i.e., the power node supplies current and the ground node always sinks current. For this reason, both analog power rail nodes can be used for the ADC reference generation, as well as for a driving scheme.

The proposed reference generation and its supply scheme not only save on-board hardware but also save a considerable amount of chip power dissipation due to the absence (or turn-off) of the on-chip reference drivers. The power saving factor can become immense when combined with a lower power supply in a future test chip design phase.

Figure 4 shows the desired behavior of all three reference nodes when both high (Vref+) and low (Vref−) outer references nodes are supposed to be connected to the board power nodes, combined with both internal and external capacitive decoupling effects, this time taking advantage of the pad bond wires inductance. Any disturbance occurring in one of the references nodes should cause the effect to be propagated to the other reference nodes, given that the ISD ADCs are sensitive to the voltage difference between them, not only during the conversion operation but also as time passes.

Figure 5 depicts the proposed simplified low-power connection scheme and the internal organization of the ISD ADCs on the column-parallel readout structure test chip CIS. The core of the test chip is mainly the ADCs given their importance, current consumption, and design/layout constraints, among others. This is the reason why the converters modulators are the only hardware parts depicted in Figure 5.

The reader may note that although the default use case for this first test chip CIS development is to use the available internal driven references, a chance was provided to validate the new low-power concept through the supply of the reference signals from the off-chip through dedicated pads.

When in default use case mode, the on-chip references drivers and the on-chip DACs supply 1.15 V, 1.65 V, and 2.15 V for the lower (Vref−), the virtual ground (Vref), and the higher (Vref+) references, respectively, performing a 1V-ADC signal conversion system. When in use case of references equals 0.65 V, 1.65 V, and 2.65 V, respectively, the CIS behaves as a 2V-ADC light converter system, with a coarse quantization step twice compared with the 1V-ADC.

To increase the ADCs signal range, the outer references need to be increased to their maximum value up to the system voltage supply, namely tied to the analog 3.3 V/0 V board supply. This is only accomplished by the off-chip connection scheme, as briefly depicted in Figure 6, with the turn-off of the internal DACs and respective drivers. In this case, the option is to connect the low (Vref−) and the high (Vref+) outer references nodes to the ground and the power nodes, respectively, placing some jumpers on the board pin-header to perform the connections and to get the wider reference's effect. In addition to this, the reader may note that the driving method is performed on both sides of the test chip for a balance driving effect of the external references.

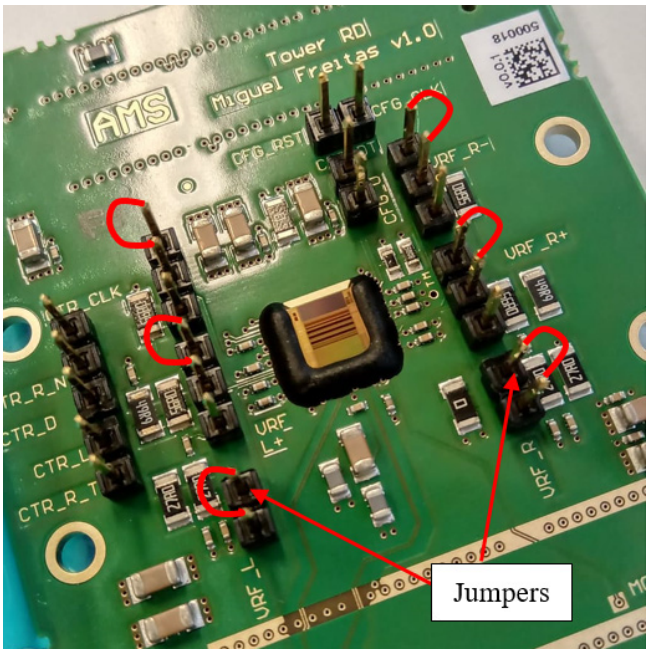

Figure 6. PCB board with pin-headers ready for external references generation and usage through the external connection with jumpers.

With regards to the virtual ground (middle) reference, Vref, it can be generated on-board through a simple resistor divider, providing sufficient driving strength. This option may be adopted given that the virtual ground signal will always be equal to half the analog supply (VDDA/2). With 1% error (precision) SMD resistors, the virtual ground generation effect can be properly created from the main board supply.

Moving towards the off-chip, the outer references generation (with the proposed connection scheme) with a simple virtual ground generation and originates further savings regarding the board space, routing complexity, and system cost, allowing one to obtain a much less bulky solution, and, simultaneously, reaching a working and practical system.

5. Proof-of-Concept and Silicon Proven Results

In this section, silicon proven results are presented, corroborating the proof-of-concept. It is worth reminding the reader that this test chip was mainly aimed to address a low-noise CIS with a fully functional column readout circuit based on high-order ISD 14-bit resolution converters and then to further optimize the sensor readout noise, speed, and power dissipation related issues during future development.

In this sense, the purpose of this part of the research work is to verify that the CIS functionality remains correct, namely a correct CIS response to light integration through an extended device integration time/exposure time (Tint/Texp) under the proposed low-power connection concept, and which actions should be taken to use it in the future.

The best way to check CIS functionality, working under the proposed low-power scheme (i.e., an off-chip 3.3 V supply outer references range), is to compare the outcomes of the short optical and electrical characterization for the off-chip reference generation, the 3V3-ADC, with the test chip CIS responses with on-chip references generation, namely the 1V and the 2V-ADCs.

Therefore, three characterization scans were performed with similar setting conditions except for the references values. Note that the characterization work was made with in-house automated tools compliant with the EMVA-1288 standard [19] using the photon-transfer method.

In the first scan, references were such that the systems worked as a 1V-ADC system (with 1.15 V–1.65 V–2.15 V), while in the second scan the references were increased to allow a 2V-ADC converter behavior (0.65 V–1.65 V–2.65 V), and finalized with the proposed reference's off-chip connection, resulting in a 3V3-ADC converter system (0 V–1.65 V–3.3 V). In all three cases, the virtual ground (i.e., the middle reference) was always equal to VDDA/2, in other words, equal to 1.65 V.

Figure 7 depicts the several ADC cases and combined photo response curve (PRC) results (characteristic from EMVA-1288 standard procedures) from the short characterization work done over the CIS device.

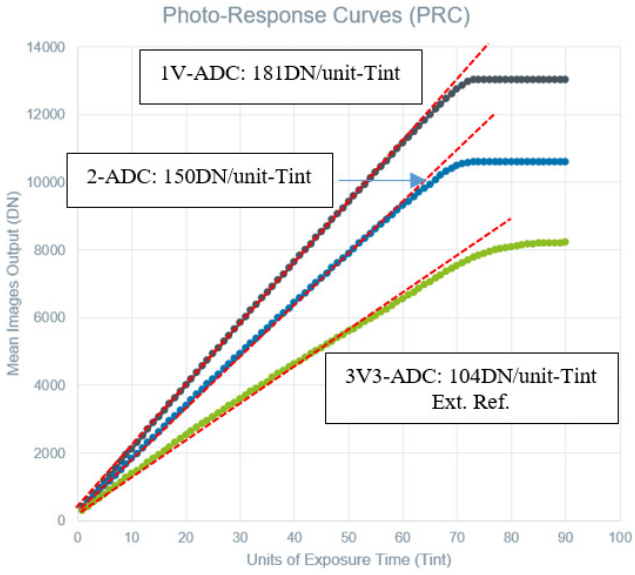

Figure 7. Combined photo response curve (PRC) data as a function of units of Tint (x19 us).

The reported PRC curves strongly indicate evidence that the whole imaging system is working correctly with the external supply of the converter references (the 3V3-ADC), given the resulting output linear response, when compared with the on-chip reference generation cases (the 1 V and the 2V-ADC).

The outcomes are linear among the three cases, until the CIS saturates, whose behavior is in accordance with the EMVA-1288 standard. In this sense, if the reader focuses on the fact

that the high/low outer references are being supplied through their external connections, namely, from the PCB board VDDA and GNDA nodes, then the corresponding PRC results (from the 3V3-ADC) are pre-ensuring that such a connection scheme is a viable option to avoid excessive device power dissipation, additionally allowing one to take all the corresponding benefits from it.

However, the PRC curves inspection is not the only indicator that the CIS device is working as expected in accordance with the standard [19]. To reinforce and confirm that the sensor is fully functional among the on-chip and the off-chip reference generation methods, each case associated photon transfer curves (PTC) is analyzed.

Figure 8 shows the relevant PTC curves, whose noise variance responses are important to check for the CIS, namely the noise curves regarding the three different reference generation cases, namely for the on-chip generation 1V-ADC, the 2V-ADC, and for the off-chip reference generation 3V3-ADC.

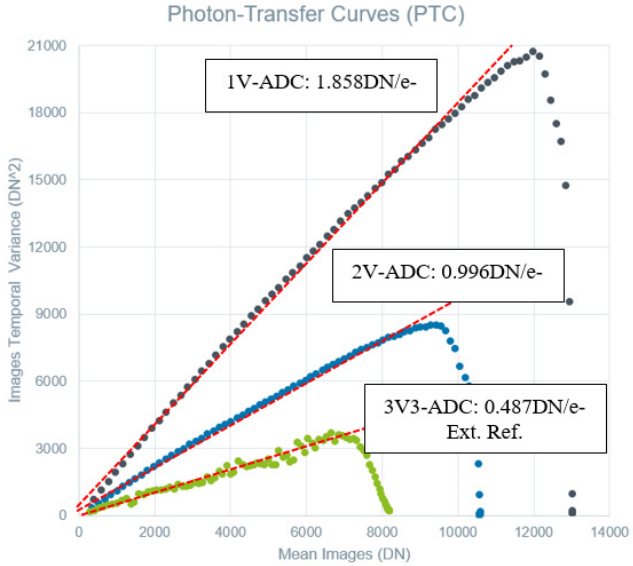

Figure 8. Combined photon transfer curve (PTC) data as a function of the image's mean values.

The correct noise variance response of an image sensor is linear with the average illumination power for a constant exposure time (or linear with the photon-generated charges, in which their counts are linear with the pixel integration time) until the sensor saturates, reaching the sensor full well (FW) capacity. Based on the above results from Figure 8 reported PTC responses, it can be inferred that the external references connection (producing the 3.3 VADC behavior) reacts linearly and similarly with the on-chip reference generation ADC cases (the 1 V and the 2 VADCs).

As a consequence of the reported Figure 7 PRC and Figure 8 PTC curves, it is possible to conclude that, fortunately, the proposed off-chip reference generation connection scheme is indeed a valid working principle. Furthermore, it is expected that, by providing an appropriate external filtering effect from the on-board power domain, the concept can be further explored and further utilized in real usage end scenarios, since the on-chip column converters are sensitive to the references, sensitive to how they are generated, and due to how clean these are.

To complement the several PRCs outcomes, Figure 9 depicts the extracted absolute system non-linearity over the several characterization pixel exposure time scans cases. From the collected data, it is demonstrated that the sensor response is fairly linear among the three test cases, as the whole system integral non-linearity (INL) remains close to 0.75% for the 1V-ADC, 1.25% for the 2V-ADC, and 1.75% for the 3V3-ADC.

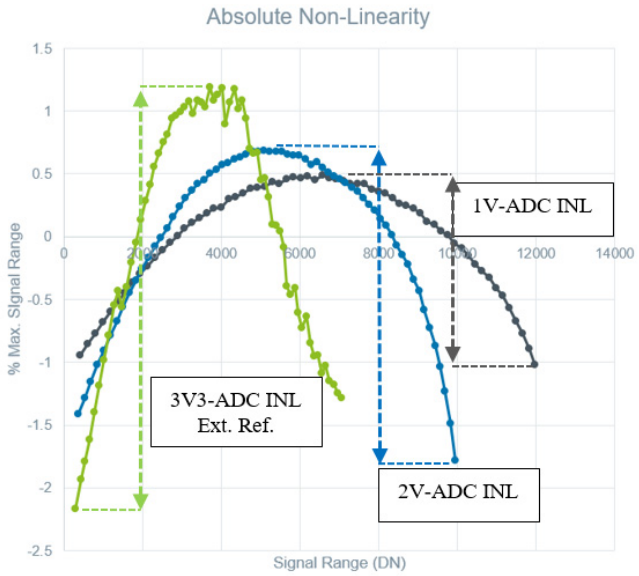

Figure 9. Absolute non-linearity curves.

The proposed low-power connection scheme exhibits slightly worse non-linearity compared to the default use case of internal references generation. Nevertheless, it is still small enough to be seen as a viable option for future consideration, simply requiring some optimization on the combined scheme and the entire converter system design to allow its full usage with acceptable non-linearity values below 1%, which is the typical system INL value for CIS devices in the market.

The observed higher non-linearity appeared only because the chip design was not optimized in first place to use this off-chip connection scheme as the default use case, given that the main focus was aimed mainly to verify the functionality of the complex on-chip high order column converters design [5]. However, a chance was given to the current test chip to try and verify the proposed off-chip references connection scheme for its future usage. Even knowing beforehand and from the characterization results, that it needs a bit more focus and careful design when taking such references connection scheme as the standard/default method for supplying and driving the references.

Next, a summary of the sensor features over the three scans is presented in Table 1.

Table 1 puts in evidence the analog power consumption and the chip total power consumption (which includes both portions of the analog and the digital power), revealing that the sensor can be operated adequately with external references, saving a lot of power, but most importantly, that it can be tied to the power rails, namely the high (Vref+) and low (Vref−) outer references. The combined Figures 7–9 graphical results and Table 1 allow one to formulate the following conclusion: The sensor performs correctly and is fully functional with the proposed external references connection scheme, behaving in accordance with the European Machine Vision Association (EMVA) standard [19].

Although the early CIS design did not have as its primary goal to operate under this proposed low-power scheme, by exhibiting a higher read noise in the dark and higher INL, among other factors, it was nevertheless aimed to perform this test as a means to confirm this low-power connection scheme as a viable and useful option for a possible future CIS to meet both low-noise and low-power features, with a simple and cost-effective reference generation scheme on the board power supply connection.

Table 1. Sensor key Specifications.

Scheme 13. × 13 um Pixel; 85% Fill Factor; 523 nm; QE > 60%	**1V-ADC Int. Ref. Range (1.15 V–1.65 V–2.15 V)**	**2V-ADC Int. Ref. Range (0.65 V–1.65 V–2.65 V)**	**3V3-ADC Ext. Ref. Range (0 V–1.65 V–3.3 V)**
Conv. Gain (CG)	1.858 DN/e^-	0.996 DN/e^-	0.487 DN/e^-
Responsivity	1.22 DN/photon 4610 DN/nJ/cm^2	0.661 DN/photon 2501 DN/nJ/cm^2	0.292 DN/photon 1104 DN/nJ/cm^2
System INL	~0.75%	~1.25%	~1.75%
Saturation Capacity	6400 e^-	9369 e^-	14083 e^-
Full Scale (at Sat. Capacity)	11,890 DN	9336 DN	6852 DN
Sensitivity Threshold	4.44 photons/pixel	4.3 photons/pixel	22.75 photons/pixel
Temporal Noise (in Dark)	5.41 DN 2.91 e^-	2.84 DN 2.85 e^-	6.64 DN 13.66 e^-
Dark Signal Non-Uniformity	2.59 DN 1.39 e^-	1.62 DN 1.63 e^-	2.35 DN 4.84 e^-
Photo Response Non-Uniformity	1.61%	1.36%	3.34%
Dynamic Range	66.84 dB	70.33 dB	60.27 dB
Signal-to-Noise Ratio	38.35 dB	40.11 dB	41.22 dB
ADC Clock Speed		20 MHz	
Single Conv. Time		*6 us*	
Digital CDS Conv.		*14 us (6 us + 2 us + 6 us)*	
Total References Power Consumption	~132 mW (*Int*) 0 W (*Ext*)	~132 mW (*Int*) 0 W (*Ext*)	0 W (*Int*) ~132 mW(*Ext*)
I. Analog Power (only the 3.3 V sup.)	264 mW	264 mW	~132 mW
II. Total Power Diss. (3.3 V & 1.8 V sup.)	310.8 mW	310.8 mW	~178.8 mW

The proposed low-power cost-effective solution was able to save 50% of the chip power consumption with regards to the chip analog power domain, knowing beforehand that the power reserved for the on-chip references generation and its drivers roughly equals to the power that is reserved for the remaining on-chip circuits supplied by the analog power.

Additionally, the proposed solution illustrates that if the scheme is combined with the future chip development analog voltage supply reduction (the latter is known to allow lower readout noise circuits through the usage of thin-oxide devices that exhibit considerably less 1/f noise power), the imaging device can not only reach future competitive levels of noise performance but can also reach competitive values of power dissipation, being able to save 45% power due to supply reduction, in addition to the 50% power already saved as mentioned above due to the off-chip references. In this specific future scenario, the references would be equal to 0 V–0.9 V–1.8 V, for the low (Vref−), the virtual ground (Vref) and the high (Vref+) outer reference, respectively.

Apart from this, the proposed solution not only ends with a much simpler and less bulky PCB system, but also ends with a cheaper overall imaging system, given that the off-chip references generation and driving method are facilitated with the proposed connection scheme, thus avoiding the need to have external and additional regulators ICs for those.

In summary, the critical issue that this research paper wishes to address is the effectiveness of the proposed low-power connection scheme and if it can originate a CIS device with

a correct behavior. This work revealed that the test CIS device is indeed fully functional with the proposed low-power connection scheme. The originality of the work falls into the proposition of an experimental external reference's supply connection scheme to generate and drive them to the on-chip ADCs, which is demonstrated by the outcomes that it works satisfactorily. The solution by itself already brings half the power to off-chip. With the particular scheme, it enables to maintain the sensor dynamic range if it is thought to be used in combination with a lower analog supply voltage (in a future CIS development), which by itself will further save considerable amount of power as well. Furthermore, it simplifies the surrounding electronics making the PCB less bulky, and it originates a more cost-effective solution, concerning external components.

To the extent of the author's knowledge, there is no such connection scheme being employed. Authors believe that this connection scheme, is a particular one from the authors since it connects the outer references (Vref+ and Vref−) directly to the power rails, except for the middle reference (the virtual ground reference), which still needs to be created in a classical form via an external DAC IC or from an on-board properly dimensioned resistor divider.

However, because this was a secondary goal of the research project, but worthy to be tested, the non-linearity and the noise increased. Therefore, further developments focused on this particular solution are necessary in order to fix the higher INL and higher noise floor, especially if such an option is foreseen to be used as the default ADCs operation mode. This needs putting emphasis and effort into the future design phase, dedicated to this issue, in order to make this low power option linear and less noisy.

6. Conclusions

A 256 × 92 pixels test CMOS image sensor, based on a 14–bit 3rd–order ISD column converter array, with a variant option of a low-power mode connection scheme is presented in this paper. The proposed solution uses the fact that the high/low outer references supply/sink current, respectively. Therefore, these references can be tied to the power rail nodes to perform their task.

The main part of this research work was dedicated to verifying that such a scheme would produce a correct and classical CIS response, resulting in appropriate PRC and PTC responses. In this sense, the research work outcomes allowed one to conclude that the low-power connection scheme does indeed work and can be beneficial when used, while also reaching a competitive imaging device with regards to the excessive power dissipation. Therefore, the proposed solution may be considered for usage in future CIS designs, as a standard option for a true low-power device based on high-order ISD column converter systems.

The choice of bringing the references outside the die allowed for a 50% power saving factor when compared with the chip power consumption, when the references are generated and driven on-chip. This option is already known in the literature, but when combined with the analog voltage supply reduction, for instance from 3.3 V to 1.8 V, the power saving factor can be incremented by 45% in addition to the already achieved 50%, reaching 22.5% of the current device power.

The default use case is such that the power consumption from the analog supply remains roughly around 1mW per readout column, accounting for 500 uW power (approx.) reserved for the entire analog column readout circuits (namely the PGAs + ADCs), and with another 500 uW power (approx.) for the reference drivers, all of these supplied at 3.3 V. By moving the references generation to an off-chip and using the chip low-power connection scheme, the power consumption per column reduced to 500 uW instead of 1 mW per column.

Finally, if the proposed chip low-power scheme is meant to be considered for usage on a future image sensor development, in conjunction with the analog power supply reduction option (for instance, the CIS supplied at 1.8 V with references at 0 V–0.9 V–1.8 V), then the columns will each consume 275 uW, accounting already for the required reference power.

This in turn facilitates the forecast and extrapolates the entire sensor power consumption, under the combined low-power scheme and the low voltage supply, when large sensors are about to be developed. For example, on a 1 K horizontal sensor resolution, the hypothetic sensor power consumption can be inferred to be 275 mW (excluding the digital power consumption portion).

Author Contributions: L.M.C.F.: writing—original draft preparation, writing—review and editing, term, conceptualization, validation, investigation, visualization. F.M.-D.: writing—original draft preparation, writing—review and editing. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: This research was supported by LARSyS (Projeto-UIDB/50009/2020) and MITIExcell, co-financed by Regional Development European Funds for the Operational Programme "Madeira 14-20"-EIXO PRIORITÁRIO 1, of Região Autónoma da Madeira, with no. M1420-01-0145-FEDER-000002. Furthermore, the authors would like to express their gratitude to Guy Meynants and Adi Xhakoni, for their support. Deepest thanks to Fabio Gaspar, Duarte Goncalves, Pascale Francis, Miguel Pestana, Joao Santos, Sergio Pestana, and Ricardo Sousa for all their help and support as well. This Research and Development (R&D) work was also supported and it was funded by AMS Sensors Portugal.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Cremers, B.; Innocent, M.; Luypaert, C.; Compiet, J.; Mudegowdar, I.C.; Esquenet, C.; Chapinal, G.; Vroom, W.; Blanchaert, T.; Cools, T.; et al. A 5 Megapixel, 1000fps CMOS Image Sensor with High Dynamic Range and 14-bit A/D Converters. In Proceedings of the 2013 International Image Sensor Workshop (IISW), Snowbird, UT, USA, 12–16 June 2013; pp. 213–215.
2. Yeknami, A.F. Low-Power Delta-Sigma Modulators for Medical Applications. Ph.D. Thesis, Linkopings University, Linköping, Sweden, 2013.
3. Freitas, L.M.C.; Morgado-Dias, F. A CMOS Slew-Rate Enhanced OTA for Imaging. *Microprocess. Microsy.* **2019**, *72*, 135–142. [CrossRef]
4. Freitas, L.M.C.; Morgado-Dias, F.; Meynants, G.; Xhakoni, A. Design and simulation of an incremental sigma-delta converter for improving the noise floor level of CMOS image sensors. In Proceedings of the International Conference in Engineering and Applications ICEA, Sao Miguel, Portugal, 8–11 July 2019.
5. Freitas, L.M.C.; Morgado-Dias, F. A CMOS image sensor with 14-bit column-parallel 3rd order incremental sigma-delta converters. *Sens. Actuator A Phys.* **2020**, *313*, 362–371. [CrossRef]
6. Freitas, L.M.C.; Morgado-Dias, F. Column Amplification Stages in CMOS Image Sensors based on Incremental Sigma-Delta ADCs. *Microelectron Eng.* **2020**, submitted.
7. Seitz, P.; Theuwissen, A.J.P. *Single-Photon Imaging*; Springer: Berlin, Heidelberg, 2011; Volume 160.
8. Suh, S.; Itoh, S.; Aoyama, S.; Kawahito, S. Column-parallel Correlated Multiple Sampling Circuits for CMOS Image Sensors and their Noise Reduction Effects. *Sensors* **2010**, *10*, 9139–9154. [CrossRef] [PubMed]
9. Chen, Y.; Xu, Y.; Mierop, A.J.; Theuwissen, A.J.P. Column-Parallel Digital Correlated Multiple Sampling for Low-Noise CMOS Image Sensors. *IEEE Sens. J.* **2012**, *12*, 316–324. [CrossRef]
10. Kawahito, S.; Suh, S.; Shirei, T.; Itoh, S.; Aoyama, S. Noise Reduction Effects of Column-Parallel Correlated Multiple Sampling and Source-Follower Driving Current Switching for CMOS Image Sensors. In Proceedings of the International Image Sensor Workshop, Bergen, Norway, 26–28 June 2009; pp. 320–323.
11. Chae, Y.; Cheon, J.; Lim, S.; Kwon, M.; Yoo, K.; Jung, W.; Lee, D.-H.; Ham, S.; Han, G. A 2.1M Pixels, 120 Frame/s CMOS Image Sensor with Column-Parallel Sigma-Delta ADC Architecture. *IEEE J. Solid-State Circuits* **2011**, *46*, 173–181. [CrossRef]
12. Xhakoni, A. High-Frame-Rate and High-Dynamic-Range Imager Readout Circuits for CIS and Stacked Technology. Ph.D. Thesis, Electrical Engineering, KU Leuven University, Leuven, Belgium, July 2015.
13. Bisiaux, P.; Lelandais-Perrault, C.; Kolar, A.; Santos, F.V.; Benabes, P. A 14-bit 250kS/s Two-step Inverter-based Incremental SigmaDelta ADC for CMOS Image Sensor. *Analog Integr. Circuits Signal Process.* **2019**, *97*, 427–435. [CrossRef]
14. Kim, W.-T.; Lee, B.-G. A Low-Power Extended-Counting Delta-Sigma ADC for CMOS Image Sensors. *J. Semicond. Technol. Sci.* **2019**, *19*, 594–599. [CrossRef]
15. Lee, I.; Kim, B.; Lee, B.-G. A Low-Power Incremental Sigma-Delta ADC for CMOS Image Sensors. *IEEE Trans. Circuits Syst. II Express Briefs.* **2016**, *63*, 362–369. [CrossRef]
16. Oike, Y.; Gamal, A.E. CMOS Image Sensor with Per-Column ΣΔ ADC and Programmable Compressed Sensing. *IEEE J. Solid-State Circuits* **2013**, *48*, 318–328. [CrossRef]

17. Xhakoni, A.; Gielen, G. Designing Incremental Sigma-Delta ADCs for Low Thermal Noise in Image Sensors. In Proceedings of the International Image Sensors Workshop, Snowbird, UT, USA, 12–16 June 2013; pp. 209–212.
18. Markus, J.; Silva, J.; Temes, G.C. Theory and Applications of Incremental Sigma-Delta Converters. *IEEE Trans Circuits Syst.* **2004**, *51*, 678–690. [CrossRef]
19. European Machine Vision Association. EMVA Standard 1288, Standard for Characterization of Image Sensors and Cameras. 2010. Available online: https://www.emva.org/standards-technology/emva-1288/ (accessed on 29 November 2010).