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Influence of Common Source and Word Line Electrodes on Program Operation in SuperFlash Memory

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Abstract: A theoretical study of the influence of word line and common source electrodes on the program operation in shrank SuperFlash memory is proposed. Numerical simulations demonstrate that the literature model defined for previous nodes is not always suitable, due to the continuous cell physical size reduction and to the consequent increment of capacitive coupling between the floating gate and adjacent electrodes. To get a deeper insight, an analytical model of the electric field in the region of source side injection is proposed. This model describes the impact of the cell physical and electrical parameters on the vertical and horizontal field components and highlights the strong dependence of the carrier injection on the technology node. Furthermore, the numerical and analytical models estimate the influence of the word line and common source electrodes on the time-to-program, the floating gate potential and the source side injection efficiency, taking into consideration, at the same time, their possible impact on the cell reliability.

Keywords: SuperFlash memory; program efficiency; word line and common source electrodes; cell physical parameters; TCAD simulations; source-side injection efficiency; time-to-program; floating gate potential

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1. Introduction

Electronic components are an important part of modern vehicles, and their role in the automotive industry is destined to grow with the gradual introduction of more and more sophisticated driver assistance systems (ADAS), setting the sight on full autonomous cars. For this reason, an increasing number of micro-controller units, together with embedded flash memory units (eFlash) are currently allocated in a vehicle [1]. In particular, eFlashes in automotive technology are usually employed for code storage and to collect the huge amount of data from the distributed on-board sensors. Due to their specific application, additional requirements are needed if compared with eFlashes in civil applications [2], i.e., high endurance, data retention and speed in program, erase and read operations [3]. Especially, fast programing is mandatory in order to face the continuous increment of memory density, thus the keeping rewriting cost as low as possible.

The embedded SuperFlash (ESF) memory was introduced in high-volume production in the 90s by SST® (ESF1) [4] as a stored charge-based memory technology alternative to the conventional floating gate (FG) one. ESF technology exhibits high injection efficiency, fast operations, over-erase immunity and improved reliability [5–7]. To achieve both short time-to-program (T2P) and high injection efficiency (η), ESF cells programing is based on the source side injection (SSI) mechanism [8–10].

According to the necessity of the progressive dimension and voltage down-scaling, in the subsequent generations of ESF memory (i.e., ESF2 and ESF3), the number of electrodes adjacent to the FG was increased in order to have a high capacitive coupling and a high FG potential (V_{FG}). Hence, in ESF2 one additional electrode (source line) and in ESF3 two more electrodes (coupling gate and erase gate) were implemented [11]. ESF3 appeared with the 110 nm technology node and it is still the leading ESF technology family with the latest

produced 28 nm node now on the market [4]. In ESF3, as in ESF1 and ESF2, the channel is shared between two electrodes, i.e., word line (WL) and FG, so that the SuperFlash cell structure can be approximated with the series of two transistors: FG-MOS and WL-MOS. The ESF3 cell is depicted in Figure 1a,b, where the erase gate and coupling gate electrodes are omitted for a clearer explanation of the cell working principle. The two transistors are in a source follower configuration and they are biased in saturation mode. In particular, V_{FG} is much higher than the FG-MOS threshold voltage, whereas V_{WL} is slightly above the WL-MOS threshold voltage. Hence, the channel portion of FG-MOS is in strong inversion (outlined in Figure 1a with the shadowed area beneath the FG), whereas the WL-MOS one is in weak inversion. The FG-MOS channel portion can be considered as a drain extension or a virtual drain [12,13]. Indeed, the WL-MOS load is represented by the series of FG channel resistance and FG drain resistance and, as they are both negligible, WL-MOS drain voltage can be considered equal to FG-MOS drain voltage (Figure 1c).

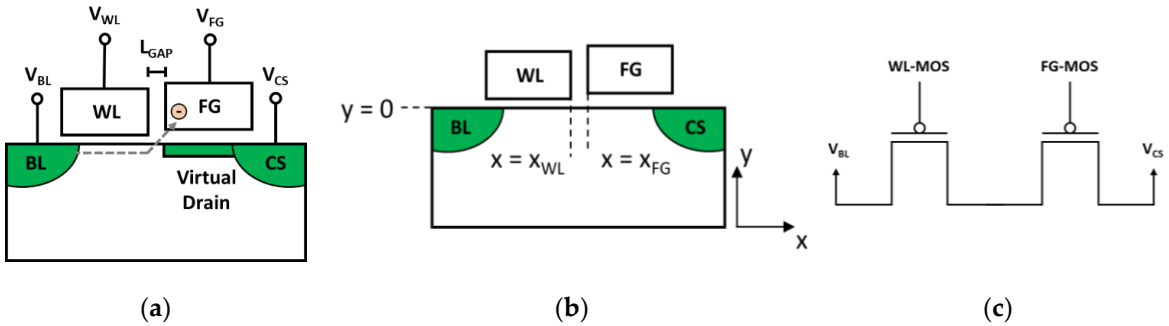


Figure 1. (**a**) The SuperFlash cell structure, with the source side injection (SSI) mechanism sketched; (**b**) adopted frame of reference definition; (**c**) approximation with the series of two transistors: WL-MOS and FG-MOS.

The SSI mechanism is sketched in Figure 1a with the dashed arrow and takes place approximately in the region between X_{WL} and X_{FG}. Electrons are injected from the substrate to the closest FG corner, involving both the horizontal and the vertical components of the electric field [14–16]. The vertical component is fixed by V_{FG} and is further enhanced thanks to the tip geometry of the FG; the horizontal component depends on the channel state, which in turn is influenced by the bias conditions applied on all the electrodes which overlook the channel, i.e., WL, bit line (BL), common source (CS) and FG itself. A way to quantify the SSI is by defining its efficiency (η) as the fraction of the channel current which ends up in the FG. It depends on the voltage waveform applied to the various electrodes and varies with the cell geometry. Being a main parameter in the program efficiency, η has been systematically and extensively studied in past ESF nodes [13,17,18].

In addition to η, also T2P and V_{FG} are key parameters in the program efficiency, concurring to define the optimum program strategy. From a practical point of view, T2P defines the program speed and V_{FG} the program window, while η is related to the power consumption, in the sense that a more efficient injection requires a lower channel current. Generally speaking, it is not possible to define a single ruling parameter in the program efficiency, as the relative importance of those three parameters should rather be referred to the specific application. For all these reasons, in this work, a theoretical study of the influence of WL and CS electrodes on η, T2P and V_{FG} is proposed, focusing specifically on the ESF3 current node now on the market [4]. Indeed, because of technology scaling, the bias conditions of the electrodes adjacent to the FG have a greater influence on both channel formation and V_{FG} than in past nodes. Therefore, the different role of electrodes as CS and WL in SSI should be discussed in order to gain a complete overview of the cell physics in the current node.

2. Methods

The SSI mechanism is investigated systematically by means of Synopsys Sentaurus technology computer-aided design (TCAD) simulations, varying the program conditions. All the numerical simulations have been performed fixing the values of the coupling gate voltage (V_{CG}), bit line voltage (V_{BL}) and erase gate voltage (V_{EG}) reported in literature [19–23] for the latest technology node, listed in Table 1 and shown in Figure 2. In particular, the bias conditions are: V_{CG} = HV (>10 V) [19–22]; word line and commons source voltages (V_{WL} and V_{CS}, respectively) have been varied, respectively, in the range 0.7–1.1 V and 4–4.6 V [20,21,23]; $V_{EG} = V_{CS}$ in order to avoid charge migration between the two electrodes [23]; I_{BL} is fixed at ~1 µA [20,24]. In all the simulations, a single 1 s-long pulse is applied on all the electrodes.

Table 1. Bias conditions in ESF3 program operation [19–23].

Electrode	Program
V_{CG}	HV
V_{CS}	4 ÷ 4.6 V
V_{EG}	4 ÷ 4.6 V
I_{BL}	1 µA
V_{WL}	0.7 ÷ 1.1 V

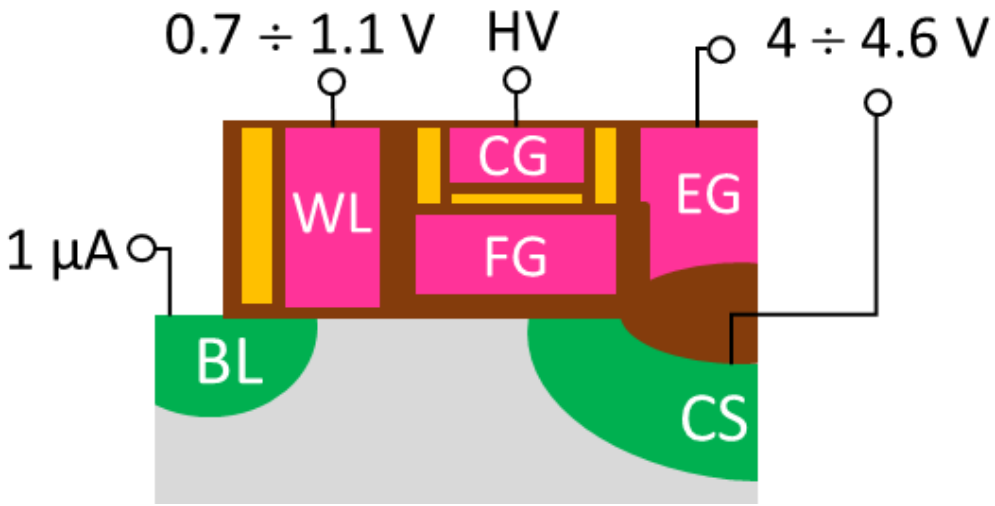


Figure 2. ESF3 cell representation with operating electrical conditions.

In the SSI mechanism both the horizontal (E_H) and vertical (E_V) electric field components are involved. In previous technology nodes, E_H and E_V during program operation were described, respectively, as [25]:

$$E_H = \frac{V_{CS} - (V_{WL} - V_{th,WL})}{L_{gap}} \quad (1a)$$

$$E_V = \frac{V_{OV,FG}}{t_{ox,FG}} \quad (1b)$$

where $V_{th,WL}$ is the threshold voltage of the WL transistor, L_{gap} is the distance between FG and WL (Figure 1a), $t_{ox,FG}$ is the FG oxide thickness and $V_{OV,FG}$ is the overdrive voltage ($V_{OV,FG} = V_{FG} - V_{th,FG}$) associated to FG-MOS. Nevertheless, the geometric features' scaling brings about additional effects, regarded as negligible in the past. For instance, as the electrodes spacing decreases the impact of WL and CS on FG increases, thus causing

different electric field behavior compared to past nodes. Furthermore, progressive distances shrinking can also affect the electrostatic cell conditions as well as E_H and E_V. Consequently, systematically investigation of CS and WL influence on program operation will be carried out in the following section. In particular, in order to isolate CS (and WL) contribution, standard biasing conditions (Table 1) will be applied, with V_{CS} and V_{WL} fixed at their mid-ranges (4.3 V and 0.9 V, respectively) when not under direct examination.

3. Results

3.1. Role of the Common Source Electrode

Impact on the Electric Field: CS electrode exerts a significant influence on the electric field components involved in SSI mechanism, especially on E_H. From Equation (1a), a linear E_H dependency on V_{CS} can indeed be observed. This holds in the current node as well, as demonstrated in Figure 3a where the simulated E_H curve is drawn as a function of the coordinate x, in the portion delimited by WL and FG edges. As concerns E_V, in past nodes it was successfully described by Equation (1b) and remained almost constant, being $V_{OV,FG}$ mainly determined by V_{CG} and influenced only partially by the other adjacent electrodes. Nevertheless, in the current node, CS contribution in V_{FG} cannot be neglected anymore, as verified in the simulated E_V curve drawn in Figure 3b. Here, E_V is depicted against the y-coordinate in x = X_{FG}, from the Si/SiO_2 interface toward the FG. By increasing V_{CS}, a horizontal translation of the E_V curve toward higher absolute values is found. This dependence is contained inside V_{FG} as it holds:

$$V_{FG}(V_{CS}) = \alpha_{CS-FG} \cdot (V_{CS_0} + \Delta V_{CS}) = \alpha_{CS-FG} \cdot V_{CS_0} + \alpha_{CS-FG} \cdot \Delta V_{CS} \quad (2)$$

where V_{CS_0} is the minimum value of V_{CS} (i.e., 4 V) and ΔV_{CS} is the variation of V_{CS} from this value. Because the product $\alpha_{CS-FG} \cdot V_{CS_0}$ is constant, a variation of V_{CS} causes a linear increase of V_{FG} and a parallel translation of the E_V curve with the same sign.

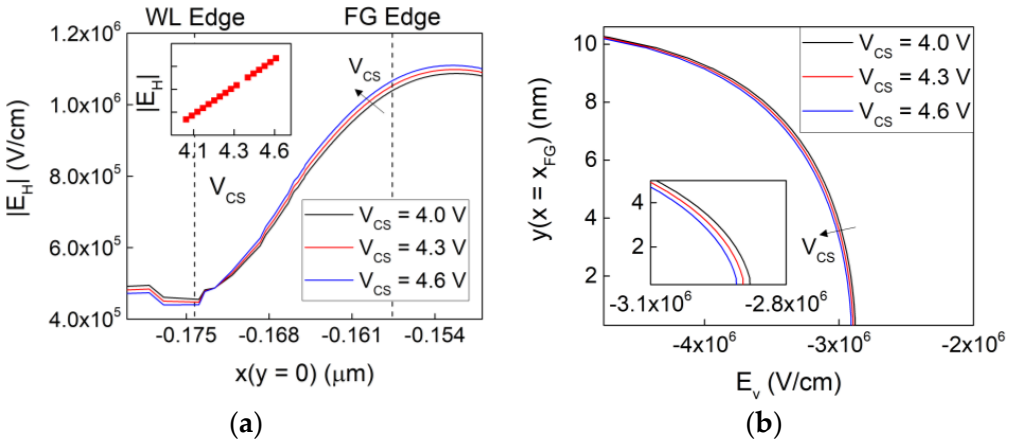


Figure 3. Technology computer-aided design (TCAD) simulations of the electric field with the common source (CS) voltage as a parameter. (**a**) The horizontal component is drawn against the x coordinate in y = 0, between the WL and the floating gate (FG) edges, the linearity being outlined in the inset. (**b**) The vertical component is drawn against the y coordinate in x = X_{FG}, between the SiO_2 interface and the FG edge, the dependence on V_{CS} being zoomed in the inset.

In conclusion, as the V_{FG} described by Equation (2) is proportional to the numerator of E_V (Equation (1b)), it can be finally stated that the total electric field $\left(\sqrt{E_V^2 + E_H^2}\right)$ increases linearly with V_{CS}.

Impact on the Floating Gate: The influence of V_{CS} on the floating gate is studied calculating V_{FG}, the FG current (I_{FG}) and the FG stored charge (Q_{FG}) during a 1 s-long program pulse (applied on V_{CS}, V_{WL}, V_{CG}, V_{EG} and V_{BL}) starting at t = 1 ns, with V_{WL} pulse am-

plitude at its mid-range and V_{CG} and V_{BL} pulse amplitude at the nominal conditions mentioned in Table 1. Results are reported in Figure 4.

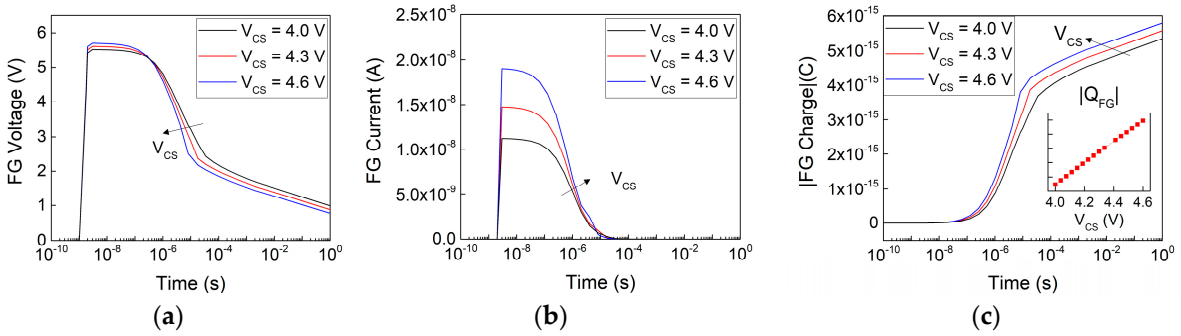


Figure 4. TCAD simulations of the (**a**) FG potential, (**b**) FG current, (**c**) charge injected in the FG, as function of time during a 1 s long program pulse with the V_{CS} pulse amplitude as a parameter. The linearity of the FG charge with V_{CS} is highlighted in the inset of (**c**).

At the very beginning of the program pulse, V_{FG} increases (Figure 4a). This is due to the capacitive coupling between FG and CS which, in turn, leads to an E_V increment, as discussed previously. I_{FG} behavior is displayed in Figure 4b. As the V_{CS} increment induces an enlargement of E_V and E_H, the hot-electron-injected current increases as well. As expected, with the gradual addition of electrons into the FG, both I_{FG} and V_{FG} start to decrease. A change of the slope takes place when the charge accumulated in the FG limits further injection (in this case, around 10^{-5} s), as can also be seen in Figure 4c. The cell is programed more rapidly at higher V_{CS}: indeed, I_{FG} is higher, so that the required time for reaching the target Q_{FG} is shorter. The linear dependency of Q_{FG} at the end of the program pulse on V_{CS} is depicted in the inset of Figure 4c. A similar result was obtained in [14], where the increment of V_{FG} with V_{CS} was experimentally measured in the 40 nm node.

3.2. Role of the Word Line Electrode

Impact on the Electric Field: As previously disclosed in the introduction, WL biasing has a great influence on the channel formation in both WL-MOS and FG-MOS portions. In particular, WL biasing controls the shrinkage of the channel in the L_{gap} area and, as the FG-MOS channel portion can be considered as a drain extension, drives the horizontal extension of the depletion region between FG-MOS and WL-MOS. From Equation (1a), the influence of WL on E_H can be quantified. As in a standard MOS, the horizontal component of the electric field depends on the difference between V_{CS} and V_{BL} and from the overdrive voltage in the WL-MOS. TCAD simulations show that E_H decreases with V_{WL} as demonstrated in Figure 5, where the absolute value of E_H is drawn by varying V_{WL}.

The vertical component E_V, instead, depends on FG-MOS overdrive voltage, thus from V_{FG}. This, in turn, can be influenced by V_{WL} due to the capacitive coupling factor between WL and FG, growing with the scaling. Hence, V_{WL} influences the numerators of both Equations (1a) and (1b). As a consequence, an increment of V_{FG} with V_{WL} is expected:

$$V_{FG}(V_{WL}) = \alpha_{WL-FG} \cdot (V_{WL_0} + \Delta V_{WL}) = \alpha_{WL-FG} \cdot V_{WL_0} + \alpha_{WL-FG} \cdot \Delta V_{WL} \quad (3)$$

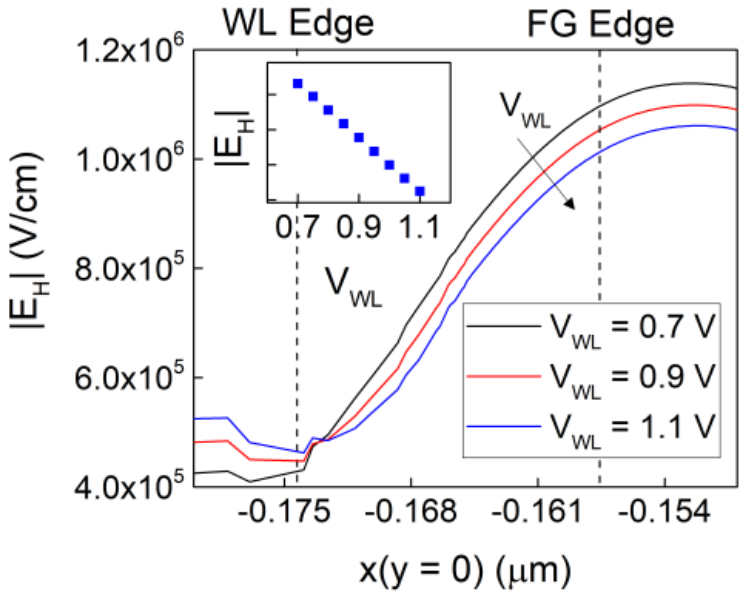
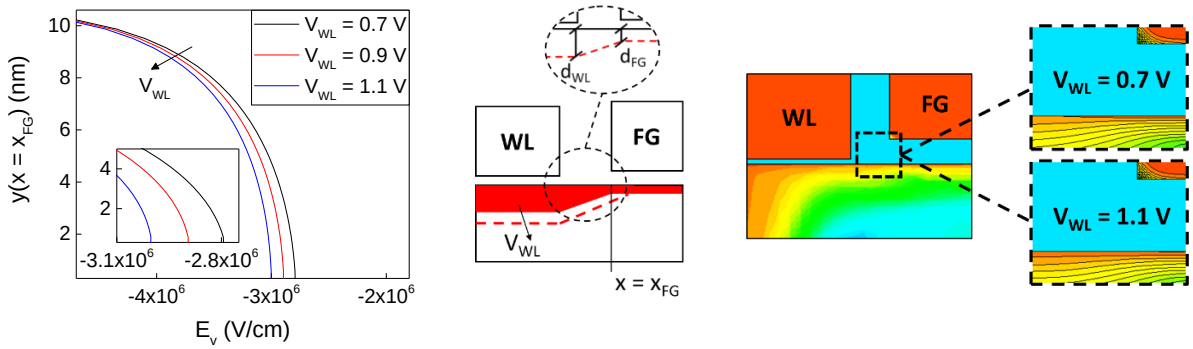


Figure 5. TCAD simulations of the horizontal component of the electric field plotted against the x coordinate in y = 0, between the WL and the FG edges, with the WL voltage as a parameter.

Equation (3) suggests that the FG potential dependency from V_{WL} is linear and, as a consequence of the direct proportionality between E_V and V_{FG} (Equation (1b)), E_V is expected to vary linearly with V_{WL} as well. On the contrary, simulations show that Equation (3) E_V does not follow the aforementioned dependency in the current node. In Figure 6a, the calculated curves of E_V are plotted as a function of the coordinate y at x = X_{FG}, with V_{WL} as a parameter. As one can see, by increasing V_{WL}, the E_V curves do not shift in a parallel way, as in the case of V_{CS}, and exhibits a spread at the Si/SiO_2 interface. To explain intuitively this behavior, in Figure 6b the shape of the channel is depicted with colored area (it has been emphasized for the sake of clarity). A lateral overlap between WL-MOS and FG-MOS channels is present, so that increasing V_{WL} the channel invades the area beneath the FG (dashed line in Figure 6b) and the amount of channel charge at x = X_{FG} increases. To get deeper insight into the E_V behavior in shrank nodes, an analytical model is proposed, which outlines the role of the cell electrical and physical parameters. To this aim, the following assumptions are made: (1) the channel depth from WL edge to the pinch-off point is linearly decreasing; (2) given a certain V_{WL}, the vertical distribution of electrons in the channel depth g(y) decreases exponentially from the Si/SiO_2 interface where it is g(0) = n_s (being n_s the electron density at the Si/SiO_2 interface) to the channel depth (d) where g(d) = N_A (being N_A the substrate doping concentration); (3) V_{FG} dependency on V_{WL} is negligible due to the low capacitive coupling between WL and FG; (4) the influence of E_H on the channel charge is negligible in X_{FG}.



(**a**) (**b**) (**c**)

Figure 6. (**a**) TCAD simulation of the electric field vertical component drawn against the y coordinate in x = X_{FG}, between the SiO_2 interface and the FG edge, with the WL voltage as a parameter. (**b**) The shape of the channel is depicted with colored area, while the dashed contour highlights that increasing V_{WL} the channel invades the area beneath the FG. (**c**) TCAD simulation of the channel electron density in x = X_{FG} represented by colors from blue to red, for two values of V_{WL}.

Based on the mentioned assumptions, it holds:

$$g(y) = n_s e^{-\frac{y}{d_{ref}}} \tag{4}$$

where d_{ref} is a fixed reference depth, not dependent on V_{WL} $\left(d_{ref} > d_{FG}\right)$. It should be noted that n_s increases with V_{WL}. This is shown in Figure 6c where a zoom of the structure is sketched and the increasing electron density is represented with colors from blue to red. The overall effect is an increment of the absolute value of the charge present in x = X_{FG}, which in turn enhances E_V. The direct extraction of carrier concentration values from TCAD simulation allows quantifying both n_s and d_{FG} dependencies on V_{WL}. Particularly, n_s is attained by probing the electron concentration at Si/SiO_2 interface in x = X_{FG} and multiplying the result to the channel width. Instead, d_{FG} is obtained by examining carrier concentration behavior as a function of y. Consequently, as shown in Figure 7a, it can be demonstrated that n_s increases linearly with V_{WL}, whereas d_{FG} varies as the square root of V_{WL}. Hence, by curve fitting the outcomes of TCAD simulations, it can be inferred that:

$$n_s(V_{WL}) = k_1 + \alpha\, V_{WL} \tag{5a}$$

$$d_{FG}(V_{WL}) \approx \sqrt{k_2 + \beta\, V_{WL}} \tag{5b}$$

where α, β, k_1 and k_2 are constants and are quantitatively derived from best fits of n_s and d_{FG} as functions of V_{WL}.

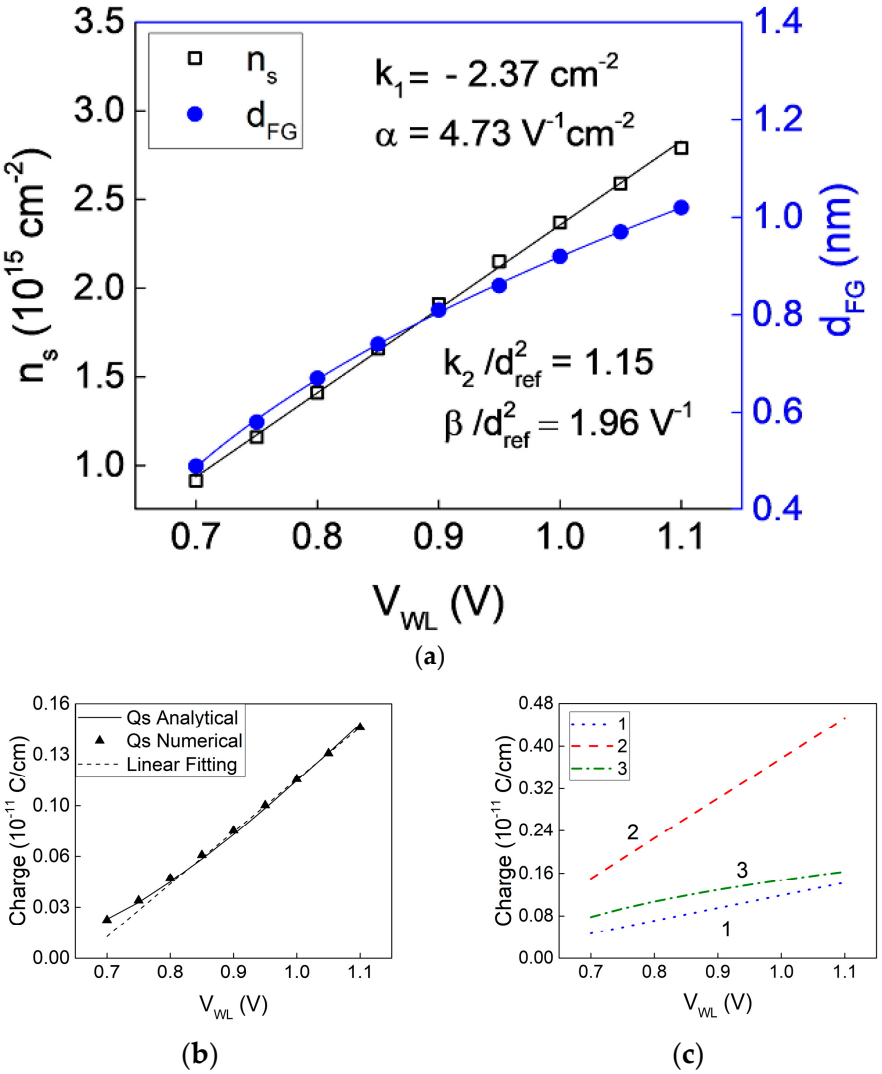


Figure 7. Results from the analytical modeling as function of V_{WL}: (**a**) surface electron density and channel depth in x = X_{FG} with linear and square root best fits (R^2 = 0.9987 and R^2 = 0.9996, respectively); (**b**) channel charge per unit width in x = X_{FG}; (**c**) weight of the three contributions of the total charge (Equation (6)).

Since the electric field is inversely proportional to the square of the distance between charges in the FG and the ones in the channel, only a small interval around x = X_{FG} is taken into consideration when calculating E_V. To obtain the amount of channel charge in x = X_{FG} (Q_C), one has to integrate g(y) along y and the normalized electron concentration (C_n). The integration limits are, respectively, d_{FG} (i.e., the channel depth at x = X_{FG}) and the Si/SiO_2 interface (y = 0) along y, and 1 (maximum concentration) and $-\ln(N_A/n_s)$ along C_n. The calculated integral is multiplied by the electron charge and the width of the structure (W), to give Q_C (expressed in C/cm). Therefore, as Q_C depends on n_s and d_{FG}, in turn it depends also on V_{WL}. Relying on assumption (4) it holds:

$$E_V(V_{WL}) = \frac{Q_C(V_{WL})}{\varepsilon_0 \varepsilon_{SiO2}} = \frac{1}{\varepsilon_0 \varepsilon_{SiO2}} \int_0^{d_{FG}} \int_{-ln\left(\frac{N_A}{n_s}\right)}^{1} qWn_s e^{-\frac{y}{d_{ref}}} dC_n\, dy = \frac{1}{\varepsilon_0 \varepsilon_{SiO2}} \int_0^{d_{FG}} qW\left(n_s e^{-\frac{y}{d_{ref}}} - N_A\right) dy = = \frac{1}{\varepsilon_0 \varepsilon_{SiO2}} \left[qW\left(-n_s e^{-\frac{d_{FG}}{d_{ref}}} + n_s - d_{FG}\, N_A\right)\right] \quad (6)$$

The total charge Q_C coming from the analytical model is displayed in Figure 7b (continuous line) together with the numerical values extracted from charge mapping in TCAD simulations (symbols). It can be seen that the agreement between numerical and analytical modeling is excellent (R^2 = 0.99887) and that the total charge variation is linear

with V_{WL}, apart from at low V_{WL} values (as demonstrated by the linear fitting displayed in Figure 7b with a dashed line).

In Figure 7c the three charge terms in the square brackets of Equation (6) are compared. Term 1 ($n_s e^{-\frac{d_{FG}}{d_{ref}}}$) refers to the surface charge density and the channel depth at X_{FG}, term 2 (n_s) refers only to the surface electron density, term 3 ($d_{FG}\ N_A$) refers to the channel depth and the substrate doping. This figure allows to understand the role of the cell physical and electrical parameters in determining E_V, thus highlighting its strong dependence on the specific technology node.

In conclusion, as the SSI mechanism depends on both E_V and E_H, their numerical values extracted from simulations are reported in Table 2 in the studied V_{WL} range. As can be noticed, the absolute value of E_V is always greater than E_H. Thus, although E_H decreases while E_V increases with V_{WL}, it can be inferred that the injected charge Q_{FG} would be more influenced by E_V. This will be verified below.

Table 2. TCAD simulated E_H and E_V absolute values calculated in x = X_{FG} and y = 0 as functions of V_{WL}.

V_{WL} [V]	$\lvert E_H \rvert$ [MV/cm]	$\lvert E_V \rvert$ [MV/cm]
0.7	1.09	2.79
0.9	1.05	2.89
1.1	1.01	3.00

Impact on the Floating Gate. The influence of V_{WL} on the floating gate is studied calculating V_{FG}, I_{FG} and Q_{FG} during a 1 s-long program pulse (applied on V_{CS}, V_{WL}, V_{CG}, V_{EG}, V_{BL}) starting at t = 1 ns, with V_{CS} = V_{EG} pulse amplitude at their mid-range and V_{CG} and V_{BL} pulse amplitude at nominal conditions. As the capacitive coupling factor between FG and WL is smaller than the one between FG and CS, the starting vertical offset of the V_{FG} is less evident than the one in the V_{CS} case. This reduced offset should result in a smaller E_v shift. In fact, as commented in the previous section, V_{WL} variation affects not only V_{FG} but also the channel state, which leads to an augmented injection current. Actually, other authors measured experimentally an opposite evolution in time of V_{FG} with V_{WL} in the 55 nm technology node [17]. Indeed, in that paper, V_{FG} at the end of the pulse reduced for values of V_{WL} over the threshold ($V_{th,WL}$). In that node, as the SSI mechanism is influenced by the technology node, and being the distance between WL and FG (relatively) long, an increment of V_{WL} led to a reduced E_H component, while E_V remained basically constant. On the contrary, in latest technology nodes, due to the shorter distance between WL and FG, the channel below WL can extend to x = X_{FG}, again reducing E_H, but increasing largely E_V, as previously shown in Table 2. Looking at Figure 8, it can be noticed that with the gradual addition of electrons into the FG, both I_{FG} and V_{FG} start to decrease, changing slope around 10^{-5} s when the stored charge Q_{FG} limits further injection.

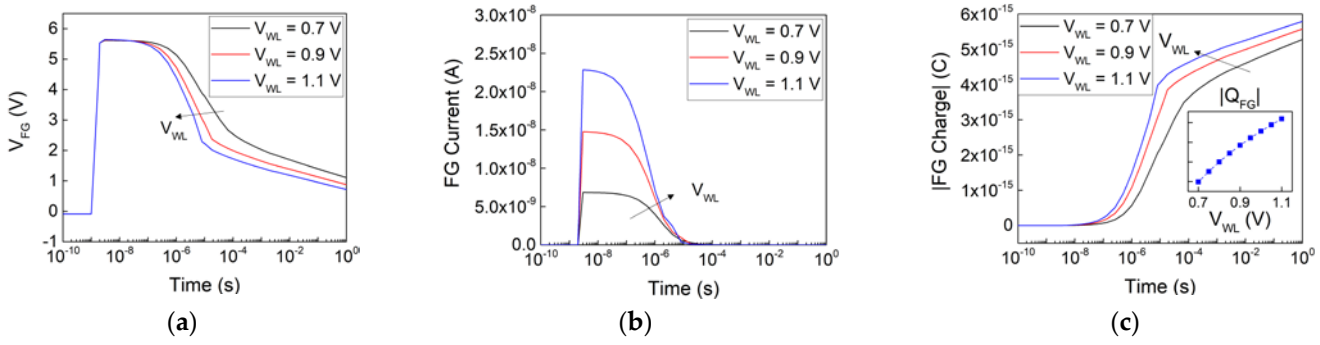


Figure 8. TCAD simulations of the (**a**) FG potential, (**b**) FG current, (**c**) charge injected in the FG, as function of time during a 1 s long program pulse with the pulse amplitude as a parameter. The sub-linearity of the FG charge with V_{WL} is highlighted in the inset of (**c**).

The cell is programed more rapidly at higher V_{WL}: indeed, I_{FG} is higher (Figure 8b), so that the required time for reaching the target Q_{FG} is shorter (Figure 8c). A sub-linear dependency of Q_{FG} at the end of the program pulse on V_{WL} is depicted in the inset of Figure 8c.

4. Discussion

In the previous sections, the impact of V_{CS} and V_{WL} on physical details underlying the SSI mechanism was studied. Hereafter, their macroscopic effects on the program operation will be analyzed, in terms of injection efficiency, FG potential and time-to-program.

The source side injection efficiency (η) is defined as the ratio between I_{FG} and the current which flows in the channel (I_{BL}): $\eta = I_{FG}/I_{BL}$. In Figure 9a, η is plotted as a function of both V_{CS} and V_{WL}. As one can see, η (slightly) decreases with V_{WL} and consistently increases with V_{CS}. The two opposite trends can be understood by studying separately I_{FG} and I_{BL}. Figure 9b,c shows that an increment of both V_{WL} and V_{CS} implies an increment of both I_{BL} and I_{FG}. However, in the V_{WL} case, the rate of variation of I_{BL} is faster than that of I_{FG} (Figure 9b), so that by increasing V_{WL} in its range, η degrades of about 10% (Figure 9a). On the contrary, in the V_{CS} case, I_{BL} and I_{FG} increase with quite different rates with V_{CS} (Figure 9c), so that, by increasing V_{CS} in its range, η improves of about 50% (Figure 9a). In conclusion, it can be affirmed that, as η (slightly) degrades with V_{WL}, it could be convenient to rather increase V_{CS}, keeping V_{WL} as low as possible.

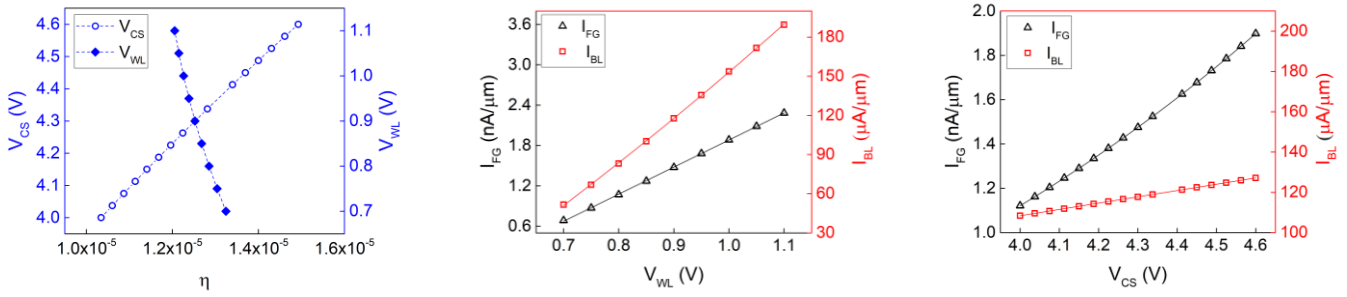


Figure 9. TCAD simulations of the overall impact of V_{CS} and V_{WL} on the main factors determining the injection efficiency: (**a**) η is drawn as a function of V_{CS} (open symbols) and V_{WL} (full symbols); (**b**) I_{FG} (open triangles) and I_{BL} (open squares) increase with V_{WL}; (**c**) I_{FG} and I_{BL} increase with V_{CS}.

As already verified in the previous sections, the potential that the FG reaches after a given program time, depends on V_{WL} and V_{CS}. In Figure 10a the absolute value of V_{FG} after a 1 s program pulse is depicted as a function of V_{WL}. As expected, V_{FG} presents a sub-linear behavior with V_{WL}, due to the sub-linear Q_{FG} dependency on V_{WL} (inset of Figure 8c). On the other hand, in Figure 10b, a linear dependence of V_{FG} on V_{CS} can be verified. The different trends of V_{FG} with V_{WL} and V_{CS} can be physically explained by considering that different portions of the ESF3 cell are influenced by V_{WL} and V_{CS}. Indeed, V_{WL} affects the channel features (depth and charge), but not the FG potential due to a negligible capacitive coupling. On the contrary, as the CS electrode is strongly coupled with the FG, a linear influence on the channel current I_{BL} is obtained (see Figure 9c). In conclusion, it can be stated that the FG potential at the end of the program pulse increases with both V_{WL} and V_{CS}, albeit with different trends.

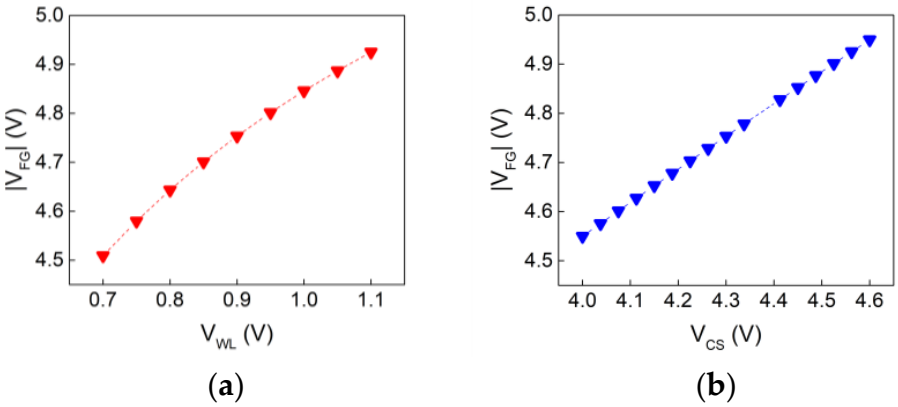


Figure 10. TCAD simulations of the FG potential absolute value increases: (**a**) sub-linearly with V_{WL} and (**b**) linearly with V_{CS}.

Finally, the time to program (T2P) is defined as the time needed to reduce the read current down to the 10% with respect to the read current associated to the erased cell. This quantity is determined by the charge injection dynamics into the FG and it is strongly not linear. It was already verified that the final charge transferred to the FG depends linearly on V_{CS} (Figure 4c), but it represented the state of the cell at the end of the program operation, not during the injection dynamics. The charge transfer occurs at a much higher rate in the very first instants so that, typically after a few microseconds, the 90% of the target charge is transferred [18]. In Figure 11, T2P is drawn as function of both V_{WL} and V_{CS}, in their respective operating ranges. As one can see, T2P decreases exponentially in both the cases, albeit with a higher rate with V_{CS}. In conclusion, it can be affirmed that, working at high V_{WL} and V_{CS} values entails a reduction in the T2P. Furthermore, a greater dependency of T2P on V_{WL}, respect to V_{CS}, can be verified.

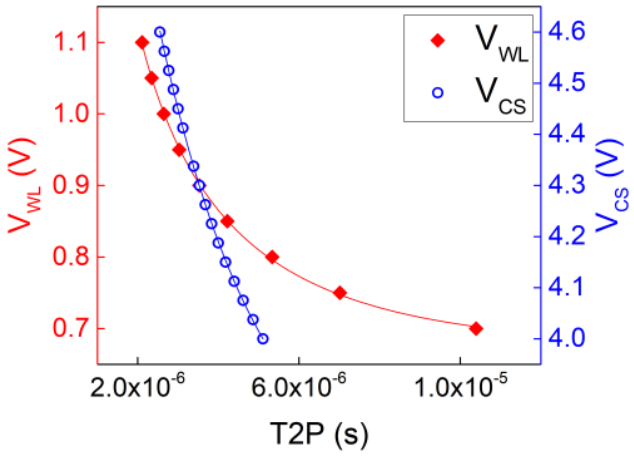


Figure 11. TCAD simulations of time-to-program drawn as function of V_{WL} (solid symbols) and V_{CS} (open symbols), in their respective operating ranges. The two solid lines are exponential interpolations.

In Figure 12a,b, a summary of the three aforementioned working quantities (V_{FG}, η and 1/T2P) dependency on V_{WL} and V_{CS} is reported. Concerning the V_{WL} increment, its detrimental impact on η (Figure 9) was assessed on one hand, but, on the other hand, its positive influence on V_{FG} and T2P (Figures 10 and 11) was also. This can be verified in Figure 12a, where two V_{WL} ranges are indicated: the best trade-off among all the three quantities lies at intermediate values of V_{WL} (dashed circle); the best solution in terms of V_{FG} and 1/T2P, regardless of η, rather requires higher V_{WL} values (solid circle). For what

concerns V_{CS}, as all the three quantities (η, 1/T2P and V_{FG}) contemporarily improve by increasing V_{CS}, a unique range is reported in Figure 12b (solid circle).

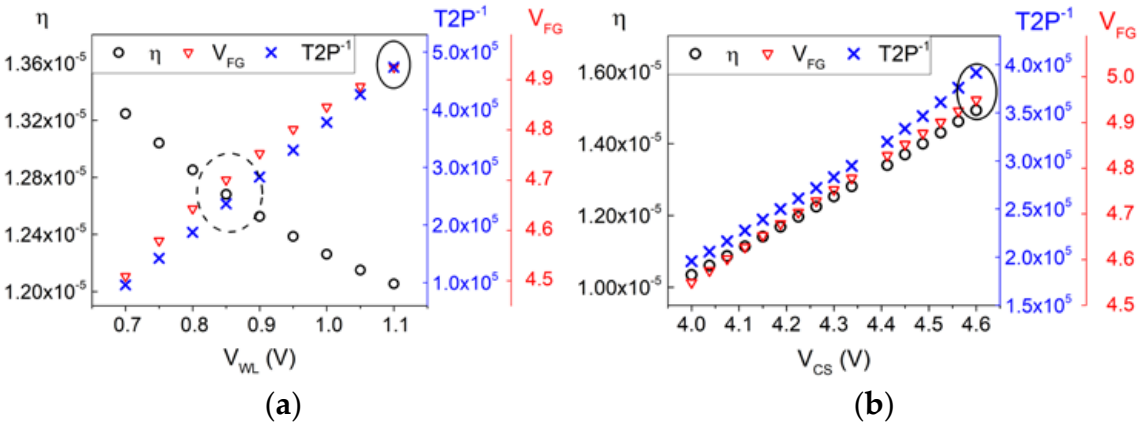


Figure 12. Summary of the three working quantities: V_{FG} (open triangles), η (open circles) and 1/T2P (crosses) drawn as function of (**a**) V_{WL} and (**b**) V_{CS}.

In conclusion, to improve the overall program operation it can be more convenient to intervene on the common source electrode rather than on the word line one. However, if in a specific application η (and therefore the power consumption) is a minor priority respect to program speed and program window, V_{WL} can be increased as well, alternatively or in addition to V_{CS}.

As a final remark, possible drawbacks of increasing V_{WL} and V_{CS} in terms of reliability are studied. First of all, by increasing V_{CS}, the total channel electric field E_{TOT} at X_{FG} increases as well, as shown in Figure 3b. Hence, an augmented lateral portion of the channel is involved in SSI, which in turn possibly leads to a widening of the interface traps amount in the injection area. The presence of these additional traps could cause an electrostatic shielding effect during program, as well as the activation of charge loss paths. Furthermore, the increment of V_{CS} can provoke channel pinch-off close to the CS edge, thus further increasing E_H (as depicted in Figure 13a), which in turn favors impact ionization and the possible creation of new traps at the Si/SiO_2 interface.

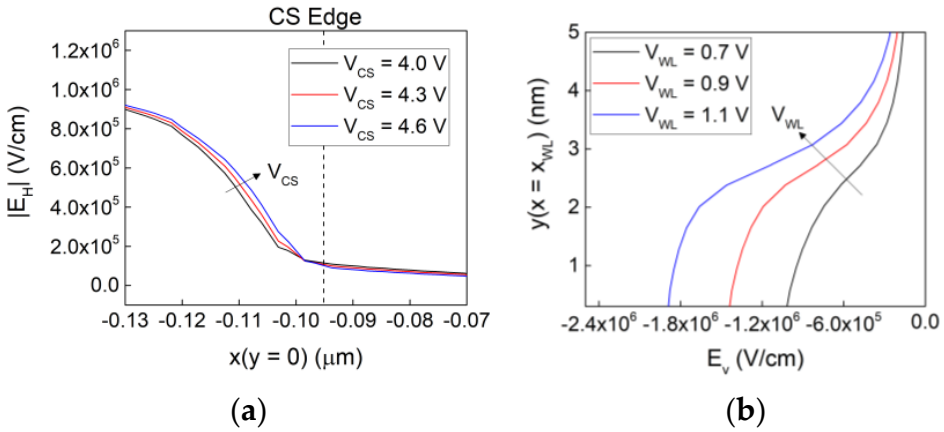


Figure 13. TCAD simulations of: (**a**) the horizontal component of the electric field (in absolute value) against the x coordinate in y = 0, at the CS edge with V_{CS} as a parameter; (**b**) the vertical component of the electric field against the y coordinate in x = X_{WL}, between the SiO_2 interface and the WL electrode with V_{WL} as a parameter.

Operating at high values of V_{WL} can also have different drawbacks. First of all, due to the electric field increment in the oxide at x = X_{WL} (shown Figure 13b), there exist a higher

probability of trap creation in this portion of the channel, which may alter the injection efficiency. Second, Figure 5 showed that the V_{WL} growth enhances also E_v at x = X_{FG}. This results in a greater amount of charge stored in the FG, but, on the other hand, leads to a more stressed Si/SiO_2 interface. Relying on the above considerations, it appears evident that, if the increment of both V_{WL} and V_{CS} brings undeniable benefits in terms of program speed and program window, it should be taken into account that they can possibly cause reliability degradation.

5. Conclusions

This work is focused on the program operation of ESF3 memory cells in the latest technology node currently on the market. TCAD numerical simulations of word line and common source electrodes influence on the SSI efficiency, the FG potential and the time-to-program were carried out using scaled cell geometry and voltages. Simulations showed that literature model proves to be suitable for common source voltage variations even in the current node. Conversely, the word line voltage effect on the electric field components was not properly represented by the mentioned model. Therefore, an analytical model of the electric field was proposed, which outlined the influence of the physical (and electrical) cell parameters on E_V. Particularly, excellent agreement between analytical and numerical values was attained, thus demonstrating a leading E_V impact on SSI mechanism, which actually determine the injection.

In addition, SSI efficiency η turned out to be (slightly) degraded by V_{WL} increment while the FG potential and the time-to-program improved at high values of the word line and common source voltages.

As a consequence, in order to improve the overall program operation, it can be more convenient to intervene on the common source electrode. However, in specific applications where the power consumption is a minor priority respect to program speed and program window, the word line voltage can be increased alternatively or in addition to common source.

Finally, as opposed to the benefits in terms of performance, V_{CS} and V_{WL} increment can cause electrical stresses in the oxide layers of the cell, with an increased risk of trap creation.

In conclusion, this work allows for a deeper comprehension of the technology scaling effects on the ESF3 cell physics in program operation. The achieved results pave the way for the implementation of innovative program strategies aimed to improve both performances and reliability in the ESF3 memory.

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References

1. Campbell, S.; O'Mahony, N.; Krpalcova, L.; Riordan, D.; Walsh, J.; Murphy, A.; Ryan, C. Sensor Technology in Autonomous Vehicles: A review. In Proceedings of the 2018 29th Irish Signals and Systems Conference (ISSC), Belfast, UK, 21–22 June 2018; pp. 1–4.
2. Taito, Y.; Kono, T.; Nakano, M.; Saito, T.; Ito, T.; Noguchi, K. A 28 nm Embedded Split-Gate MONOS (SG-MONOS) Flash Macro for Automotive. *IEEE J. Solid-State Circuits* **2016**, *51*, 213–221.
3. Kono, T. Embedded non-volatile memory system as an enabler of smarter world. In Proceedings of the 2017 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, 24–27 April 2017; pp. 1–4.
4. Available online: http://www.sst.com/technology/superflash-technology.aspx (accessed on 11 May 2020).

5. Sung, H.; Lei, T.F.; Hsu, T.; Kao, Y.; Lin, Y.; Wang, C.S. Characterization for Split-Gate Flash Cell. *IEEE Electron Device Lett.* **2005**, *26*, 194–196. [CrossRef]
6. Wu, T.; Chih, Y.; Chen, S.; Wang, W.; Chang, M.-C.; Shih, J.; Chin, H.; Wu, K. Characterization of split gate flash memory endurance degradation mechanism. In Proceedings of the 11th International Symposium on the Physical and Failure Analysis of Integrated Circuits. IPFA 2004 (IEEE Cat. No.04TH8743), Taiwan, 5–8 July 2004; pp. 115–117.
7. Markov, V.S.; Korablev, K.G.; Kotov, A.G.; Liu, X.; Jia, Y.; Dang, T.N.; Levi, A.F.J. Charge-gain program disturb mechanism in split-gate flash memory cell. In Proceedings of the 2007 IEEE International Integrated Reliability Workshop Final Report, South Lake Tahoe, CA, USA, 15–18 October 2007; pp. 43–47.
8. Montanari, D.; Van Houdt, J.; Wellekens, D.; Vanhorebeek, G.; Haspeslagh, L.; Deferm, L.; Groeseneken, G.; Maes, H. Multi-level charge storage in source-side injection flash EEPROM. In Proceedings of the Nonvolatile Memory Technology Conference, Albuquerque, NM, USA, 24–26 June 1996; pp. 80–83.
9. Wang, K.-T.; Chao, T.-S.; Chiang, T.-Y.; Wu, W.-C.; Kuo, P.-Y.; Wu, Y.-H.; Lu, Y.-L.; Liao, C.-C.; Yang, W.-L.; Lee, C.-H.; et al. Physical Mechanism of High-Programming-Efficiency Dynamic-Threshold Source-Side Injection in Wrapped-Select-Gate SONOS for nor-Type Flash Memory. *IEEE Electron Device Lett.* **2009**, *30*, 1206–1208. [CrossRef]
10. Shih, C.-H.; Liang, J.-T.; Wang, J.-S.; Chien, N.D. A source-side injection lucky electron model for schottky barrier metal-oxide-semiconductor devices. *IEEE Electron Device Lett.* **2011**, *32*, 1331–1333. [CrossRef]
11. Hidaka, H. Split-Gate Floating Poly SuperFlash®Memory Technology, Design, and Reliability. In *Embedded Flash Memory for Embedded Systems:Technology, Design for Sub-systems, and Innovations*; Springer: Berlin/Heidelberg, Germany, 2017.
12. Saha, K. Design considerations for sub-90-nm split-gate flash-memory cells. *IEEE Trans. Electron Devices* **2007**, *54*, 3049–3055. [CrossRef]
13. Guan, H.; Lee, D.; Li, G. An analytical model for optimization of programming efficiency and uniformity of split gate source-side injection superflash memory. *IEEE Trans. Electron Devices* **2003**, *50*, 809–815. [CrossRef]
14. Cho, C.Y.-S.; Chen, M.-J.; Chen, C.-F.; Tuntasood, P.; Fan, D.-T.; Liu, T.-Y. A novel self-aligned highly reliable sidewall split-gate flash memory. *IEEE Trans. Electron Devices* **2006**, *53*, 465–473.
15. Ma, Y.; Pang, C.; Pathak, J.; Tsao, S.; Chang, C.; Yamauchi, Y.; Yoshimi, M. A novel high density contactless flash memory array using split-gate sources-side-injection cell for 5 V-only applications. In Proceedings of the 1994 VLSI Technology Symposium, Honolulu, HI, USA, 7–9 June 1994; pp. 49–50.
16. Kamiya, M.; Kojima, Y.; Kato, Y.; Tanaka, K.; Hayashi, Y. EPROM cell with high gate injection efficiency. In Proceedings of the 1982 International Electron Devices Meeting, San Francisco, CA, USA, 13–15 December 1982; pp. 741–744.
17. Yamauchi, Y.; Kamakura, Y.; Matsuoka, T. A Source-Side Injection Single-Poly Split-Gate Cell Technology for Embedded Flash Memory. In Proceedings of the 2013 International Conference on Solid State Devices and Materials, Hilton Fukuoka Sea Hawk, Fukuoka, Japan, 24–27 September 2013; pp. 110–111.
18. Tkachev, Y.; Kotov, A. A detailed analysis of hot-electron programming efficiency in 40-nm split-gate flash memory cells. In Proceedings of the 2017 IEEE International Memory Workshop (IMW), Monterey, CA, USA, 14–17 May 2017; pp. 7–10.
19. Shum, D.; Luo, L.Q.; Kong, Y.J.; Deng, F.X.; Qu, X.; Teo, Z.Q.; Liu, J.Q.; Zhang, F.; Cai, X.S.; Tan, K.M.; et al. 40nm Embedded self-Aligned split-gate flash technology for high-density Aautomotive microcontrollers. In Proceedings of the 2017 IEEE International Memory Workshop (IMW), Monterey, CA, USA, 14–17 May 2017; pp. 6–9.
20. Jourba, S.; Bollon, N.; Decobert, C.; Festes, G.; Bertello, B.; Zhou, F.; Markov, V.; Tkachev, Y.; Kim, J.; Ghazav, P.; et al. Performance and Reliability of 4 Mb eFLASH Memory Array Featuring 28 nm Split-Gate Cell with HKMG Select Transistor. In Proceedings of the 2020 IEEE International Memory Workshop (IMW), Dresden, Germany, 17–20 May 2020; pp. 1–4.
21. Richter, R.; Trentzsch, M.; Dunkel, S.; Muller, J.; Moll, P.; Bayha, B.; Mothes, K.; Henke, A.; Mazur, M.; Paul, J.; et al. A cost-efficient 28nm split-gate eFLASH memory featuring a HKMG hybrid bit cell and HV device. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 1–4.
22. Do, N.; Kim, J.; Lemke, S.; Tee, L.; Tkachev, Y.; Liu, X.; Ghazavi, P.; Zhou, F.; Villard, B.; Jourba, S.; et al. Scaling split-gate flash memory technology for advanced MCU and emerging applications. In Proceedings of the 2019 IEEE 11th International Memory Workshop (IMW), Monterey, CA, USA, 12–15 May 2019; pp. 1–4.
23. Wu, C.-M.; Liu, S.-C. Split gate flash memory structure and method of making the split gate flash memory structure. U.S. Patent No. 9,614,048, 4 April 2017.
24. Do, N.; Yang, J.; Sheng, Y.J.; Su, C.S.; Wu, M.T.; Ouyang, H.; Liang, H.; Hariharan, S.; Tadayoni, M.; Norman, J.; et al. Scaling of Split-Gate Flash Memory with 1.05V Select Transistor for 28 nm Embedded Flash Technology. In Proceedings of the 2018 IEEE International Memory Workshop (IMW), Kyoto, Japan, 13–16 May 2018; pp. 1–3.
25. Yamauchi, Y.; Kamakura, Y.; Matsuoka, T.; Ueda, N. Source-side injection single-polysilicon split-gate flash memory. *Jpn. J. Appl. Phys.* **2014**, *53*, 34201. [CrossRef]