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Output Voltage Ripple Reduction in a Symmetric Multistage-Stacked Boost Architecture (MSBA) Converter

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Abstract: This article proposes a different operation mode in a recently proposed converter, the multistage-stacked boost architecture (MSBA) converter working under the symmetric operation mode. The operation mode of the converter is analyzed with a modified pulse width modulation (PWM) scheme, in which the switching function of transistors is obtained from an interleaved scheme. The results show that the modified PWM results in a similar operation of the converter, with a reduced output voltage ripple, without increasing the switching frequency. A mathematical model of the converter is provided, the output voltage ripple calculation is performed in the traditional, and the modified PWM scheme, simulation, and experimental results are provided to verify the operation mode and the obtained equations.

Keywords: boost converter; multistage-stacked boost architecture; pulse width modulation converter

1. Introduction

The power electronics field is related to the electrical energy transformation through electronic components; one of their specific fields is the development of large voltage gain dc–dc converters [1], which are important in renewable energy generation systems and other environmentally friendly applications [2], for example, in photovoltaic (PV) panels or fuel cells (FCs), in which the dc voltage that comes from the PV panel or the FC, must be increased from some dozens of volts to some hundreds of volts.

There are traditional topologies, such as the buck, boost, or buck–boost converter, some of them has the capability to increase the input voltage, but the required voltage gain can be too large for traditional topologies [3], manufacturers of integrated circuits for the control of power converters, usually do not warranty their circuits can work with duty cycles larger than 0.75 or 0.8, which would limit the operation of traditional converters to voltage-gains of around five [3] (the definition of duty cycle and their relation to voltage gain will be further explained).

A solution to achieve a large voltage gain is the use of transformers or coupled inductors [1], but transformer-less converters can be manufactured with available commercial components (off-the-shelves), which make them attractive, while magnetic-coupling based converters, based for example on transformers or coupled inductors, usually require the magnetic component to be designed in a custom manner. On the other hand, the magnetic coupling may provide electrical isolation to the converter. If electrical isolation is not required, transformer-less topologies are cheaper, and their manufacturing process is faster.

Other solutions to achieve large voltage gain are the use of voltage multipliers combined with traditional converters [4–6], or quadratic topologies [7,8].

Additionally, then, the research on transformer-less topologies is an active field. One of the recently investigated transformer-less dc–dc boost converter topologies is the so-called, multistage-stacked boost architecture (MSBA) converter, initially introduced in [9,10], has been studied in other works of the literature; for example, their control has been studied in [11]. In contrast to other large voltage gain topologies, such as other quadratic topologies,

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the MSBA converter allows one to increase the structure and attain voltage levels that are higher than the blocking capability of the semiconductor devices [9], their structure can be extended with similar building blocks. On the other hand, it has two transistors in contrast to other dc–dc converters, which utilizes a single switch; furthermore, if the structure is extended, more transistors are required.

This article analyzes the operation mode of the multistage-stacked boost architecture MSBA converter working under symmetric operation mode, and it proposes a new operation mode with a modified pulse width modulation (PWM) scheme. In the modified PWM scheme, the switching functions of transistors are obtained from an interleaved PWM and shifted 180°. The interleaved PWM has been utilized in several studies to reduces the input current ripple in converters [12]; this work is focused on the output voltage ripple.

The results show that the modified PWM results in a similar operation of the converter; it has the same equilibrium and the same power rating in all devices, but it offers a reduction on the output voltage ripple without increasing the switching frequency; if the switching frequency can be increased, the designer still can choose the proposed strategy and achieve a smaller voltage ripple compared to the former strategy. A mathematical model of the converter is provided, the output voltage ripple calculation is performed in the traditional, and the modified PWM scheme, simulation, and experimental results are provided to verify the operation mode and the obtained equations.

2. The MSBA Converter with Non-Interleaved PWM

The topology understudy is depicted in Figure 1. It is composed of two inductors L_1 and L_2, two capacitors C_1 and C_2, two transistors s_1 and s_2, and two diodes s_{1n} and s_{2n}. Diodes switch complementary with transistors; when a transistor is closed, their complementary diode is open, and vice-versa; the subtitle "n" (from "*not*") in the name of diodes indicates their complementary transistor, s_{1n} is complementary to s_1, and s_{2n} is complementary to s_2.

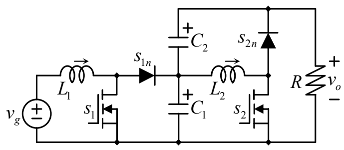

Figure 1. The multistage-stacked boost architecture (MSBA) converter.

In the symmetric operation mode, both transistors share the same switching function s_x and duty cycle D; Figure 2a shows the block diagram of the pulse width modulation (PWM) scheme at the former operation mode of the converter, and Figure 2b shows important waveforms in this process, the first four signals are the state variables of the converter, the current through both inductors and the voltage across capacitors' terminals. At the button of Figure 2b, the switching function s_x is shown over the triangular carrier and the duty cycle signal, which are depicted together at the button of the figure.

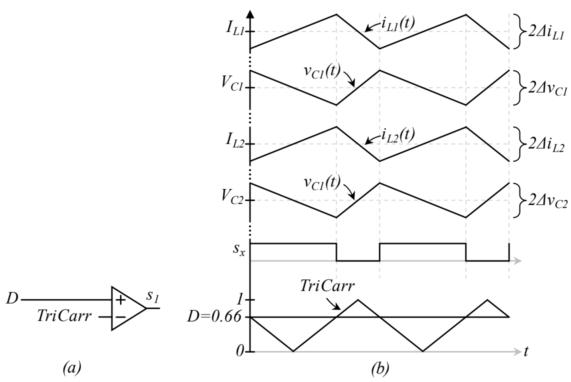

Figure 2. Pulse width modulation (PWM) scheme of the series-capacitor boost converter.

The switching function s_x, also called the PWM signal, is obtained by comparing the dc signal "D" (which can take values between 0 and 1) against a triangular carrier TriCarr. The switching function $s_x = 1$ when D is larger than TriCarr, and $s_x = 0$ when D is below the signal TriCarr.

The operation of the converter produces two different switching states or equivalent circuits, Figure 3a shows the equivalent circuit of the converter when $s_x = 1$, both transistors are closed, and diodes are reversely polarized (s_{1n} whit V_{C1} and s_{2n} with $V_{C1} + V_{C2}$).

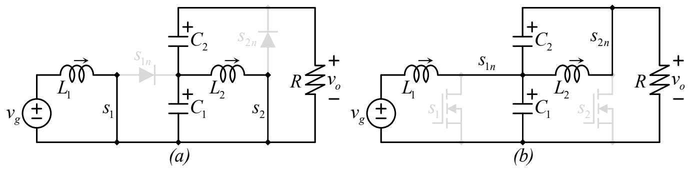

Figure 3. (**a**) Switching state when $s_1 = 1$ and $s_2 = 1$, (**b**) Switching state when $s_1 = 0$ and $s_2 = 0$.

Those switching states lead to two different mathematical models; by following the Kirchhoff voltage law (KVL) and the Kirchhoff current law (KCL), the mathematical model of the circuit shown in Figure 3a is given by (1) and (2).

$$L_1 \frac{di_{L1}}{dt} = v_g; \quad L_2 \frac{di_{L2}}{dt} = v_{C1} \tag{1}$$

$$C_1 \frac{dv_{C1}}{dt} = -i_{L2} - i_o; \quad C_2 \frac{dv_{C2}}{dt} = -i_o \tag{2}$$

Being C_1 and C_2 the capacitance of their respective capacitors; L_1 and L_2 the inductance of inductors; v_{C1} and v_{C2} the voltage across capacitors C_1 and C_2; i_{L1} and i_{L2} the currents through inductors L_1 and L_2; v_g is the input voltage; and i_o is the output current, the current through the output resistor, which in this case is equal to $(v_{C1} + v_{C2})/R$.

The mathematical model of the circuit shown in Figure 3b is given by (3) and (4).

$$L_1 \frac{di_{L1}}{dt} = v_g - v_{C1}; \quad L_2 \frac{di_{L2}}{dt} = -v_{C2} \tag{3}$$

$$C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_0; \quad C_2 \frac{dv_{C2}}{dt} = i_{L2} - i_o \tag{4}$$

Now the traditional averaging technique [1] can be used to determine the full average model. However, first, let's remind that the duty cycle D is defined as the relation of the time period in which a transistor is closed, divided over the total switching period T_S. The remainder of the average time (in which the transistor is open) can be expressed as $(1 - D)$. From this definition, the time period in which the circuit behaves like Figure 3a is equal to DT_S, and the time in which the circuit behaves like Figure 3b is equal to $(1 - D)T_S$. In order to obtain the average model, the value of variables in each switching state can be multiplied by the time each switching state holds and divided over the total switching period T_S. This leads to:

$$L_1 \frac{di_{L1}}{dt} = d(v_g) + (1 - d)(v_g - v_{C1}) \tag{5}$$

$$L_2 \frac{di_{L2}}{dt} = d(v_{C1}) + (1 - d)(-v_{C2}) \tag{6}$$

$$C_1 \frac{dv_{C1}}{dt} = d(-i_{L2} - i_o) + (1 - d)(i_{L1} - i_o) \tag{7}$$

$$C_2 \frac{dv_{C2}}{dt} = d(-i_o) + (1 - d)(i_{L2} - i_o) \tag{8}$$

The term T_S is not present since it is canceled during the averaging process; furthermore, the lowercase "d" is used instead of the uppercase "D", in general, lowercase letters are used to indicate that signals can change (are variables), and uppercase letters are used to indicate they operate in steady-state (considered as constant in this specific condition). The average model in (5)–(8) can be further simplified to the model in (9)–(12).

$$L_1 \frac{di_{L1}}{dt} = v_g - (1-d)v_{C1} \tag{9}$$

$$L_2 \frac{di_{L2}}{dt} = dv_{C1} - (1-d)v_{C2} \tag{10}$$

$$C_1 \frac{dv_{C1}}{dt} = -di_{L2} + (1-d)i_{L1} - i_o \tag{11}$$

$$C_2 \frac{dv_{C2}}{dt} = (1-d)i_{L2} - i_o \tag{12}$$

The mathematical model described in (9)–(12) is sometimes called the non-linear, or full average, or large-signal model of the converter; from this large-signal model, the steady-state condition or equilibrium can be obtained when derivatives are equal to zero, the equilibrium is calculated (13) and (14).

$$V_{C1} = \frac{V_g}{1-D}; \quad V_{C2} = \frac{D}{1-D}V_{C1} = \frac{D}{(1-D)^2}V_g \tag{13}$$

$$I_{L1} = \frac{I_0}{(1-D)^2}; \quad I_{L2} = I_0\frac{1}{1-D} \tag{14}$$

Finally, the output voltage of the converter, see Figure 1, is given by the series connection of both capacitors, the output voltage is then the summation of V_{C1} + V_{C2}, and finally expressed in terms of the input voltage V_g and the duty cycle D as (15).

$$V_o = V_{C1} + V_{C2} = \frac{V_g}{(1-D)^2} \cdot I_o = \frac{V_o}{R} \tag{15}$$

The equilibrium described in (13) and (14) is similar to the equilibrium of the classical quadratic boost converter. The discussed converter is also a quadratic boost, which can be observed from their output voltage (15). One advantage of the MSBA converter against the quadratic boost is that capacitor C_2 has less voltage rating, which has an impact on the size of the converter; on the other hand, it requires two transistors, while the traditional quadratic boost requires only one.

The Output Voltage Ripple

The output voltage ripple is an important parameter to define the power quality of the converter; it is desired to have an output voltage as pure (or clean) as possible, which means as free of switching ripple as possible. A pure DC signal would be desirable, but this is impossible; it would require an infinitely large capacitance. The output voltage ripple can be reduced by choosing larger capacitors, but this brings a compromise between the size of the converter and the output voltage ripple.

As described ahead, the MSBA converter can offer an advantage in this matter when it is operated with the modified PWM scheme, but first, the traditional operation mode is described to have a comparison point.

The voltage ripple in each capacitor can be calculated considering that their voltage decreases when then transistors are closed; since their current is negative in this particular switching state, this lasts for a time period equal to DT_S. The derivative of the voltage or voltage slope in a capacitor is equal to their current divided over the capacitance $dv/dt = I/C$. Considering that the voltage ripple in C_1 and C_2 can be calculated as:

$$\Delta v_{C1} = DT_S \frac{(I_{L2} + I_o)}{2C_1}; \quad \Delta v_{C2} = DT_S \frac{I_o}{2C_2}. \tag{16}$$

The ripple is an absolute value, and then the current through the capacitor can be expressed as positive; the number 2 comes from the fact that the ripple is defined as the maximum deviation from the average voltage; the average is at the middle point in the triangular waveform. Peak to peak variation in Figure 2 is labeled as twice of the ripple.

Similarly to the switching ripple in capacitors voltage, there is a switching ripple in inductors currents, and they can be similarly calculated [1]; this article focuses on the voltage ripple.

From Figure 2, the ripples in capacitors are in phase, the voltage in capacitors rise and fall at the same time, capacitors are connected in additive series, which produces that the output voltage ripple is the summation of the ripple in individual capacitors.

$$\Delta v_o = \frac{DT_S}{2}\left(\frac{I_{L2} + I_o}{C_1} + \frac{I_o}{C_2}\right) \tag{17}$$

3. The MSBA Converter in the Proposed Operation Mode

The proposed operation mode of the MSBA converter is based on an interleaved PWM scheme, and shown in Figure 4, like the PWM scheme in interleaved converters, there is a single duty cycle signal, but two triangular carriers shifted 180°, called in this case s_{1Carr} and s_{2Carr} switching functions of transistors are different, but they have the same duty cycle (the same proportion of time in the closed position of the switch).

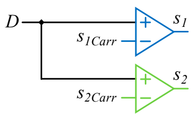

Figure 4. PWM scheme in the proposed operation mode.

The proposed operation mode is more complex to analyze than the former operation mode for the following reason, in the former operation mode, there were two transistors operating with the same switching functions; this produces only two switching states, or equivalent circuits, as shown in Figure 3. Having only two switching states simplifies the averaging process. However, if each transistor has their own switching function, there are four possible switching states, which are shown in Figure 5, those switching states are: (i) $s_1 = 1$ and $s_2 = 0$, (ii) $s_1 = 0$ and $s_2 = 1$, (iii) $s_1 = 1$ and $s_2 = 1$, and (iv) $s_1 = 0$ and $s_2 = 0$.

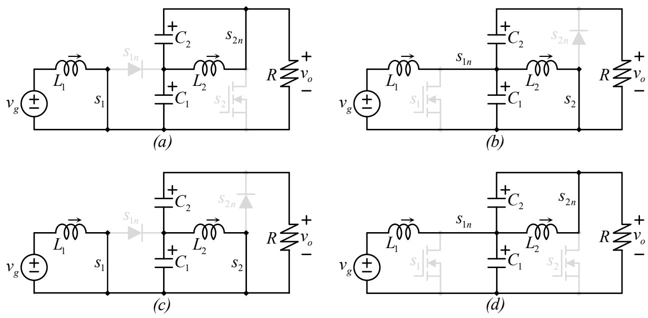

Figure 5. Equivalent circuit according to the switching state (**a**) $s_1 = 1$ and $s_2 = 0$, (**b**) $s_1 = 0$ and $s_2 = 1$, and (**c**) $s_1 = 1$ and $s_2 = 1$, and (**d**) $s_1 = 0$ and $s_2 = 0$.

Even if the number of possible switching states is four, the number of switching states that appears during the operation mode is three (two in a particular point), and they depend on the value of the duty cycle D. The duty cycle D may change during the operation, adjusted by a controller (for example, a PID controller), to maintain the output voltage in a certain desired value. The operation of the converter can be classified in three possible cases (when $D < 0.5$, $D = 0.5$, and $D > 0.66$). Figure 6 shows three particular cases (when $D = 0.33$, $D = 0.5$, and $D = 0.66$) to exemplify how switching functions would look like and to observe how the different equivalent circuits may appear.

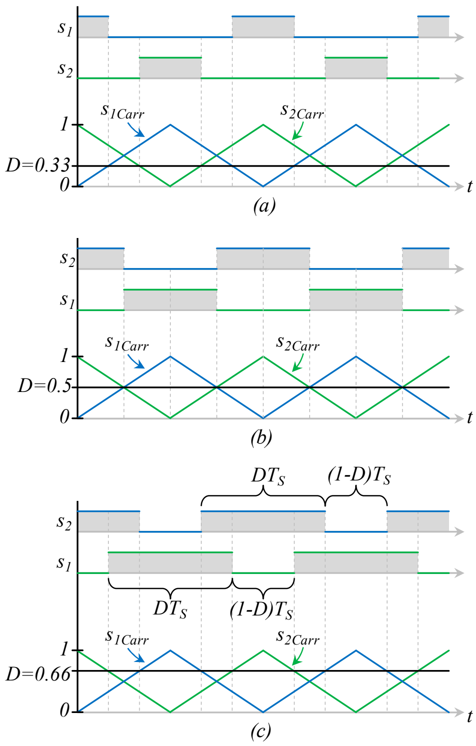

Figure 6. PWM and switching functions for different cases of the duty cycle: (**a**) when $D = 0.33$, (**b**) when $D = 0.5$, and (**c**) when $D = 0.66$; in this last case, time-period calculations are shown.

Case $D < 0.5$: When the duty cycle is smaller than 0.5, PWM signals are as shown in Figure 6a; the low value of D causes each switch to close for a short period of time, and the second transistor to close after a time in which both signals are off (a digital 0). There is not a time in which both transistors are closed at the same time (signals blue and gray are not high simultaneously in Figure 6a, and then the switching state in Figure 5c did not appear, all other three switching states in Figure 5 ($s_1 = 1$ and $s_2 = 0$, $s_1 = 0$ and $s_2 = 1$, and $s_1 = 0$ and $s_2 = 0$) are present in this operation mode.

Case $D = 0.5$: In this particular case, only two switching states are present, see Figure 6b; those switching states are when transistors are $s_1 = 1$ and $s_2 = 0$, and $s_1 = 0$ and $s_2 = 1$ (see Figure 5a,b). This particular case can be analyzed as any of the other two cases in their boundary case.

Case $D > 0.5$: This operation mode is shown in Figure 6c, which in contrast to other diagrams in Figure 6, the time calculations for the different periods are also shown; this is because this operation mode is the focus of this article. In this operation mode, there is not a time in which both transistors are open at the same time, but there is a time in which both transistors are closed at the same time. The switching states that appear during this operation mode are $s_1 = 1$ and $s_2 = 0$, $s_1 = 0$ and $s_2 = 1$, and $s_1 = 1$ and $s_2 = 1$.

Despite the four possible combinations of switch positions, the proposed operation mode does not affect the mathematical model; at the end of the averaging, the mathematical model of the converter is still described by Equations (9)–(12). That means the proposed operation provides the same dynamic performance to the MSBA converter, compared to the former strategy. The equilibrium is also described as (13) and (14). Equations are not repeated for convenience. The difference is the calculation of the output voltage ripple, which is certainly different to (17).

The Output Voltage Ripple in the Proposed Operation Mode

Before providing the equations to calculate the output voltage ripple in the proposed operation mode, a discussion about the ripple origin may improve the understanding of the principle.

In the former operation mode, during any of both switching states (see Figure 3), both capacitors are getting charged or discharged at the same time. In Figure 3a, capacitor C_1 is getting discharged with $I_{L2} + I_o$, while capacitor C_2 is getting discharged with I_o; both capacitors (which are series-connected) are getting discharged at the same time. On the other hand, in Figure 3b, capacitor C_1 is getting charged with $I_{L1} - I_o$ (is getting charged since I_o is smaller than I_{L1} as stated in (14)), while capacitor C_2 is getting charged with $I_{L2} - I_o$ (is getting charged since I_o is smaller than I_{L2} as stated in (14)). The conclusion is that both capacitors get charged or discharged at the same time, and then the ripple of individual capacitors gets a cumulative contribution to the output voltage ripple.

In the proposed operation mode, the discussed switching states are also present; notice that Figure 3a is equal to Figure 5c, and Figure 3b is equal to Figure 5d, but the other two switching state are present in which one capacitor is getting charged while the other one is getting discharged, and thus represent a non-cumulative contribution to the output voltage ripple.

In Figure 5a, capacitor C_1 is getting discharged with I_o, while capacitor C_2 is getting charged with $I_{L2} - I_o$. On the other hand, in Figure 5b, capacitor C_1 is getting charged with $I_{L1} - I_{L2} - I_o$, while capacitor C_2 is getting charged with I_o. The conclusion is that in those new switching states, one capacitor gets charged while the other gets discharged, and vice-versa; this behavior helps to reduce the output voltage ripple since the ripple of individual capacitors does not get a cumulative contribution to the output voltage ripple.

To calculate the output voltage ripple in the proposed operation mode of the MSBA converter, we must consider that the maximum voltage variations (the switching ripple) can be present on one of the new switch states, the one shown in Figure 5a, or the one shown in Figure 5b, this depends on the duty cycle (as explained the new operation mode has two different sets of switching states (see Figure 6). Additionally, From Figure 6, both new switching states hold for a time $(1 - D)T_S$. The expression for the output voltage ripple is then the largest value of those ripples expressed in (18) and (19), respectively.

$$\Delta v_{oN1} = \frac{(1-D)T_S}{2}\left(\frac{I_{L1} - I_{L2} - I_o}{C_1} - \frac{I_o}{C_2}\right) \tag{18}$$

$$\Delta v_{oN2} = \frac{(1-D)T_S}{2}\left(\frac{-I_o}{C_1} + \frac{I_{L2} - I_o}{C_2}\right) \tag{19}$$

Equations (18) and (19) will provide different values, but as will be shown in the next section, both have a smaller ripple compared to (17) for the same size of devices and power rating, without increasing the switching frequency, if the switching frequency can be larger, the designer still can choose the proposed strategy and achieve a smaller voltage ripple compared to the former strategy, the best choice would be the combination of the proposed strategy with the largest possible switching frequency (the switching frequency of the design can be limited by the semiconductors technology and the losses).

Figure 7 shows a zoom into the theoretical waveforms of the output voltage ripple; Figure 7a shows the former strategy; only two switching states are present, the state in which both transistors are on (Figure 5c) and the state in which both switches are off (Figure 5d), Figure 7 shows the derivative of the output voltage as the summation of the derivative of voltages across both capacitors, as it can be observed Equation (17) corresponds to the time in which transistors are closed, and both capacitors are getting discharged.

Figure 7b shows the zoom intro the output voltage ripple in the proposed strategy, the falling derivative is always the same, since the switching state is also the one shown in Figure 5c, when both transistors are closed, on the other hand, the rising derivative may be produced for two different switching states, when s_1 is closed while s_2 is open (Figure 5a), and when s_1 is open while s_2 is closed (Figure 5b). Those two rising derivatives were used to determine (18) and (19).

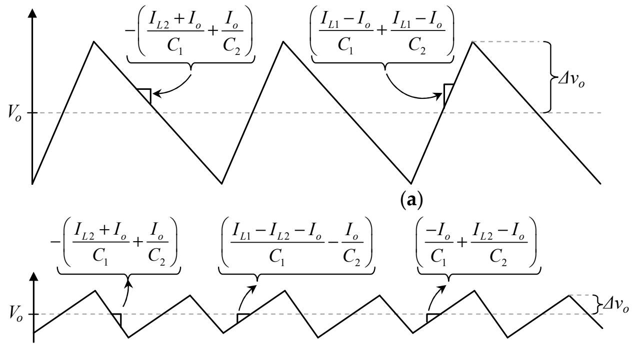

Figure 7. Zoom into the output voltage ripple (**a**) in the former strategy and (**b**) in the proposed strategy.

4. Comparative Evaluation and Discussion

In this section, two MSBA converters with the same design are compared, with the former and the proposed operation mode; as mentioned before, the equilibrium does not change, both converters have the same power rating, but the output voltage ripple is smaller for the proposed operation mode within the full operating range. Both converters have equal inductance in inductors $L_1 = L_2 = 330$ µH; the switching frequency is selected as 50 kHz. The capacitance of capacitors was initially selected as $C_1 = C_2 = 20$ µF for both capacitors, then two additional cases with different capacitance were tested.

The comparative evaluation is based on the numerical simulation of a real application, in which an MSBA boost converter is fed with a fuel cell (FC), which voltage varies from 20 to 25 V, the output voltage is expected to be a constant 200 V dc bus, which feeds a grid-tie inverter. The power varies linearly depending on the FC parameters; the maximum voltage was attained when the minimum current was drawn from the FC, the minimum current was 2A; on the other hand, the minimum voltage was attained when the maximum current was drawn from the FC, the maximum current is 10 A. Those parameters are similar to the operation of a real FC; see FCS-C200 from [13].

Figure 8 shows the output voltage ripple for the former operation mode and the new operation mode (both Equations (18) and (19)) vs. the input voltage; it can be observed that the proposed operation mode achieved a lower output voltage ripple for the full operating range.

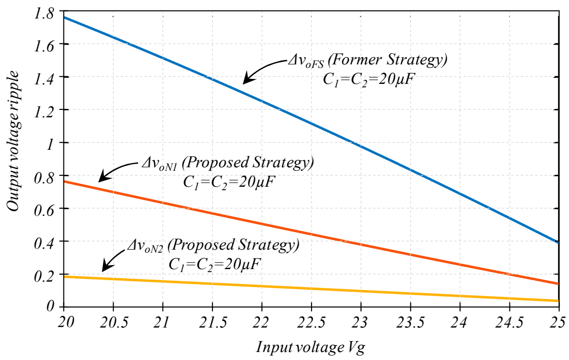

Figure 8. Output voltage ripple calculation for the full operation range with $C_1 = C_2 = 20$ µF.

Similar to Figures 8 and 9 the output voltage ripple is shown, but in this case, the value of capacitors was different, in this case, C_1 = 20 µF while C_2 = 10 µF, the change has been done to show how the largest value of the ripple in Equations (18) and (19), depends on the duty cycle and the value of capacitors, in this case, for an input voltage smaller than 22 V, the output voltage ripple of the proposed strategy must be calculated with Equation (18), on the other hand, for an input voltage larger than 22 V, the output voltage ripple of the proposed strategy must be calculated with Equation (19), both equations must be evaluated, and the largest value must be considered as the output voltage ripple. Despite that Equations (18) and (19) provided a smaller output voltage ripple compared to the former operation mode for the entire operating range.

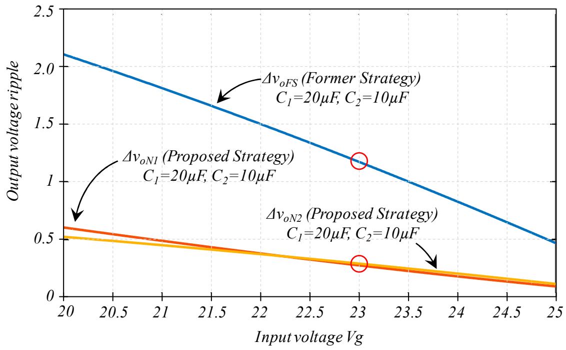

Figure 9. Output voltage ripple calculation for the full operation range with C_1 = 20 µF and C_2 = 10 µF, red circles indicate the operation point of the simulation shown in Figure 10.

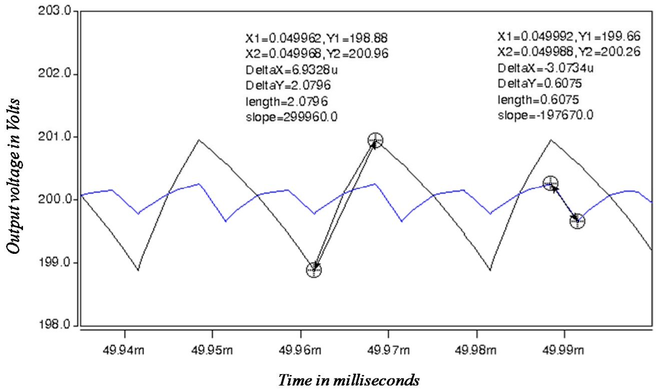

Figure 10. Zoom into the output voltage to measure the switching ripple.

A particular point in Figure 9 is marked with red circles; Figure 10 shows the simulation results for the output voltage in this particular point. The output voltage was 200 V dc with a small ripple; the figure shows a zoom in, in which (only) 5 V are shown (from 198 to 203 V); the zoom was made to appreciate the ripple, it seemed the voltage was well regulated to 200 V, the output voltage of a converter controlled in the former strategy is shown in black color, the output voltage ripple for the proposed strategy is shown in blue, a couple of measurement shows the peak-to-peak the ripple in the DeltaY measurement. Reminder that the peak-to-peak ripple is twice of Equations (17)–(19). Values can vary in a small percentage since Matlab calculates the equations, and the Synopsys Saber simulator provides a switched simulation with all parameters of components, including losses and parasitic elements.

As another example, we could reduce the capacitance of capacitors and obtain similar (or superior) performance with smaller capacitors; the last example, shown in Figure 11, compares the former operation mode with capacitors of C_1 = 20 µF and C_2 = 10 µF, against the proposed operation mode with capacitors of C_1 = 6.8 µF and C_2 = 3.3 µF. Figure 11 shows that even with smaller capacitors, the proposed operation mode achieved a smaller output voltage ripple in the entire operating range.

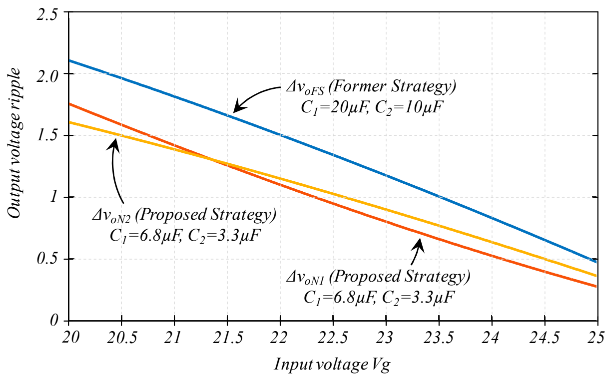

Figure 11. Former operation mode with C_1 = 20 µF and C_2 = 10 µF vs. the proposed operation mode with C_1 = 6.8 µF and C_2 = 3.3 µF.

5. Design Analysis and Experimental Results

An experimental prototype was built to demonstrate the principle of the proposed operation mode. Figure 12 shows the schematic of the experiment, which is an MSBA converter with synchronous rectification, which means the bidirectional power flow is possible, but only their boost function was performed.

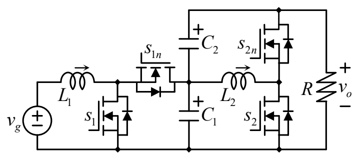

Figure 12. The schematic of the experimental test bench.

5.1. Design Description

This section describes the design of the converter, which was simulated and implemented for experimental results. Similar to the comparative evaluation, the output voltage was chosen as 200 V, and the input voltage ranges from 20 to 25 V, the switching frequency was selected as 50 kHz, and the output or load resistor was 385 Ω.

With the provided information, the maximum and minimum operation points can be determined; when V_g = 20 V, the operation point can be calculated as (20) and (21).

$$G_{25} = \frac{200}{25} = 8 \tag{20}$$

$$G_{20} = \frac{200}{20} = 10 \tag{21}$$

For a certain gain, the duty cycle can be determined as (22).

$$G = \frac{1}{(1-D)^2} \Rightarrow D = \frac{\sqrt{G}-1}{\sqrt{G}}. \tag{22}$$

Additionally, then the minimum and maximum duty cycle can be determined as (23) and (24).

$$D_{25} = \frac{\sqrt{8}-1}{\sqrt{8}} = 0.6464 \tag{23}$$

$$D_{20} = \frac{\sqrt{10}-1}{\sqrt{10}} = 0.6838 \tag{24}$$

The equilibrium described in (13) and (14), would have the following operation points. For V_g = 25:

$$V_{C1\_25} = \frac{25}{1-0.6464} = 70.7107 \tag{25}$$

$$V_{C2\_25} = \frac{0.6464}{(1-0.6464)^2} \times 25 = 129.2893 \tag{26}$$

$$I_{L1\_25} = \frac{1}{(1-0.6464)^2} \times \frac{200}{385} = 4.1558 \tag{27}$$

$$I_{L2\_25} = \frac{1}{(1-0.6464)} \times \frac{200}{385} = 1.4693 \tag{28}$$

Additionally, for V_g = 20:

$$V_{C1\_20} = \frac{25}{1-0.6838} = 63.2456 \tag{29}$$

$$V_{C2\_20} = \frac{0.6838}{(1-0.6838)^2} \times 20 = 136.7544 \tag{30}$$

$$I_{L1\_20} = \frac{1}{(1-0.6838)^2} \times \frac{200}{385} = 5.1948 \tag{31}$$

$$I_{L2\_20} = \frac{1}{(1-0.6838)} \times \frac{200}{385} = 1.6427 \tag{32}$$

One of the advantages of the MSBA converter was more evident; a traditional quadratic boost converter would require C_2 to be rated to 200 V.

5.1.1. Inductors

After the equilibrium calculations, the inductance in inductors and capacitance in capacitors is chosen based on the desired percentage of switching ripple allowed in components. Let us start with the inductance of inductors; the equations of the ripples are expressed in (33) and (34).

$$\Delta i_{L1} = DT_S \frac{V_g}{2L_1} \tag{33}$$

$$\Delta i_{L2} = DT_S \frac{V_{C1}}{2L_2} \tag{34}$$

In most boost type dc–dc converters, the selection of inductors is related to the input current ripple. A common design parameter is to choose inductors to have an input current ripple of a maximum of 10% (for example), internal inductors (inductors whose current ripple has no effect on the input current ripple and may have a larger current ripple. It is always desired to have a small current ripple, but the drawback is the size of inductors, and then an equilibrium among having large (and heavy) inductors against having a large input current ripple is a decision of the designer.

In this case, L_1 and L_2 were chosen as 440 μH; this allows one to have a current ripple of 8.8% in the worst case (L_1 when V_g = 25).

Now we can proceed to calculate the current ripple and then the peak current (dc plus the ripple) of inductors; this peak current must be smaller than the saturation current of inductors (the current in which the magnetic core gest their saturation flux level).

For V_g = 25:

$$\Delta i_{L1-25} = 0.6464 \times 20 \times 10^{-6} \frac{25}{2 \times 440 \times 10^{-6}} = 0.3673 \tag{35}$$

$$\Delta i_{L2-25} = 0.6464 \times 20 \times 10^{-6} \frac{70.7107}{2 \times 440 \times 10^{-6}} = 1.0389 \tag{36}$$

For V_g = 20:

$$\Delta i_{L1-20} = 0.6838 \times 20 \times 10^{-6} \frac{25}{2 \times 440 \times 10^{-6}} = 0.3108 \tag{37}$$

$$\Delta i_{L2-20} = 0.6838 \times 20 \times 10^{-6} \frac{63.2456}{2 \times 440 \times 10^{-6}} = 0.9829 \tag{38}$$

The maximum or peak currents in inductors in the extreme operation points are then expressed as in Equations (39)–(42)

For V_g = 25:

$$I_{L1-Peak25} = I_{L1-25} + \Delta i_{L1-25} = 4.5231 \tag{39}$$

$$I_{L2-Peak25} = I_{L2-25} + \Delta i_{L2-25} = 2.5082 \tag{40}$$

For V_g = 20:

$$I_{L1-Peak20} = I_{L1-20} + \Delta i_{L1-20} = 5.5056 \tag{41}$$

$$I_{L2-Peak20} = I_{L2-20} + \Delta i_{L2-20} = 2.6256 \tag{42}$$

The inductors saturation current must be rated to the values provided by (41) and (42), plus a safety margin. Now the root-mean-square (RMS) value of the current through inductors can be calculated; since the current is the traditional DC value plus a triangular ripple, we can use the Equation (43), provided in Appendix A of [1].

$$I_{RMS} = I_{DC} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{I_{DC}}\right)^2} \tag{43}$$

where I_{DC} is the average or dc value of the current and Δi, the switching ripple.

For V_g = 25:

$$I_{L1-RMS-25} = 4.1558\sqrt{1 + \frac{1}{3}\left(\frac{0.3673}{4.1558}\right)^2} = 4.1613 \tag{44}$$

$$I_{L2-RMS-25} = 1.4693\sqrt{1 + \frac{1}{3}\left(\frac{1.0389}{1.4693}\right)^2} = 1.5870 \tag{45}$$

For V_g = 20:

$$I_{L1-RMS-20} = 5.1948\sqrt{1 + \frac{1}{3}\left(\frac{0.3108}{5.1948}\right)^2} = 5.1979 \tag{46}$$

$$I_{L2-RMS-20} = 1.6427\sqrt{1 + \frac{1}{3}\left(\frac{0.9829}{1.6427}\right)^2} = 1.7380 \tag{47}$$

The inductors rated current must be chosen according to (46) and (47), plus a safety margin.

5.1.2. Capacitors

The capacitance can be chosen from the discussed output voltage ripple section and the comparative evaluation section, in this case, the capacitance was chosen as C_1 = 20 µF, C_2 = 10 µF, which is the combination that leads to Figure 9. The peak voltage of capacitors can be chosen from the equilibrium plus a safety margin; the voltage is usually twice the voltage at the equilibrium, the safety margin is not influenced by the switching ripple, since the voltage ripple in capacitors is a small percentage of their dc-value (in contrast to inductors).

In case it is required, the voltage ripple of capacitors in the proposed operation mode can be evaluated when their respective switch is off; this leads to Equations (45)–(48).

$$\Delta v_{C1} = (1-D)T_S \frac{I_{L1} - I_{L2} - I_o}{2C_1} \tag{48}$$

$$\Delta v_{C2} = (1-D)T_S \frac{I_{L2} - I_o}{2C_2} \tag{49}$$

In the described experiment, the ripple is less than half a volt.

5.1.3. Switches

Switches are rated according to the voltage they need to sustain and current they need to drain; furthermore, the power dissipation is also an important calculation for switches.

The voltage rating is according to the voltage they need to sustain when they are open, in the case of s_1 and s_{1n}, they must be rated to V_{C1}, expressed as (13), in the case of s_2 and s_{1n}, they must be rated to the output voltage V_o, expressed as (15).

The average current transistors need to drain can be expressed as.

$$I_{S1} = DI_{L1} \cdot I_{S1n} = (1-D)I_{L1} \tag{50}$$

$$I_{S2} = DI_{L2} \cdot I_{S2n} = (1-D)I_{L2} \tag{51}$$

In the experiment, the average current through switches is determined as:

For V_g = 25:

$$I_{S1-25} = 0.6464 \times 4.1558 = 2.6865 \tag{52}$$

$$I_{S2-25} = (1-0.6464) \times 1.4693 = 0.9498 \tag{53}$$

For V_g = 20:

$$I_{S1-20} = 0.6838 \times 5.1948 = 3.5521 \tag{54}$$

$$I_{S2-20} = (1-0.6838) \times 1.6427 = 1.1233 \tag{55}$$

If diodes or IGBTs (in synchronous rectification) are chosen for switches (diodes may be used for s_{1n} and s_{2n}), the average current is enough to provide a good approximation to the conduction losses, but if MOSFETS (metal-oxide-semiconductor field-effect transistor) are used (which may be the first option for s_1 and s_2), we need to calculate the RMS current, which is a traditional pulsating waveform with linear ripple, we can use Equation (56), provided in Appendix A of [1].

$$I_{S1-RMS} = I_{L1}\sqrt{D}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_{L1}}{I_{L1}}\right)^2} \tag{56}$$

$$I_{S1n-RMS} = I_{L1}\sqrt{(1-D)}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_{L1}}{I_{L1}}\right)^2} \tag{57}$$

$$I_{S2-RMS} = I_{L2}\sqrt{D}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_{L2}}{I_{L2}}\right)^2} \tag{58}$$

$$I_{S2n-RMS} = I_{L2}\sqrt{(1-D)}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_{L2}}{I_{L2}}\right)^2} \tag{59}$$

In the experiment, the average current through switches is determined as expressed in Equations (60) to (67).

For V_g = 25:

$$I_{S1-RMS} = 4.1558 \times \sqrt{0.6464}\sqrt{1 + \frac{1}{3}\left(\frac{0.3673}{4.1558}\right)^2} = 3.3457 \tag{60}$$

$$I_{S1n-RMS} = 4.1558 \times \sqrt{(1 - 0.6464)}\sqrt{1 + \frac{1}{3}\left(\frac{0.3673}{4.1558}\right)^2} = 2.4743 \tag{61}$$

$$I_{S2-RMS} = 1.4693 \times \sqrt{0.6464}\sqrt{1 + \frac{1}{3}\left(\frac{1.0389}{1.4693}\right)^2} = 1.2760 \tag{62}$$

$$I_{S2n-RMS} = 1.4693 \times \sqrt{(1 - 0.6464)}\sqrt{1 + \frac{1}{3}\left(\frac{1.0389}{1.4693}\right)^2} = 0.9436 \tag{63}$$

For V_g = 20:

$$I_{S1-RMS} = 5.1948 \times \sqrt{0.6838}\sqrt{1 + \frac{1}{3}\left(\frac{0.3108}{5.1948}\right)^2} = 4.2982 \tag{64}$$

$$I_{S1n-RMS} = 5.1948 \times \sqrt{(1 - 0.6838)}\sqrt{1 + \frac{1}{3}\left(\frac{0.3108}{5.1948}\right)^2} = 2.9230 \tag{65}$$

$$I_{S2-RMS} = 1.6427 \times \sqrt{0.6838}\sqrt{1 + \frac{1}{3}\left(\frac{0.9829}{1.6427}\right)^2} = 1.4372 \tag{66}$$

$$I_{S2n-RMS} = 1.6427 \times \sqrt{(1 - 0.6838)}\sqrt{1 + \frac{1}{3}\left(\frac{0.9829}{1.6427}\right)^2} = 0.9773 \tag{67}$$

Finally, there are several approximations to calculate the switching losses; the simplest way is the triangular power approximation, which can be performed with the blocking voltage, the current in switches, and the rise and falling time, which depends on the device.

Table 1 shows the parameter of all elements of the schematic shown in Figure 12, which also coincide with the graphic in Figure 9, and the simulation of Figure 10.

Table 1. Parameters of converters.

L_1 and L_2	440 µH
C_1	20 µF
C_2	10 µF
Switches (all)	TPH3212PS GaN-FET
R	385 Ω

In order to corroborate the operation of the converter in the proposed operation mode, two different operation points were tested in both the former and the proposed operation mode.

Figures 13–16 show important waveforms, in four cases, two different values of D with both the former and the proposed strategy. The output voltage v_o (purple), the input current i_g (green), which is also the current i_{L1} (through inductor L_1), and both gate or firing signals s_1 (brown) and s_2 (blue). All Figures 12–15 show in their (b) index, the same waveforms with a zoom in the output voltage ripple.

The zoom in the output voltage was exceptionally large (output voltage ripple was less than 1%) that the switching noise could be seen, but the waveform and amplitude were consistent with the simulation and the theoretical analysis.

We could observe that despite the switching noise, the experimental results were consistent with the theoretical analysis and the simulation results.

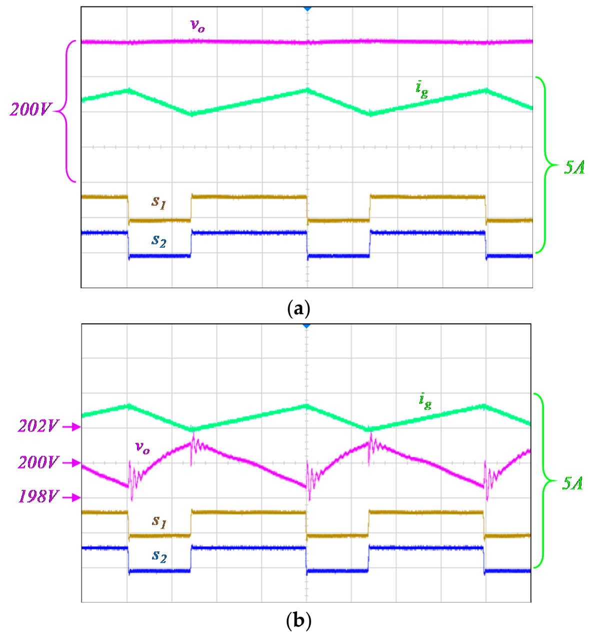

Figure 13. (**a**) The output voltage, input current, and firing signals when D = 0.6476 ($Vg \approx 25$ V) in the former strategy and (**b**) same signals with a zoom in the output voltage ripple.

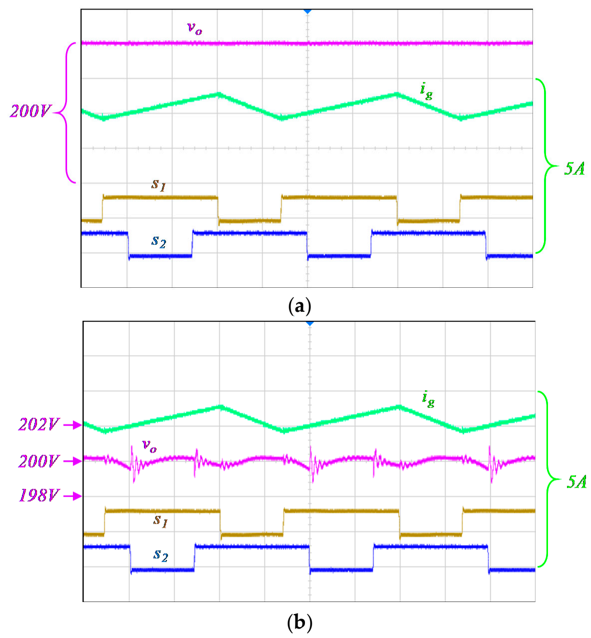

Figure 14. (**a**) The output voltage, input current, and firing signals when D = 0.6476 ($Vg \approx 25$ V) in the proposed strategy and (**b**) same signals with a zoom in the output voltage ripple.

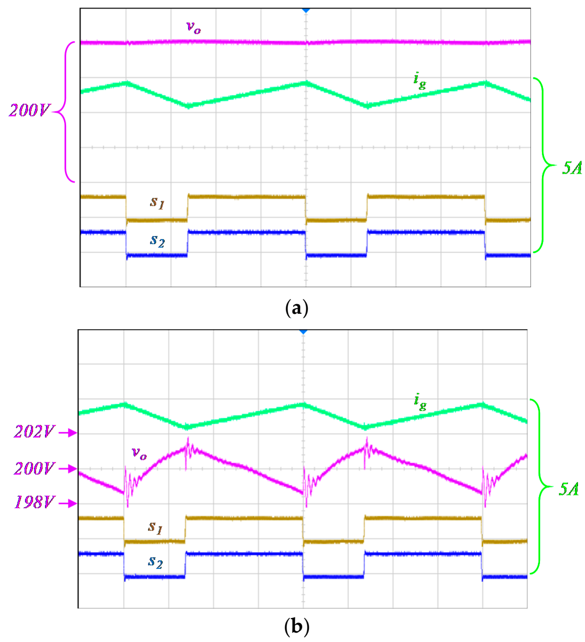

Figure 15. (**a**) The output voltage, input current, and firing signals when D = 0.6543 ($Vg \approx 24$ V) in the former strategy and (**b**) same signals with a zoom in the output voltage ripple.

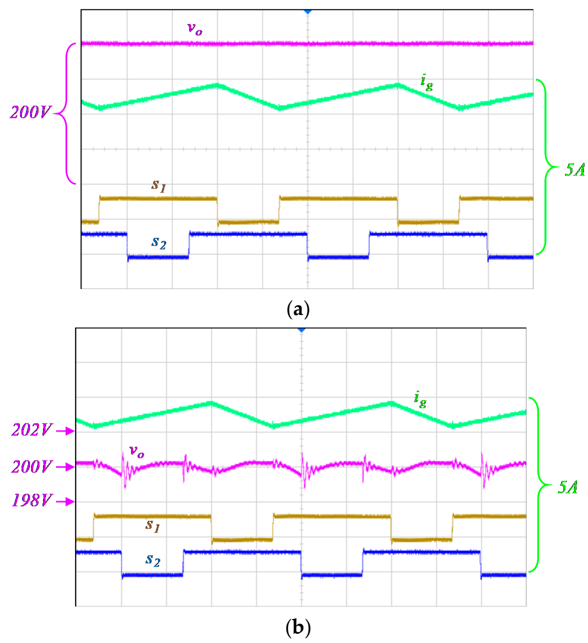

Figure 16. (**a**) The output voltage, input current, and firing signals when D = 0.6543 ($Vg \approx 24$ V) in the proposed strategy and (**b**) same signals with a zoom in the output voltage ripple.

6. Conclusions

This article analyzed the operation mode of the multistage-stacked boost architecture (MSBA) converter working under symmetric operation and proposed their operation with a modified pulse width modulation (PWM) scheme. In the proposed scheme, the switching functions of transistors had the same duty cycle but a phase shift of 180°; the displacement was obtained through an interleaved PWM scheme.

The results showed that the modified PWM results in a similar operation of the converter, it had the same equilibrium and the same power rating in all devices, but it offered a reduction on the output voltage ripple without increasing the switching frequency. A mathematical model of the converter was provided, the output voltage ripple calculation was performed in the traditional, and the modified PWM scheme, simulation, and experimental results were provided to verify the operation mode and the obtained equations.

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