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A Single-Amplifier Dual-Residue Pipelined-SAR ADC

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Abstract: This work presents a 12 bit 200 MS/s dual-residue pipelined successive approximation registers (SAR) analog-to-digital converter (ADC) with a single open-loop residue amplifier (RA). By using the inherent characteristics of the SAR conversion scheme, the proposed ADC sequentially generates two residue levels from the single RA, which eliminates the need for inter-stage gain-matching calibration. To convert the sequentially generated the two residues, a capacitive interpolating SAR ADC (I-SAR ADC) is also proposed. The I-SAR ADC is very compact because it consists of the one comparator, a CDAC, and control logic like a conventional SAR ADC. In addition, the I-SAR ADC needs no static power dissipation for the residue interpolation. A prototype ADC fabricated in a 40 nm CMOS technology occupies an active area of 0.026 mm^2. At a 200 MS/s sampling-rate with the Nyquist input, the ADC achieves an SNDR (Signal-to-Noise distortion ratio) of 62.1 dB and 67.1 dB SFDR (Spurious-Free Dynamic Range), respectively. The total power consumed is 3.9 mW under a 0.9 V supply. Without any inter-stage mismatch calibration, the ADC achieve Walden Figure-of-Merit (FoM) of 19.0 fJ/conversion-step.

Keywords: high speed and high resolution; low power; successive-approximation-register (SAR); analog-to-digital converter (ADC); pipelined-SAR architecture; open-loop residue amplifier; dual-residue; calibration-free; inter-stage mismatch; capacitive interpolation

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1. Introduction

Recently, high-resolution (>10 ENOB (Effective Number of Bits)) and high-speed (>150 MS/s) analog-to-digital converters (ADCs) with low power consumption have become an essential building block in modern wireless communication systems. Owing to the evolution of the CMOS process, the charge-redistribution successive-approximation-register (SAR) ADC is very attractive as a high-performance ADC [1–5]. However, the SAR ADC has a speed bottleneck due to the serial conversion mechanism, and it is difficult to have a high signal-to-noise ratio (SNR) due to the comparator noise.

Among the several architectural approaches, the SAR-assisted pipeline configurations have been proven a promising high-speed high-resolution ADC structure with excellent energy efficiency [6–17]. As shown Figure 1, this type of hybrid ADC uses the low-resolution energy-efficient SAR ADCs and the residue amplifiers (RAs). The ADC enhances noise performance through residue amplification and improves the effective operational conversion speed by operating in a pipeline fashion. However, the RA remains a major design challenge in terms of power, noise, and area. Even though the dynamic amplifiers recently reported in [6,7] showed remarkable power efficiency and speed, the calibration circuitry for accurate residue gain is an unavoidable overhead. Ring amplifiers [15,16] have the advantage of lower power consumption and process scalability, but the design complexity increases to achieve high DC gain for accurate inter-stage gain. To avoid the accurate gain requirement of the RA, dual-residue pipelining schemes have been proposed [17–23]. Because the conversion scheme uses the ratio of the two residues to find the LSB code, it is important that the two residues are amplified by the same gain value. This means that the relative gain value between the two RAs is more important than the absolute gain value. Although the requirement is relaxed because the residue amplifier is not designed with an

absolute gain value, the two RAs that still need to have matched gain is another design overhead.

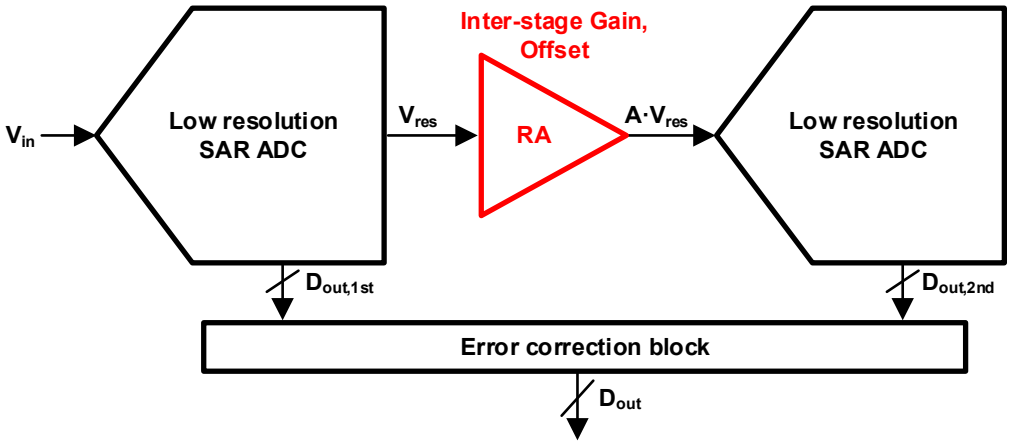


Figure 1. Block diagram of the Pipelined-SAR ADC.

With the pros and cons of the previous architectural approaches, a structural consideration is needed to reduce the design complexity without the need for additional calibration logic while reducing the power burden by reducing the amplifier requirement. Hence, this paper presents a new dual-residue pipelined-SAR architecture that uses a single open-loop residue amplifier. The proposed ADC does not require any inter-stage mismatch calibration for an accurate gain. We also introduce a capacitive interpolating SAR ADC (I-SAR ADC) for the two-residue interpolation. The I-SAR ADC needs no static power consumption for the residue interpolation. A 12 b 200 MS/s prototype ADC demonstrates the feasibility of the new architecture [22].

This article is organized as follows. In Section 2, the conventional dual-residue architecture is reviewed. Section 3 introduces the proposed single-amplifier dual-residue generation technique and a capacitive interpolation SAR ADC as a low power sub-stage ADC. Section 4 shows the proposed architecture and hardware implementation. Finally, Section 5 presents the measured performance of the prototype ADC and comparison. Finally, Section 6 concludes this article.

2. Review of Dual-Residue Processing Concept

Figure 2a shows the structure of the pipelined ADC proposed in [19]. According to the result of analog-to-digital conversion performed by the first flash ADC (Flash 1), the two-residue architecture uses the differences between the input signal and the closet quantization levels (V_{r+} and V_{r-}). In other words, the voltage levels of two residues are determined according to the input level within a full scale of 1 LSB. In addition, then, the complementary residues are amplified by two RAs (A1 and A2), respectively. Finally, the second stage (Flash 2) can determine the output code by interpolating the two amplified residues with opposite polarity. For this operation, the exact gain values of the two RAs are not as important as the conventional pipeline ADC because the relative position of the ground level is an input information. As shown in Figure 2b, the architecture operates correctly no matter what value is chosen for the inter-stage gain, provided that both residue gains match. This means that the dual-residue architecture eliminates the need for the absolute gain accuracy. Additionally, since the amplified complementary residues (the outputs of the RAs) are used to determine the LSB code from the second stage, a reference voltage is not required. However, if the amplifiers have different gains, the ADC cannot avoid performance degradation (Figure 2c). Therefore, the required gain and offset matching burden is still considerable.

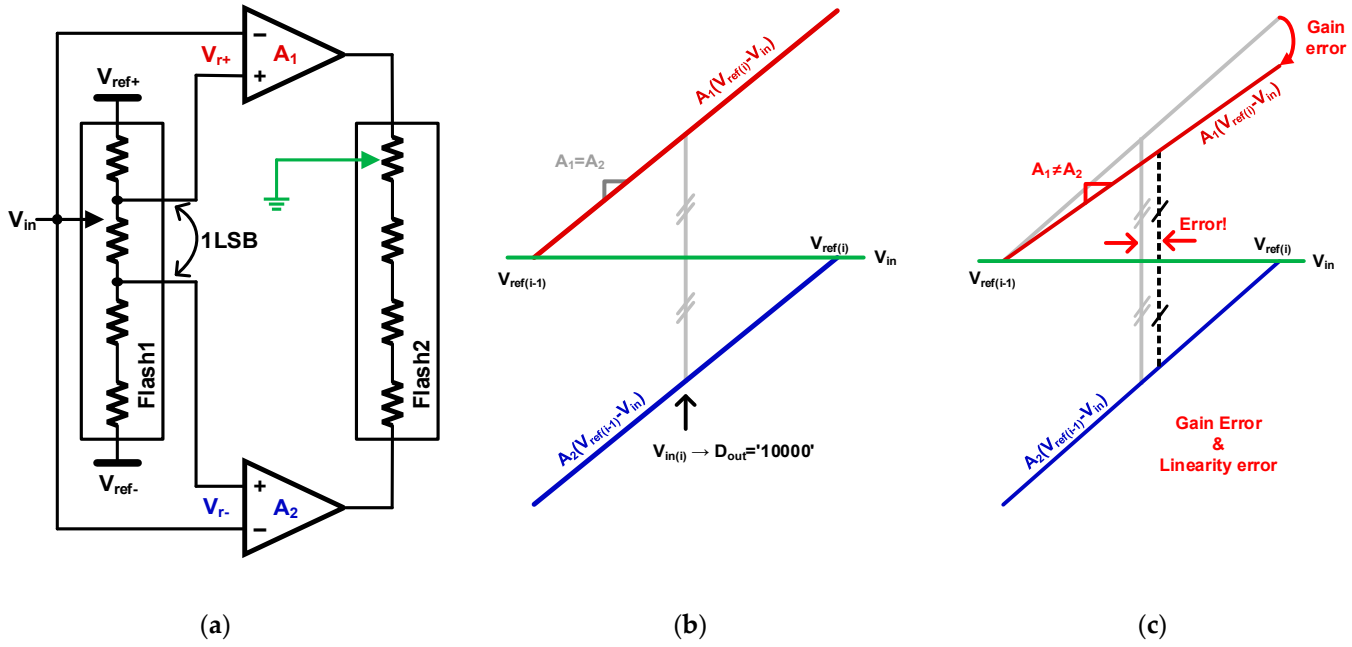


Figure 2. Dual-residue processing concepts: (**a**) Block diagram from [19]; (**b**) Residue profile with matched gain; (**c**) Residue profile with mismatched gain.

Figure 3 shows the previous implementations for interpolating the two complementary residues. With the same interpolation scheme as in [19], the resistor-based (R-based) network reported in [23] can easily output multiple interpolated levels (Figure 3a). However, the R-based network requires an additional capacitor DAC (CDAC) for the pipeline operation and thus requires a large area. In addition, static power is consumed because RAs must be powered continuously for interpolation operation. In the capacitor-based (C-based) network reported in [20], the static current does not flow (Figure 3b). However, there are many switches connected to the critical node (V_{ra+} and V_{ra-}). With the connection, the junction capacitance of the switches causes the linearity issue of interpolated levels. In conclusion, a new interpolation structure that has a small area but does not consume static power and does not have linearity issues is needed.

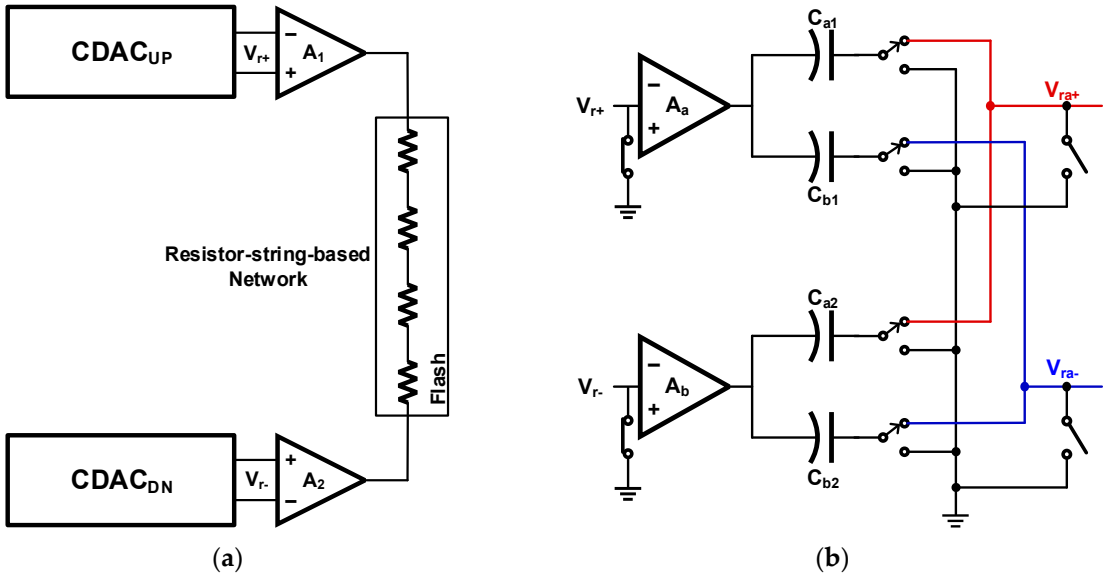


Figure 3. Interpolation schemes: (**a**) Resistor-based interpolation in [19,23]; (**b**) Capacitor-based interpolation in [20].

3. Proposed Architecture

Based on the earlier discussions, a new pipelined SAR architecture is proposed that uses only a single RA, which requires neither gain accuracy nor matching, allowing calibration-free open-loop RA (Figure 4). In addition, a capacitive interpolation SAR ADC for the second stage is also proposed for low power fine analog-to-digital conversion.

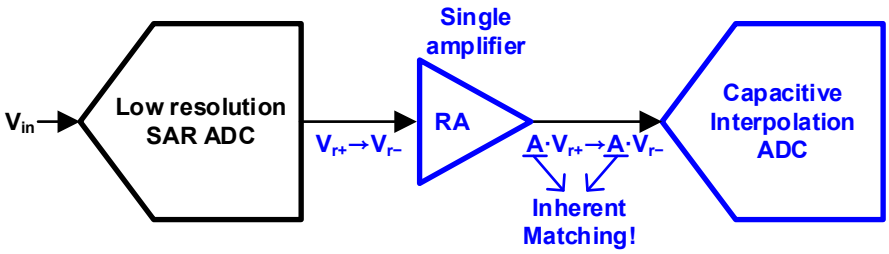
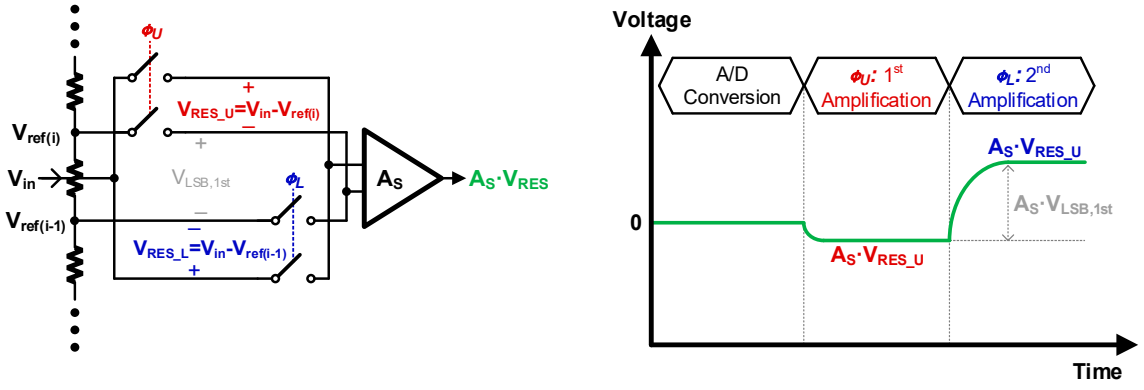


Figure 4. Block diagram of the proposed dual-residue pipelined-SAR ADC.

3.1. Dual-Residue Generation with a Single Amplifier

Figure 5 explains the conceptual block diagram and operation of the proposed single-amplifier dual-residue technique. As shown in Figure 5a, unlike the conventional architecture, in which two RAs that simultaneously amplify two residues, the proposed scheme is that two residues are sequentially amplified with one residue amplifier. The residue voltage waveform is demonstrated phase-by-phase in Figure 5b. After A/D conversion, the closest quantization levels ($V_{ref(i)}$ and $V_{ref(i-1)}$) can be decided. When Φ_U is enabled, V_{RES_U} is amplified by the RA with gain of As. V_{RES_U} represents the difference between the input signal (V_{in}) and the larger value among the quantization levels ($V_{ref(i)}$) closest to V_{in}. After sampling $As \cdot V_{RES\_U}$ in the following stage, V_{RES_L} is amplified and transferred. Please note that the resolution of the coarse ADC is sufficiently fine (>5 bit), a gain mismatch between the two residues rarely occurs.



(**a**) (**b**)

Figure 5. Conceptual operations from Flash ADC: (**a**) Block diagram; (**b**) Timing diagram.

Figure 6 explains the principle of the proposed single-amplifier dual-residue technique in SAR ADC. The proposed technique generates two residues sequentially by taking advantage of the SAR operation: Assuming that the LSB of the coarse decision is '0', the upper residue V_{RES_U} is generated on the first-stage CDAC when the coarse SAR conversion is completed. In the example shown in Figure 6a,b, the LSB decision is done by switching C_{LSB} from V_{cm} to V_{ref-}. When V_{RES_U} is generated by switching C_{LSB}, the 1st amplification (Φ_U) operation is performed. To generate a lower residue, V_{RES_L}, only 1-LSB transition of the coarse resolution is required, which can be simply done by switching the termination capacitor C_{TEM}. As shown in Figure 6c,d, V_{REF_L} is can be generated by switching CTEM to V_{ref+} from V_{cm} after 1st amplification. Please note that the proposed

technique does not require an additional hardware burden and only requires 1 cycle of timing to generate a complementary residue. In addition, unlike the conventional scheme, the sequentially generated two residue signals are amplified by a single RA (with the gain of A_S) and sampled by the second stage sequentially. This single-amplifier dual-residue technique provides inherently gain-matched residues. Thus, a simple open-loop RA can be used as long as it satisfies the required backend linearity.

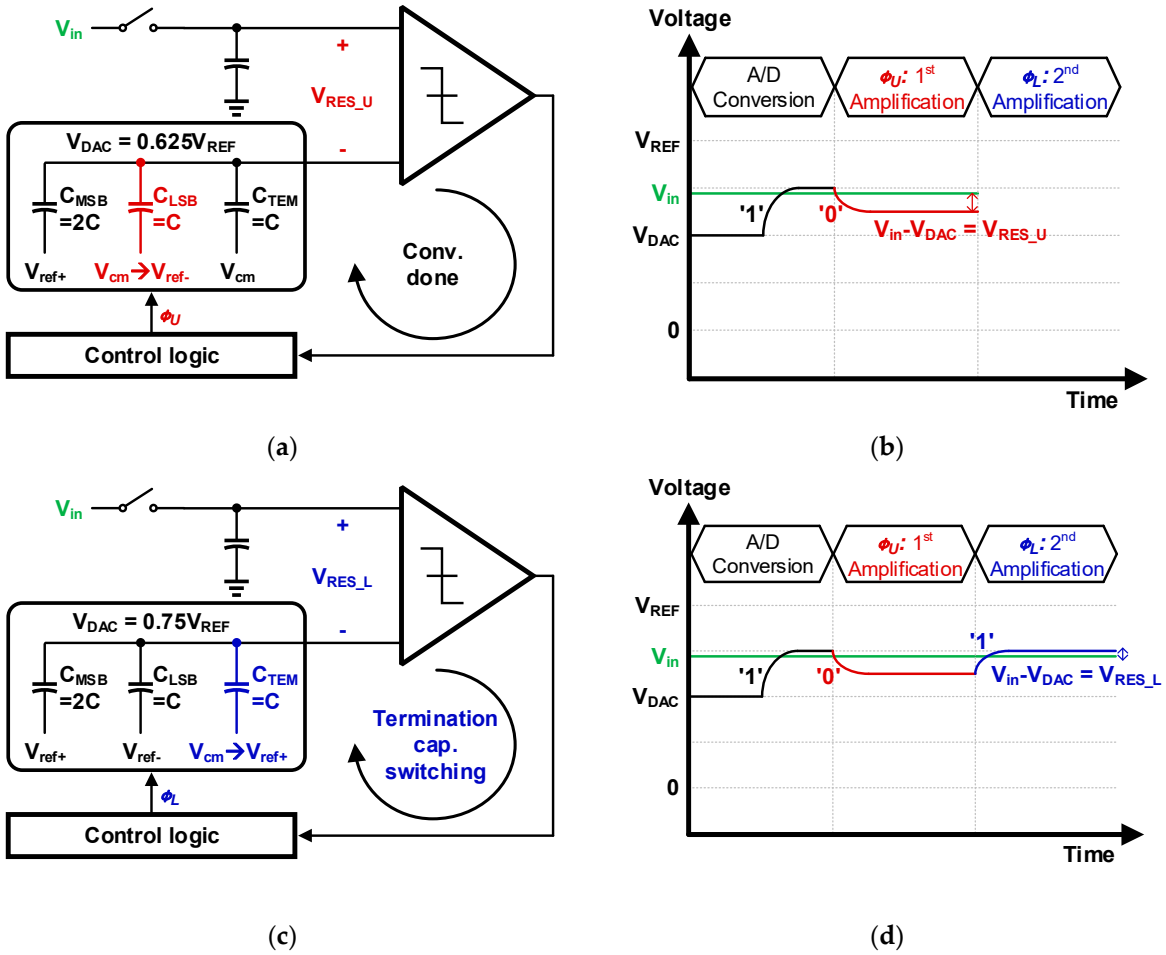
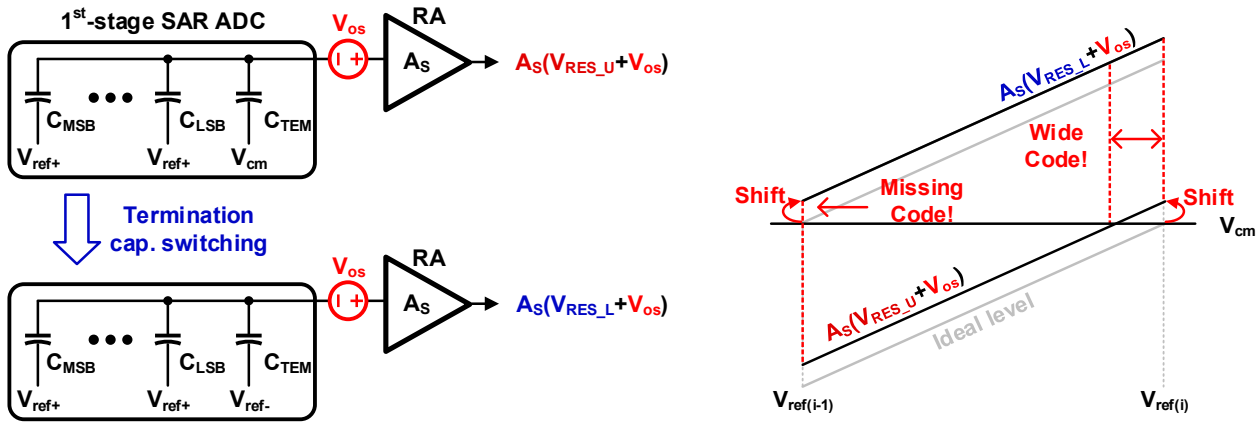


Figure 6. Conceptual operations from SAR ADC: (**a**) Block diagram; (**b**) Timing diagram; (**c**) Block diagram; (**d**) Timing diagram.

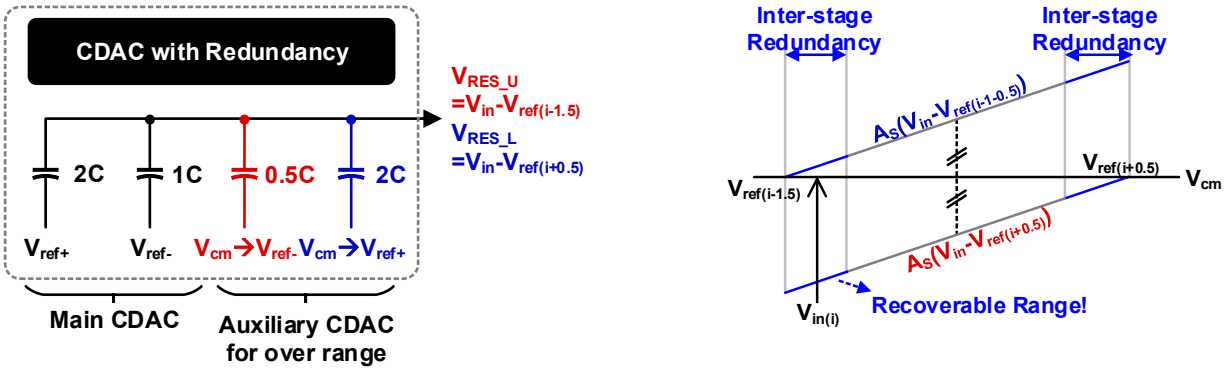
However, there are other non-idealities to consider. First, the amplifier offset needs to be considered. As shown in Figure 7a, if the amplifier has an offset, two residues (V_{RES_U} and V_{RES_L}) are amplified by including an amplifier offset with the same polarity. Figure 7b shows the residue profile when the amplifier offset occurs. Please note that the *x*-axis direction means the level of the input signal at the 1st stage, and the *y*-axis direction means the level after amplification. From the shifted residue profile, the amplifier reduces linearity by generating missing and wide codes as well as fine code offset. Additionally, the input level may be out of the acceptable range due to disturbance such as settling error or comparator noise in the first stage ADC.



(**a**) (**b**)

Figure 7. Non-idealities in the proposed architecture: (**a**) Schematic with the residue amplifier offset mismatch; (**b**) Residue profile.

To overcome these issues, the over-ranged residue generation technique is proposed. In other words, we intentionally choose reference levels to generate the two residues with recoverable range as much as +/− 0.5 LSB scale of inter-stage redundancy. In the example shown in Figure 8a, in addition to the main CDAC, which determines the code of the 1st stage, an auxiliary CDAC for over-ranged residue generation was implemented. Since only the capacitance weight of the LSB scale is needed, the area increase is insignificant, less than 0.04% for the 12-bit prototype ADC. When the coarse conversion is done, V_{RES_U} is generated based on $V_{ref(i+0.5)}$, and V_{RES_L} is generated based on $V_{ref(i-1.5)}$. Owing to the inter-stage redundancy presented by the proposed over-ranged residue generation technique, a recoverable range is allowed even if comparator noise or amplifier offset occurs, as shown in Figure 8b. The final digital code is output through the digital error correction block using the coarse code of the 1st stage and the fine code of the 2nd stage.



(**a**) (**b**)

Figure 8. Proposed over-ranged residue generation technique: (**a**) Schematic for conceptual operation; (**b**) Residue profile with inter-stage redundancy.

3.2. Capacitive Interpolation SAR ADC (I-SAR ADC)

As mentioned in Section 3.1, two residues are amplified with the identical gain in time sequence through a single amplifier. To sample sequentially generated residues and interpolate them efficiently, we propose a new structure.

Figure 9 shows the detailed schematic of the proposed capacitive interpolation SAR ADC (I-SAR ADC). The I-SAR ADC consists of two sub-CDACs ($CDAC_U$, $CDAC_L$) with

identical weighted capacitors and samples V_{RES_U} and V_{RES_L} to the sub-CDACs through a bottom-plate sampling manner. The top node shared by the two sub-CDACs is connected to only one V_{cm} switch for charge initialization in the phase of Φ_{top}, minimizing non-linearity issues due to junction capacitance. In addition, it has very high area efficiency by using one comparator and SAR control logic.

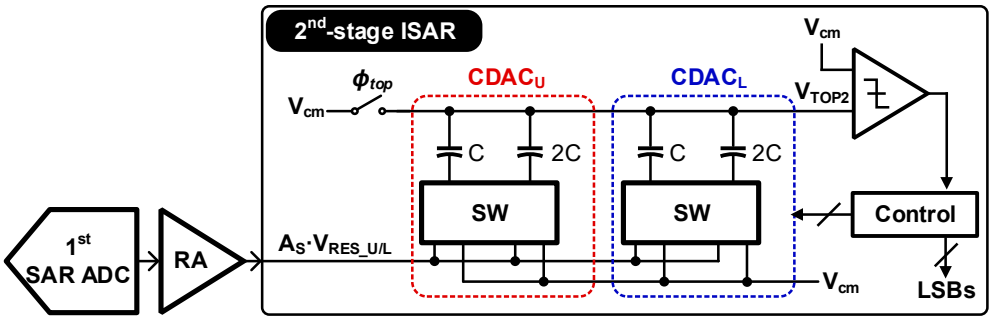


Figure 9. Schematic of the proposed interpolation SAR ADC.

Figure 10 shows how to interpolate the two amplified residues to resolve LSBs with the I-SAR ADC, with a simplified 2b example. The two amplified residues, $A_S \cdot V_{RES\_U}$ and $A_S \cdot V_{RES\_L}$, are sampled on the 2nd-stage CDAC in sequence. As shown in Figure 10a, when $A_S \cdot V_{RES\_U}$ is sampled on $CDAC_U$, the bottom plates of $CDAC_L$ are floated. In the phase of Φ_L, $A_S \cdot V_{RES\_L}$ is sampled to $CDAC_L$ and $CDAC_U$ is floated to preserve the sampled $A_S \cdot V_{RES\_U}$. During the residue sampling phases, the V_{cm} level is continuously applied to the top node. Thereafter, residue interpolation is conducted for LSBs decision. Figure 10c,d shows the connection of the bottom switches and the corresponding voltage waveform at the top node. First, MSB of the 2nd-stage (MSB_{2nd}) is determined by charge-sharing the two smallest capacitors, C, with V_{cm} while other capacitors are floated, resulting in $V_{TOP2} = (V_{RES\_U} + V_{RES\_L})/2$. If the first conversion gives $MSB_{2nd} = 0$, meaning the residue is on the V_{RES_L} side, the following interpolation is conducted by connecting the 2C in $CDAC_L$ to V_{cm}, making $V_{TOP2} = (1 \times V_{RES\_U} + 3 \times V_{RES\_L})/4$ for MSB_{2nd-1} decision, according to the SAR principle (Figure 10d). Please note that the charge frozen on the floating 2C in $CDAC_U$ does not contribute to the output.

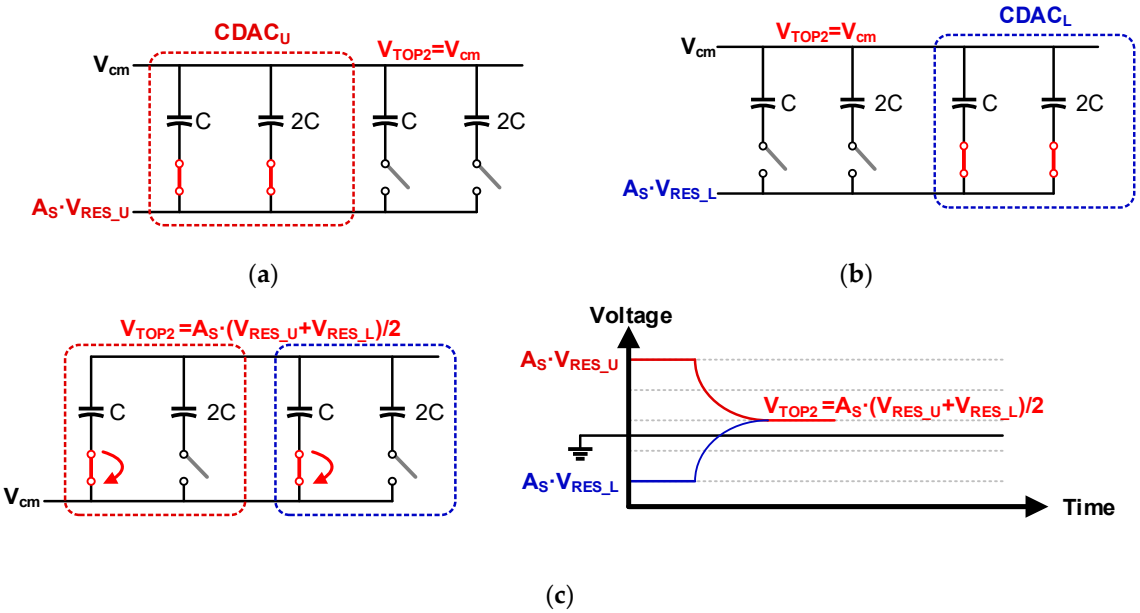
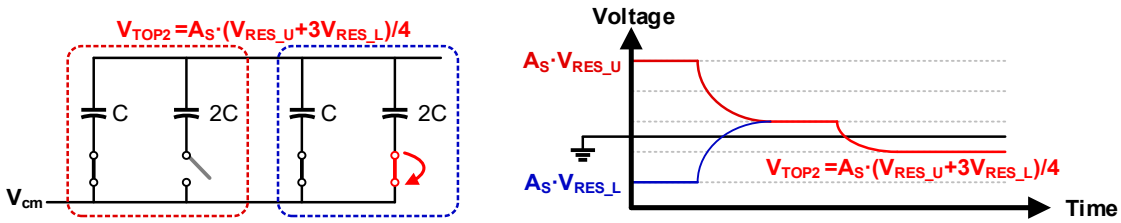


Figure 10. *Cont.*



(**d**)

Figure 10. Conceptual operations from SAR ADC: (**a**) VRES_U sampling on CDACU; (**b**) V_{RES_L} sampling on $CDAC_L$; (**c**) MSB_{2nd} conversion; (**d**) MSB_{2nd-1} conversion.

As shown in Figure 11, with two higher-resolution weighted CDACs, the 2nd stage I-SAR ADC can resolve the higher resolution. The interpolated level on the top node (V_{top2}) is determined as follows:

$$V_{top2} = \frac{N_U \times (A_s \cdot V_{RES_U}) + N_L \times (A_s \cdot V_{RES_L})}{N_U + N_L} \quad (1)$$

where N_U and N_L is the total weight of capacitors connected to the top node in their CDACs ($CDAC_U$ and $CDAC_L$), respectively. Please note that the proposed interpolation scheme with floating capacitors does not require additional references, while layout should be carefully done so that the parasitic capacitance does not affect the performance. Even though the top-node parasitic may reduce the residue gain, it does not degrade the linearity owing to the dual residue principle, as explained in Section 3.1.

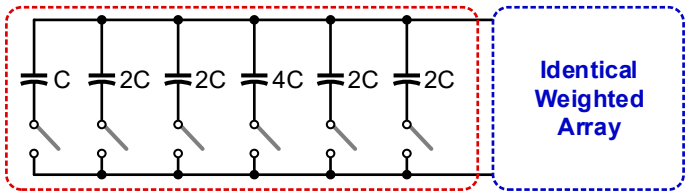


Figure 11. CDAC configuration for higher resolution.

4. Hardware Implementation

Figure 12a,b shows the architecture and operational timing diagram of the prototype pipelined-SAR ADC with the proposed single-amplifier dual-residue generation technique and the I-SAR ADC. The digital error correction logic receives 9 bit code from 1st stage ADC and 5 bit code from 2nd stage ADC to determine final 12 bit output.

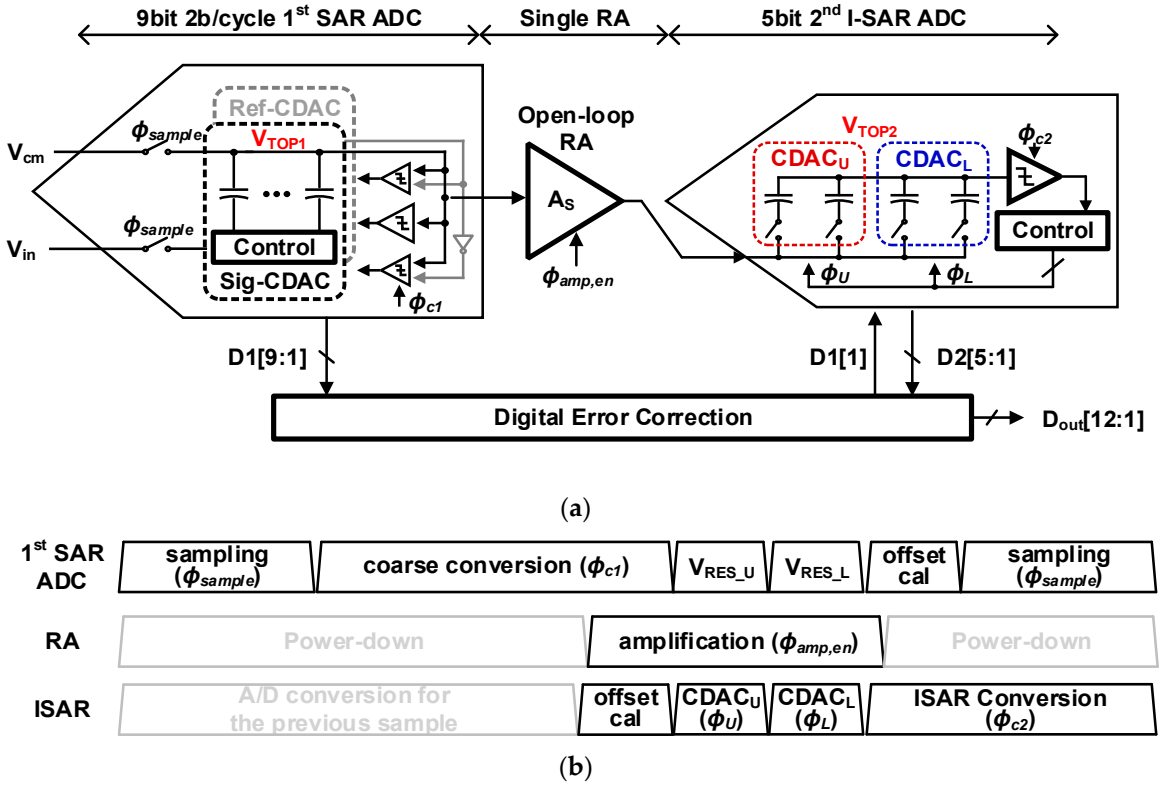


Figure 12. (**a**) Architecture for the prototype ADC with the proposed techniques; (**b**) Timing diagram. Reprinted with permission from Ref. [22]. Copyright 2019 the Japan Society of Applied Physics.

4.1. 1st-Stage ADC: Multi-Bit SAR ADC with Background Calibration

The 1st-stage SAR ADC consists of 9-bit non-binary (8b full-binary equivalent) CDACs, two 8-bit CDACs to generate additional reference signals, the bootstrapped switches in [24] and SAR control logic. Figure 13 depicts the simulated differential nonlinearity (DNL) and integrated nonlinearity (INL). According to the simulation results, the target mismatch of the unit capacitor is determined to be 0.5%. Therefore, the unit capacitance of the CDAC is determined to be 5.1 fF with a sandwich-structured capacitor [25]. The SAR ADC has three comparators for operating in a 2b/cycle manner [26]. A total of six cycles are used to determine 9-bit code, and the first three cycles are determined by 2-bit, and the subsequent three cycles are determined by 1-bit. After the A/D conversion, the residue signals are generated on the SIG-CDAC in this particular design.

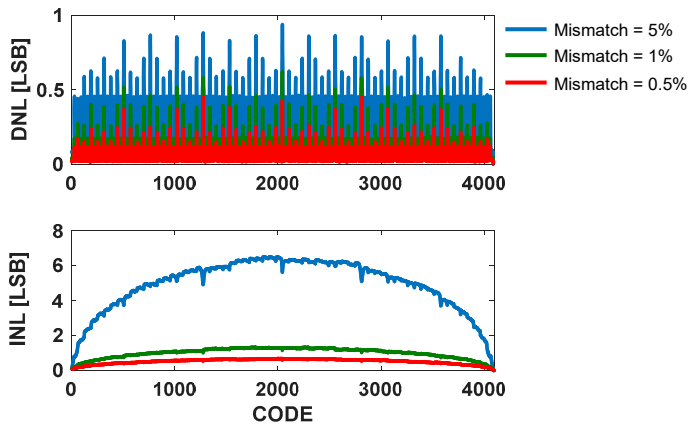


Figure 13. CDAC Mismatch Simulation.

4.2. Residue Amplifier

Although the dynamic amplifier in [6,7] is a power-efficient structure as a residue amplifier, a signal integration period is essential for high gain and low noise characteristics. Therefore, the integration time to degrades the operating speed for our structure where the two residues are amplified twice. Owing to the RA-gain-irrelevant principle, we can use a simple two-stage open-loop amplifier as RA (Figure 14). The RA has a very compact structure, as there are no additional transistors for any calibration. The gain is designed to be around 14, considering the noise and speed requirements. The 2nd stage of the RA is turned on only during the residue amplification phase ($\Phi_{amp,en}$) for power saving. To prevent the linearity degradation, a power gating scheme was not applied for 1st stage of the RA.

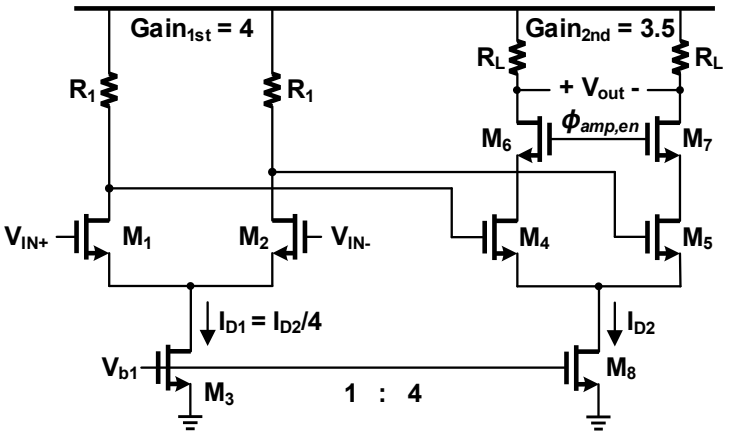


Figure 14. Open-loop residue amplifier. Reprinted with permission from Ref. [22]. Copyright 2019 the Japan Society of Applied Physics.

4.3. 2nd-Stage ADC: Proposed Successive-Approximation Interpolation ADC

The 2nd-stage I-SAR ADC has a 5-bit resolution, including 1-bit redundancy. Considering the matching requirement, the unit capacitance of the CDAC for I-SAR ADC is determined to be 3.6 fF with a finger-type structure. The two sequentially generated residues are sampled to $CDAC_U$ and $CDAC_L$ during Φ_U and Φ_L, respectively. Please note that only a single additional clock is required (i.e., Φ_L) for the proposed dual-residue operation compared with typical pipelined-SAR operations. The two sampled dual residues are interpolated by the I-SAR ADC during Φ_{c2}, while a new input is sampled on the 1st-stage SIG-CDAC.

5. Measurement Results and Discussion

A prototype 12 bit 200 MS/s pipelined-SAR ADC with the proposed single-amplifier dual-residue architecture and I-SAR ADC was implemented in 40 nm CMOS technology. Figure 15 shows a die photograph of the chip. Due to the open-loop residue amplifier without any mismatch calibration block and the simple interpolation network, the active area of the ADC core is only 260 um $\times$ 100 um (0.026 mm^2).

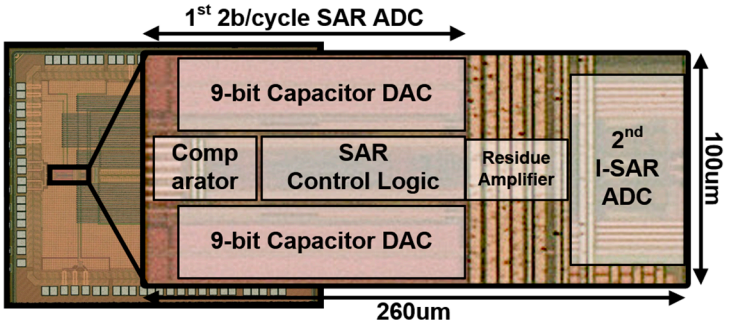


Figure 15. Die photograph. Reprinted with permission from Ref. [22]. Copyright 2019 the Japan Society of Applied Physics.

At a sampling rate of 200 MS/s, the measured power consumption is 3.9 mW under a 0.9 V supply. Figure 16 shows the detailed power breakdown. The 1st-stage SAR ADC takes the largest portions, accounting for 42% of the total power consumption. In the 1st-stage SAR ADC, the power consumption of three comparators is about 0.61 mW for 2-bit/cycle operation. The second largest portion of total power consumption is taken by the residue amplifier. Depending on the ratio of the current consumption, the 2nd amplifier consumes four times more energy than the 1st amplifier. In the 2nd I-SAR ADC, most of the power of about 0.68 mW is consumed by the comparator and the SAR control logic.

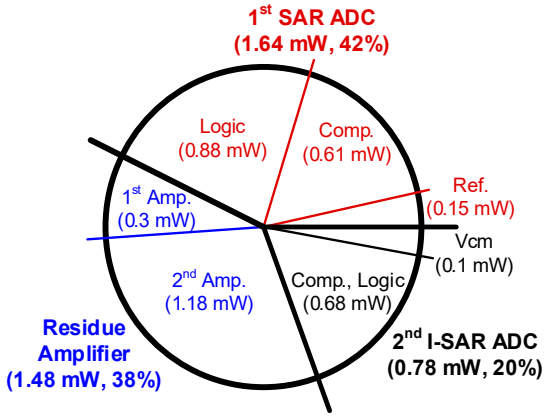


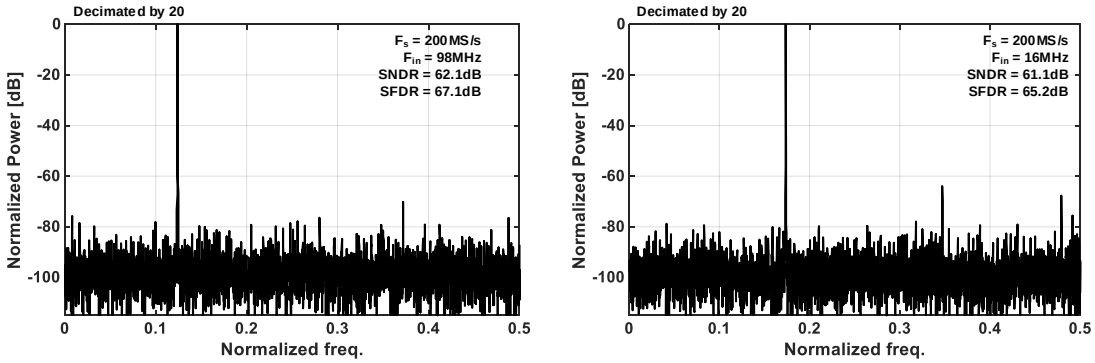
Figure 16. Power breakdown.

Figure 17 shows the measured fast Fourier transform (FFT) spectrum depending on the input frequencies. The results are decimated by a factor of 20. For a Nyquist-rate input, the measured spurious-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are 62.1 dB and 67.1 dB, respectively. For 16 MHz as a low frequency input, the measured SNDR and SFDR are 61.1 dB and 65.2 dB, respectively.

Figure 18 shows the dynamic performance for various input frequencies and sampling frequencies. Figure 18a plots the measured SNDR and SFDR values versus the input frequency at 200 MS/s. From low input frequency to Nyquist frequency, the resultant effective number of bits (ENOB) is around 9.85 bits or above. Figure 18b plots the measured SNDR and SFDR values versus the sampling rates with a low frequency input.

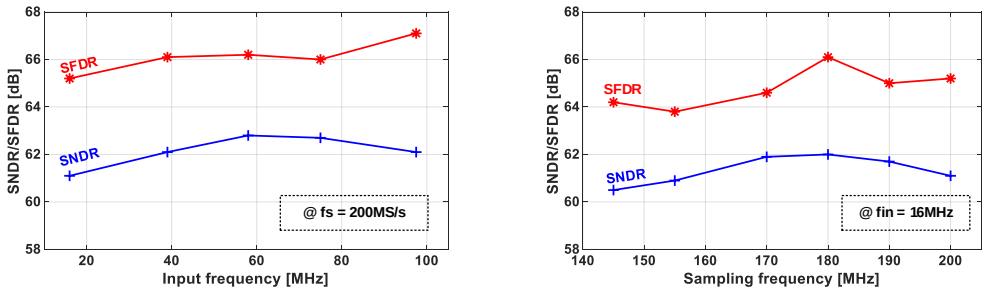
Table 1 summarizes and compares the prototype ADC performance to state-of-the-art pipeline ADCs and pipelined-SAR ADCs. The prototype ADC in this work shows the smaller area because no additional calibration circuitry for residue amplifier is needed. In addition, the compact of I-SAR ADC contributes to the small implementation. Compared with previous calibration-free ADCs, the ADC in this work achieved much higher SNDR and Figure of Merit. Unlike other designs, the proposed ADC does not require gain calibration, achieving a competitive Walden Figure-of-Merit (FoM_w) of 19.0 fJ/conversion-

step. These results show that the proposed ADC with the dual-residue scheme could be a promising pipelined SAR architecture for high-speed and high-resolution applications.



(**a**) (**b**)

Figure 17. Measured spectrum at 200 MS/s with: (**a**) Nyquist input; (**b**) 16 MHz input. Reprinted with permission from Ref. [22]. Copyright 2019 the Japan Society of Applied Physics.



(**a**) (**b**)

Figure 18. Measured SNDR and SFDR versus: (**a**) various input frequencies at 200 MS/s; (**b**) various conversion rates at 16 MHz. Reprinted with permission from Ref. [22]. Copyright 2019 the Japan Society of Applied Physics.

Table 1. Performance comparison. Reprinted with permission from Ref. [22]. Copyright 2019 the Japan Society of Applied Physics.

	This Work	**VLSI11 Miyahara**	**ISSCC15 Boo**	**VLSI14 Zhou**	**ISSCC17 Yoshioka**	**ISSCC17 Huang**
Architecture	Dual residue Pipelined-SAR	Dual residue Pipeline	Pipeline	Pipelined-SAR	Pipelined-SAR	Pipelined-SAR
Resolution	12	10	12	12	12	12
Technology (nm)	40	90	65	40	28	65
Area (mm^2)	0.026	0.46	0.59	0.24	0.1	0.08
Sampling Speed (1 Channel) (MS/s)	200	320	250	160	80	330
SNDR (dB)	62.1	53	65.7	65.3	61.1	63.5
SFDR (dB)	67.1	65	84.6	86.9	72.7	83.4
Power (dB)	3.9	40	49.7	4.96	1.9	6.23
FoMw [1] (fJ/conversion-step)	19.0	390	108.5	20.7	12.8	15.4
Inter-stage Mismatch Calibration	Not Required	Relative Gain Calibration	Off-chip Calibration	Digital Background Calibration	Assisted by Digital Amplifier	Replica Dynamic Amplifier

[1] Walden FoM = Power/(2^{ENOB} × Sampling frequency).

6. Conclusions

This paper proposed a 12 bit 200 MS/s dual-residue pipelined-successive approximation registers analog-to-digital converter with only one residue amplifier. By using the inherent characteristics of the SAR conversion scheme, the proposed design generates two residue signals from the single amplifier, which eliminates the need for inter-stage gain-matching calibration. A capacitive interpolating SAR conversion technique was also introduced for the second stage for power efficiency and small area. Owing to these techniques, the single-channel 12 bit 200 MS/s prototype ADC achieved the SNDR of 62.1 dB and 67.1 dB SFDR at a sample rate of 200 MHz. In addition, from low input frequency to Nyquist input frequency, the ENOB stayed above 9.85 bits. Finally, the prototype ADC achieved a Walden figure-of-merit values of 19.0-fJ/conversion-step without any calibration scheme for the residue amplifier. Moreover, the prototype ADC had the smallest area, at 0.026 μm^2, among previously published pipelined-SAR ADCs.

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Abbreviations

SAR	Successive-approximation-register
ADC	Analog-to-digital Converter
RA	Residue Amplifier
I-SAR ADC	Interpolation SAR ADC
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise distortion ratio
SFDR	Spurious-Free Dynamic Range
ENOB	Effective Number of Bits
DNL	Differential Non-Linearity
INL	Integrated Non-Linearity
FoMw	Walden figure-of-merit

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